FRESCO LOGIC

Product Datasheet

FL1009

PCI Express to Dual USB 3.0 Host Controller

Revision 0.98a

October 2011

Fresco Logic **CONFIDENTIAL**

Revision History

Revision	Date	Comment
0.91	3 Dec 2010	Initial release of DRQFN package.
0.92 PR	17 Dec 2010	Pre-release version of FL1009-2Q0
0.93 PR	7 Jan 2010	Move pin B37 from NC to TESTN
0.94	19 Jan 2011	Update supported crystal frequency and related control pin Update power measurement data Add power down sequence
0.95	1 Apr 2011	Update power consumption data
0.96	1 Jun 2011	Update power consumption data
0.97	10 Jul 2011	Changing signal type to LVTTL of following pins: SMIN, ROMSDA, ROMSCL Update operating current data Add Appendix C SMT Thermal Profile
0.98a	31 Oct 2011	Update reference footprint: Appendix A

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1. Introduction

The FL1009 is Fresco Logic's single-chip PCI Express to USB 3.0 host controller. It fully integrates an Extensible Host Controller Interface (xHCI) engine, a dual-port 5Gbps USB 3.0 transceiver, a PCI Express endpoint controller and a 5Gbps PCI Express transceiver. FL1009 implements the Universal Serial Bus 3.0 Specification Revision 1.0 and the Extensible Host Controller Interface (xHCI) Specification Revision 1.0, and complies with the PCI Express Rev 2.1 Specification at 5Gbps data rate, and the PCI Local Bus Specification Revision 2.2. FL1009 is backward compatible for operation with USB 2.0 and USB 1.1 devices.

The FL1009 controller features Fresco Logic's patented GoXtream™ xHCI Accelerator Engine, which maps the xHCI standard directly into a set of parallel functional units, providing acceleration of all xHCI operations while maintaining compatibility with existing software driver models.

With its innovative architecture and high level of integration, FL1009 delivers exceptional performance, while minimizing total system cost and providing the most straightforward usage model in the industry.

The FL1009 controller is available in the following package:

- DRQFN, 116 pin, 9mm×9mm

1.1 Features

- Compliant with USB 3.0 Specification Revision 1.0
- Compliant with Extensible Host Controller Interface (xHCI) Specification Revision 1.0
- 2 downstream USB ports support SS/HS/FS/LS data rates (5Gbps/480Mbps/12Mbps/1.5Mbps)
- Support charging downstream port of Battery Charging Specification Revision 1.1
- Single (x1) PCI Express Lane
- Supports PCI Express Specification Revision 2.1 at 5GT/s
- Supports PCI Express Card Revision 1.0
- Supports PCI Bus Power Management Interface Specification Revision 1.2
- 3.3V/1.05V power supply
- Support 12MHz crystal oscillator
- Integrated SuperSpeed USB Transceiver
- Integrated PCI Express Transceiver
- WHQL certified driver support for Windows 7, Windows Vista and Windows XP, as well as Linux

1.2 Applications

- Motherboard
- Notebook
- Add-in card
- Express card
- DTV
- Embedded PC
- Any consumer product with PCIe interface

1.3 Ordering Information

Table 1-1 Ordering Information

Part Number	Description	Status
FL1009-2Q0	DRQFN 116-pin 9mm×9mm	Production

1.4 Top Marking

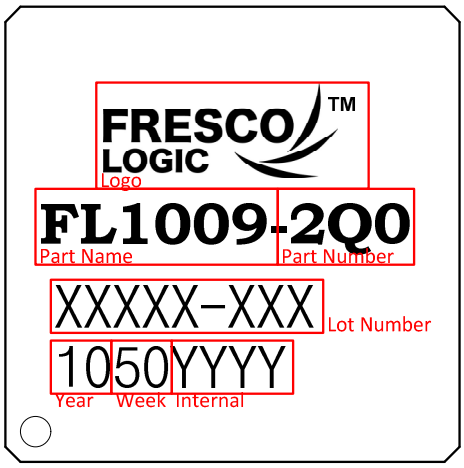


Figure 1 FL1009 Top Marking

Figure 1 illustrates the top marking of FL1009 samples. The part number is composed of two portions: “FL1009” is the part name, which tells the product family; the “2Q0” denotes the major stepping and the package type as revision 2 and DRQFN package respectively.

2. Signal Description

This chapter provides signal mapping and detailed description of each signal of FL1009. The following notations are the signal type:

- LVTTL Digital control signal
- DIFF Analog Differential pair
- ANA Analog I/O
- OD Open Drain I/O

2.1 Ballout Definition

Figure 2 shows the ballout map of FL1009 from the top of the package view.

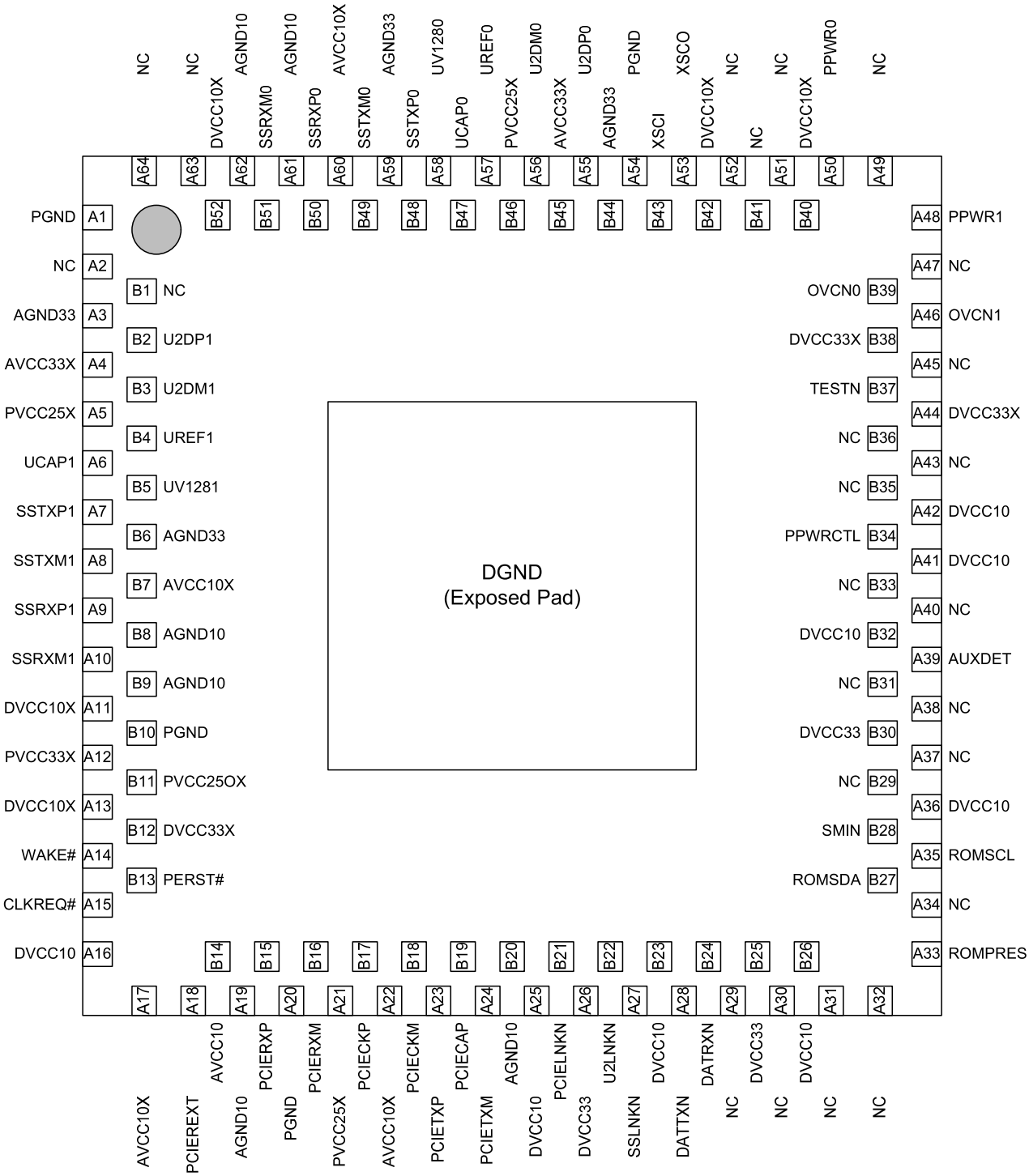


Figure 2 FL1009 Ballout Map (Top view / Transparent View)

2.2 Signal Descriptions

This section contains detailed signal for each interface.

2.2.1 PCI Express Interface

Table 2-1 Signal description of PCIe Interface

Pin Name	Ball#	Type	Dir.	Description
WAKE#	A14	OD	O	PCIe wakeup signal, active low
CLKREQ#	A15	OD	O	Indicate when REFCLK is needed for express card, active low
PERST#	B13	LVTTL	I	PCIe reset, active low
PCIECKP	B17	DIFF	I	PCIe differential clock (+), 100MHz
PCIECKM	B18	DIFF	I	PCIe differential clock (-), 100MHz
PCIEREXT	A18	ANA	O	Connect an external resistor (12kΩ ± 1%) to AGND33
PCIECAP	B19	ANA	O	Connect an external capacitor 100nF to AGND33
PCIERXP	B15	DIFF	I	The PCI Express differential inputs to the PHY (+)
PCIERXM	B16	DIFF	I	The PCI Express differential inputs to the PHY (-)
PCIETXP	A23	DIFF	O	The PCI Express differential outputs from the PHY (+)
PCIETXM	A24	DIFF	O	The PCI Express differential outputs from the PHY (-)

2.2.2 USB Port 0 Interface

Table 2-2 Signal description of USB Port 0 Interface

Pin Name	Ball#	Type	Dir.	Description
XSCI	B43	ANA	I	Crystal oscillator input 12MHz
XSCO	A53	ANA	O	Crystal oscillator output 12MHz
U2DP0	A55	DIFF	IO	USB2.0 differential data (+).
U2DM0	A56	DIFF	IO	USB2.0 differential data (-).
UREF0	A57	ANA	O	Connect an external resistor (12kΩ ± 1%) to AGND33
UCAP0	B47	ANA	O	Connect an external capacitor 2nF to PGND
UV1280	A58	ANA	O	Connect an external capacitor 3.3uF to AGND33
SSTXP0	B48	DIFF	O	USB3.0 SuperSpeed differential output (+)
SSTXM0	B49	DIFF	O	USB3.0 SuperSpeed differential output (-)
SSRXP0	B50	DIFF	I	USB3.0 SuperSpeed differential input (+)
SSRXM0	B51	DIFF	I	USB3.0 SuperSpeed differential input (-)
PPWR0	A50	LVTTL	O	Vbus port power control (optional)
OVCN0	B39	LVTTL	I	Indicate over current occurs on VBus, active low (optional)

2.2.3 USB Port 1 Interface

Table 2-3 Signal description of USB Port 1 Interface

Pin Name	Ball#	Type	Dir.	Description
U2DP1	B2	DIFF	IO	USB2.0 differential data (+).
U2DM1	B3	DIFF	IO	USB2.0 differential data (-).

UREF1	B4	ANA	O	Connect an external resistor (12kΩ ± 1%) to AGND33
UCAP1	A6	ANA	O	Connect an external capacitor 2nF to PGND
UV1281	B5	ANA	O	Connect an external capacitor 3.3uF to AGND33
SSTXP1	A7	DIFF	O	USB3.0 SuperSpeed differential output (+)
SSTXM1	A8	DIFF	O	USB3.0 SuperSpeed differential output (-)
SSRXP1	A9	DIFF	I	USB3.0 SuperSpeed differential input (+)
SSRXM1	A10	DIFF	I	USB3.0 SuperSpeed differential input (-)
PPWR1	A48	LVTTL	O	Vbus port power control (optional)
OVCN1	A46	LVTTL	I	Indicate over current occurs on VBus, active low (optional)

2.2.4 Miscellaneous Signals

Table 2-4 Signal description of miscellaneous signals

Pin Name	Ball#	Type	Dir.	Description
SMIN	B28	LVTTL	O	SMI interrupt output pin, active low
ROMSDA	B27	LVTTL	IO	External EEPROM interface. I2C data (optional)
ROMSCL	A35	LVTTL	O	External EEPROM interface. I2C clock (optional)
ROMPRES	A33	LVTTL	I	External EEPROM interface. ROM present. (optional)
U2LNKN	B22	LVTTL	O	Status indicator: USB2 link-up, active low
PCIELNKN	B21	LVTTL	O	Status indicator: PCIe link-up, active low
SSLNKN	A27	LVTTL	O	Status indicator: USB3 link-up, active low
DATTXN	A28	LVTTL	O	Status indicator: USB3 transmission, active low
DATRXN	B24	LVTTL	O	Status indicator: USB3 receiving, active low
PPWRCTL	B34	LVTTL	I	VBus controllable, internal pull down 0: VBus is NOT controlled by FL1009 1: VBus is controlled by FL1009 (connect to DVCC33X)
AUXDET	A39	LVTTL	I	AUX power detection, internal pull down Connect a 4.7K resistor to DVCC33X to support remote wake-up from D3cold.
TESTN	B37	LVTTL	I	Test mode enable, active low Connect a 4.7K resistor to DVCC33X for normal function.

2.2.5 Power / Ground

Table 2-5 Signal description of power / ground signals

Pin Name	Ball#	Aux Domain	Description
AVCC33X	A4, B45	AUX	Analog 3.3V power
AGND33	A3, A59, B6, B44		Analog 3.3V ground
AVCC10X	A17, A22, A60, B7	AUX	Analog 1.05V power
AVCC10	B14		Analog 1.05V power
AGND10	A19, A61, A62, B8, B9, B20		Analog 1.05V ground
PVCC33X	A12	AUX	PLL 3.3V power
PVCC25X	A5, A21, B46	AUX	PLL 2.5V power
PVCC25OX	B11	AUX	PLL 2.5V power **output** for connecting to PVCC25X
PGND	A1, A20, A54, B10		PLL ground
DVCC33X	A44, B12, B38	AUX	Digital 3.3V power
DVCC10X	A11, A13, B40, B42, B52	AUX	Digital 1.05V power
DVCC33	A26, B30, B25		Digital 3.3V power
DVCC10	A16, A25, A36, A41, A42, B23, B26, B32		Digital 1.05V power
DGND	Exposed Pad		Digital ground

2.2.6 NC Pins

Table 2-6 No connection pin list

NC Pin Ball#
A2, A29, A30, A31, A32, A34, A37, A38, A40, A43, A45, A47, A49, A51, A52, A63, A64, B1, B29, B31, B33, B35, B36, B41

3. Function Description

3.1 Block Diagram

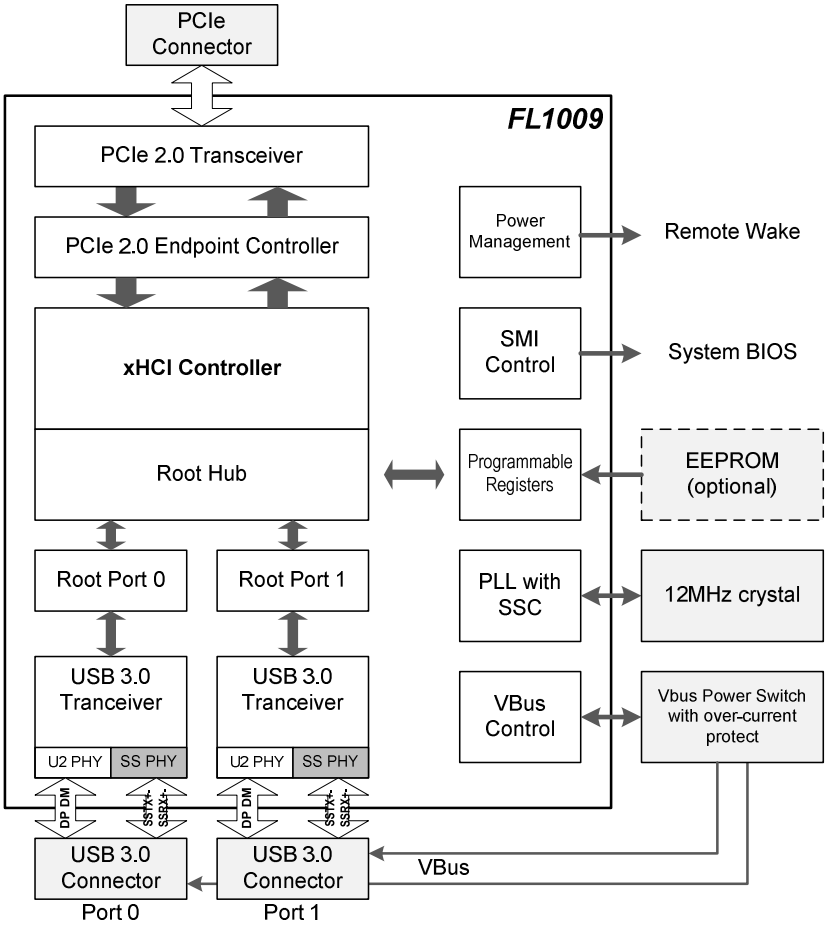


Figure 3 FL1009 block diagram

3.2 xHCI Controller

The FL1009 from Fresco Logic is a high-performance PCI Express-based xHCI host controller, which supports all required functions of the xHCI Specification Revision 1.0. The FL1009 controller is highly integrated and features Fresco Logic's patented GoXtream™ xHCI acceleration technology. Dedicated functional units provide full hardware acceleration of all xHCI functionality, guaranteeing the best possible performance while minimizing power.

The performance is enhanced by eliminating the inherent latencies and bottlenecks of hardware/software hand-offs. The power is reduced by eliminating the overhead of the additional processors, components and circuitry needed for software-based approaches. Additional benefits of this highly-integrated approach are lower total system cost and a simpler deployment and usage model.

The FL1009 is fully integrated with PCI Express and USB transceivers and supports both USB 3.0 and USB 2.0 devices. The FL1009 features a Gen 2, x1 PCI Express lane and two USB 3.0 downstream ports.

The FL1009 supports the full capabilities of traversing the Scatter/Gather list to complete the DMA functions called out by the xHCI Specification. The general interfaces described in the xHCI Specification include a Host Configuration Space, a Memory- mapped IO space and a Host memory space. Section 5.1.1.39 contains the details of these spaces within the FL1009 xHCI controller.

3.3 Root Hub and Root Ports

The FL1009 implements the Root Hub functionality described in the USB 3.0 Specification. FL1009 supports a dual port configuration.

The root port provides USB-specified link functionality for SuperSpeed, high-speed, full-speed and low-speed links. It communicates with the USB PHY to transfer the data onto the link. Each root port has buffers to support the bandwidth requirements of its link.

Additionally, each port has its own power management and link negotiation capabilities, allowing individual ports to power down separately. Link management is done in each of the root ports, which can be suspended or reset by software without affecting overall xHCI controller operation.

3.4 USB Transceiver

FL1009 integrates a dual-port 5Gbps SuperSpeed USB transceiver which is fully compliant with USB 3.0 specification and backward compatible with all USB 2.0 speed: High-speed, full-speed and low-speed. The transceiver is equipped with adaptive receiver equalization, which enhances the receiving capability from signal attenuation due to the channel or crosstalk noises. As to clock generation, the transceiver supports 12MHz external crystal, and provides the generation of Spread Spectrum Clocking (SSC), as required by the specification.

3.5 PCI Express Transceiver

FL1009 integrates a 5.0GT/s PCI Express transceiver which is fully compliant with the PCI Express Specifications Revision 2.0. It is capable of transmitting and receiving data at a rate of 5Gbps.

3.6 Power Management

3.6.1 USB Power States

FL1009 supports all power modes defined in USB 3.0 Specification. Table 3-1 addresses the USB 3.0 power modes.

Table 3-1 USB 3.0 Power State

Link State	Description	Characteristic	Exit Latency Range
U0	Link active	Link operational state	N/A
U1	Link idle – fast exit	RX and TX circuitry quiesced	us
U2	Link idle – slower exit	Clock generation circuitry may additionally be quiesced	us – ms
U3	Link suspend	Transceiver power is off	ms

FL1009 supports remote wake from USB device

3.6.2 PCIe Power States

FL1009 supports both PCI Power Management (PCIPM) and PCI Express Active State Power Management (ASPM). The ASPM may be initiated by FL1009 or by system software. FL1009 supports D0, D1, D3hot and D3cold states as well as ASPM L0s, L1 states.

4. Electrical Characteristics

4.1 Operating Conditions

Table 4-1 Recommended Operating Conditions

Symbol	Parameters	Min.	Typ.	Max.	Unit
DVCC10 DVCC10X	Digital core power supply	1.0	1.05	1.1	V
DVCC33 DVCC33X	Digital IO power supply	2.97	3.3	3.63	V
AVCC10 AVCC10X	Analog 1.0V power supply	1.0	1.05	1.1	V
AVCC33 AVCC33X PVCC33X	Analog 3.3V power supply	3.15	3.3	3.45	V
T_A	Operating ambient temperature	0		85	˚C
T_C	Operating case temperature ($T_C = T_A + \theta P$)	0		105	˚C

4.2 Absolute Maximum Ratings

Permanent damage of devices may occur if the absolute maximum ratings are exceeded. These are only stress ratings, and the functional operations should be restricted within the conditions detailed in Table 4-2. Exposure to the absolute maximum rating conditions may also affect the reliability of the devices. The input and output negative voltage ratings may be exceeded if the input and output currents are not exceeded.

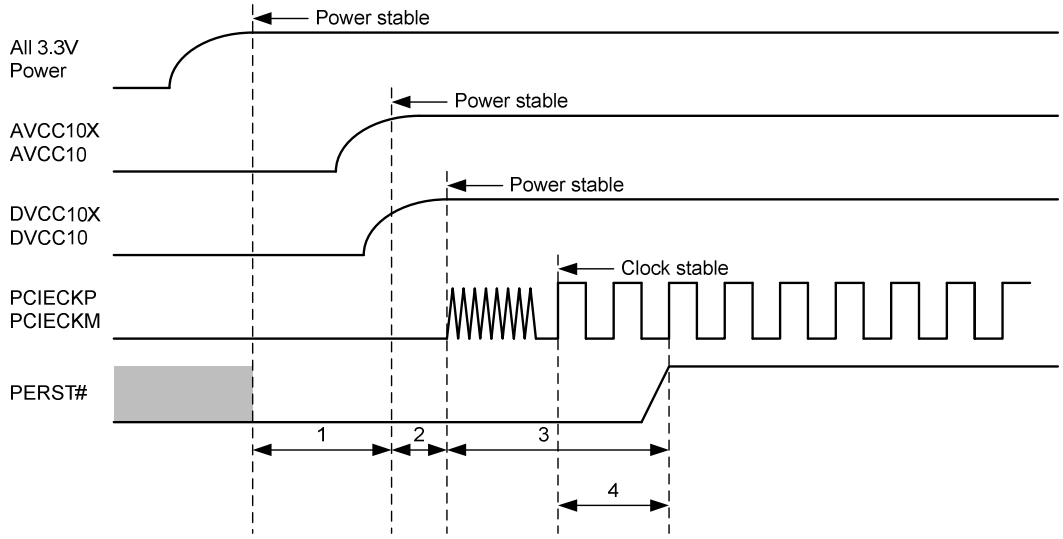
Table 4-2 Absolute Maximum Ratings

Symbol	Description	Rating	Unit
DVCC10 DVCC10X	Digital core power supply	-0.5 ~ 1.4	V
DVCC33 DVCC33X	Digital IO power supply	-0.5 ~ 4.6	V
AVCC10 AVCC10X	Analog 1.0V power supply	-0.5 ~ 1.4	V
AVCC33 AVCC33X PVCC33X	Analog 3.3V power supply	-0.5 ~ 4.6	V
V_{IN3}	Input voltage of LVTTL IOs	-0.5 ~ 4.6	V
I_{IN}	DC input current	50	mA
I_{OUT}	DC output short circuit current	50	mA
T_{STG}	Storage temperature	-65 ~ 150	℃

4.3 Power-up Sequence

FL1009 has 1.05V and 3.3V voltage supplies for analog and digital functionalities respectively and also has 2 resets: PERST# and internal power-on reset. Please follow below power-up sequence including power supplies, resets, and reference clocks.

1. Assert PERST#
2. All 3.3V including analog and digital supplies are stable
3. Analog 1.05V stable
4. Digital 1.05V stable. Digital 1.05V must not be earlier than Analog 1.05V.
5. PERST# de-assert after reference clock stable



1. All 3.3V (AVCC33X, AVCC33, DVCC33X, DVCC33, PVCC33X) stable to Analog 1.05V (AVCC10X, AVCC10) stable
2. Analog 1.05V stable to Digital 1.05V (DVCC10X, DVCC10) stable
3. Digital 1.05V stable to PERST# de-asserted
4. Reference clock (PCIECKP, PCIECKM) stable to PERST# de-asserted

Figure 4 Power-up sequence

Table 4-3 Power-up sequence parameters

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
T_{PON33_A10}	Time interval of 3.3V stable to analog 1.05V stable		1	-	-	ms
T_{PONA10_D10}	Time interval of analog 1.05V stable to digital 1.05V stable	Digital 1.05V must not be earlier than analog 1.05V.	0			ms
T_{POND10_PRST}	Time interval of digital 1.05V stable to PERST# de-asserted		100			ms
T_{PONCK_PRST}	Time interval of PCIe reference clock stable to PERST# de-asserted		100			us

4.4 Power-down Sequence

Figure 5 illustrates the power-down sequence requirement of FL1009. Please follow below power-down sequence including power supplies, resets, and reference clocks.

1. Assert PERST#
2. Remove 3.3V supply after PERST# is asserted.
3. Remove PCIe reference clock after PERST# is asserted
4. Remove 1.05V supply no sooner than 3.3V supply is removed.

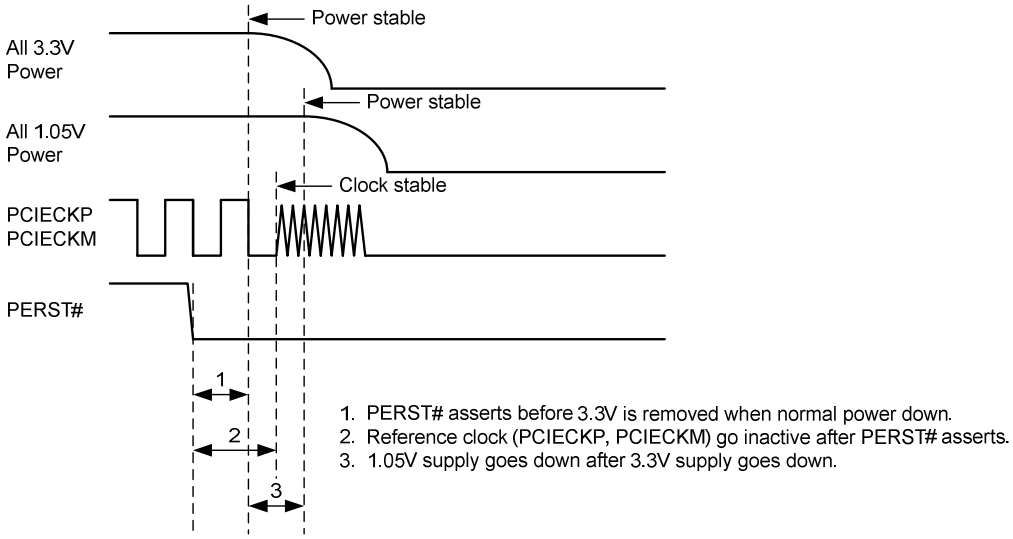


Figure 5 Power-down Sequence

Table 4-4 Power-down sequence parameters

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
T_{PDN33_10}	Time interval of removing 3.3V to removing 1.05V supply.	1.05V must not be removed earlier than 3.3V supply removed.	0			ms

4.5 DC Electrical Specifications

The section defines the electrical specifications of digital signal pins which are defined as LVTTL in Chapter 2.

Table 4-5 LVTTL I/O DC Characteristic

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage	3.3V LVTTL			0.8	V
V_{IH}	Input high voltage	3.3V LVTTL	2.0			V
V_{OL}	Output low voltage	3.3V LVTTL			0.4	V
V_{OH}	Output high voltage	3.3V LVTTL	2.4			V
R_{PU}	Internal pull-up resistor		40	75	190	KΩ
R_{PD}	Internal pull-down resistor		40	75	190	KΩ
C_{IN}	Input capacitance			2.1		pF

4.6 Power Consumption

Table 4-6 FL1009 maximum power consumption

Symbol	Condition	Power	Unit
P_{IDLE}	No device connected	95	mW
$P_{USB2-1P}$	One USB 2.0 device connected	350	mW
$P_{USB3-1P}$	One USB 3.0 device connected	450	mW
$P_{USB2-2P}$	Two USB 2.0 devices connected	450	mW
$P_{USB3-2P}$	Two USB 3.0 devices connected	750	mW
P_{SLEEP}	Host controller sleep with remote wake-up support	40	mW

Table 4-7 FL1009 operating current (measured under typical process corner)

Symbol	Condition	Current of each power lines								Total Current	Unit
		AVCC33X	PVCC33X	DVCC33X	DVCC33	AVCC10X	AVCC10	DVCC10X	DVCC10		
P_{IDLE}	No device connected	0	1	0	1	10	10	1	15	38	mA
$P_{USB2-1P}$	One USB 2.0 device connected	18	44	0	5	10	33	14	82	206	mA
$P_{USB3-1P}$	One USB 3.0 device connected	2	60	0	5	91	33	14	85	290	mA
$P_{USB2-2P}$	Two USB 2.0 devices connected	36	44	0	5	11	33	24	83	236	mA
$P_{USB3-2P}$	Two USB 3.0 devices connected	4	75	0	5	170	33	24	91	402	mA
P_{SLEEP}	Host controller sleep with remote wake-up support	0	1	0	1	8	0	2	0	12	mA

4.7 AC Characteristics

The section defines the requirement of reference clock source and the power supplies.

Table 4-8 Reference clock specification

Symbol	Description	Condition	Min.	Type	Max.	Unit
F_{XTAL_12}	Frequency of 12MHz crystal		-30ppm	12	+30ppm	MHz
T_{DUTY}	Clock duty cycle		40	50	60	%
ESR	Crystal ESR		2.4		40	Ω

Table 4-9 Power noise specification

Symbol	Description	Condition	Min.	Type	Max.	Unit
$V_{NOISE33}$	Power noise on 3.3V supply	1 Hz ~ 100KHz			100	mVpp
$V_{NOISE10}$	Power noise on 1.0V supply	1 Hz ~ 100KHz			50	mVpp

4.8 USB Electrical Characteristics

Table 4-10 Electrical characteristic of SuperSpeed transmitter

Symbol	Description	Condition	Min.	Type	Max.	Unit
UI	Unit Interval		199.94	200.00	200.06	ps
$V_{TX-DIFF-PP}$	Differential peak-to-peak TX voltage swing	2 * $\|V_{TXP} - V_{TXN}\|$, measured at TX near-end	800		1200	mV
$V_{TX-DIFF-PP\_LOW}$	Low-power differential peak-to-peak TX voltage swing	2 * $\|V_{TXP} - V_{TXN}\|$, measured at TX near-end	400		1200	mV
$V_{TX-DE-RATIO}$	TX de-emphasis level		3.0		4.0	dB
$R_{TX-DIFF-DC}$	DC differential impedance		72		120	Ω
$C_{AC-COUPLING}$	AC coupling capacitor		75		200	nF
T_{TX-EYE}	Transmitter eye	Including all jitter sources, measured at the silicon pad.	0.625			UI
$T_{TX-DJ-NEAR}$	Near-end TX deterministic jitter	Deterministic jitter only assuming the Dual Dirac distribution, measured at the silicon pad by using the CP0 pattern.			0.205	UI
$T_{TX-DJ-FAR}$	Far-end TX deterministic jitter	Deterministic jitter only assuming the Dual Dirac distribution, measured at TP1			0.43	UI
$T_{TX-RJ-FAR}$	Far-end TX random jitter	Measured at the silicon pad by using the CP1 pattern at 10^{-12}BER			0.23	UI
$T_{TX-TJ-FAR}$	Far-end TX total jitter	Measured at the silicon pad (TJ = DJ + RJ)	-	-	0.66	UI
$C_{TX-PARASITIC}$	TX input capacitance for return loss	-	-	-	1.25	pF
R_{TX-DC}	Transmitter DC common-mode impedance	-	18	-	30	Ω
$V_{TX-DC-CM}$	TX DC common-mode voltage	-	-	0.75	1.2	V
$V_{TX-DC-CM-U0-U1}$	Absolute TX DC common-mode voltage between the U0 and U1 modes	-	-	0.75	1.2	V
V_{T-D-R}	The voltage change allowed during the receiver detection	The total amount of voltage change during TX-Detect-RX	-	-	200	mV

Table 4-11 Spread Spectrum Clocking (SSC) parameters

Symbol	Description	Condition	Min.	Type	Max.	Unit
$T_{SSC-MOD-RATE}$	Modulation rate	USB transceiver power	30	31.5	33	KHz
$T_{SSC-FREQ-DEVIATION}$	SSC deviation	USB PLL power	0	4000	5000	ppm
$T_{SSC-SLEW-RATE}$	SSC slew rate	USB transceiver power	-	-	10	ms/s

Table 4-12 Electrical characteristics of LFPS

Symbol	Description	Condition	Min.	Type	Max.	Unit

T_{Period}	Period of the LFPS signal	-	20	-	100	ns
$V_{CM-AC-LFPS}$	LFPS AC common-mode voltage	-	-	0.75	1.2	V
$V_{TX-DIFF-PP-LFPS}$	Differential peak-to-peak LFPS voltage swing	2 * $\|V_{TXP} – V_{TXN}\|$, measured at TX near-end	800	-	1200	mV
$V_{TX-DIFF-PP-LFPS-LP}$	Low-power differential peak-to-peak LFPS voltage swing	2 * $\|V_{TXP} – V_{TXN}\|$, measured at TX near-end	400	-	1200	mV
$T_{RISE-FALL-2080}$	Rise/Fall time of the LFPS signal	-	-	-	4	ns

Table 4-13 Electrical characteristics of SuperSpeed receiver

Symbol	Description	Condition	Min.	Type	Max.	Unit
UI	Unit interval	-	199.94	200.00	200.06	ps
R_{RX-DC}	Receiver common-mode impedance	-	18	-	30	Ω
$R_{RX-DIFF-DC}$	Receiver DC differential impedance	-	72	-	120	Ω
$V_{RX-LFPSDET-DIFF-PP}$	LFPS detect threshold	-	100	-	300	mV
$V_{RX-DIFF-PP-POSTEQ}$	Differential RX peak-to-peak voltage	-	30	-	-	mV
T_{RX-TJ}	Max RX inherent timing error	-	-	-	0.45	UI
T_{RX-DJ}	Max RX inherent deterministic timing error	-	-	-	0.285	UI
$C_{RX-PARASITIC}$	RX input capacitance for return loss	-	-	-	1.1	pF
$V_{RX-AC-CM}$	RX AC common-mode voltage	-	-	-	150	mV
$V_{RX-AC-CM-U0-U1}$	RX AC common-mode voltage during the U0-to-U1 transition	-	-	-	200	mV

Table 4-14 Electrical characteristic of USB 2.0 High-speed

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Driver characteristic						
$T_{HSRDRATE}$	High-speed TX data rate	-	479.76	-	480.24	Mbps
$T_{HSRDRATE}$	High-speed RX data rate	-	479.76	-	480.24	Mbps
t_{HSR}	High-speed differential rise time	-	500	-	-	ps
t_{HSF}	High-speed differential fall time	-	500	-	-	ps
Input level of differential receiver						
V_{HSDIFF}	High-speed differential input sensitivity	$\|V_{I(DP)} – V_{I(DM)}\|$, measured at the connection of an application circuit.	300	-	-	mV
V_{HSCM}	High-speed data signaling common-mode voltage range	-	–50	-	500	mV
V_{HSDSC}	High-speed disconnection detection threshold	Disconnection detected	625	-	-	mV
		No disconnection detected	-	-	525	mV

Output Level						
V_{HSOI}	High-speed idle level output voltage (Differential)	-	-10	-	10	mV
V_{HSOL}	High-speed low level output voltage (Differential)	-	-10	-	10	mV
V_{HSOH}	High-speed high level output voltage (Differential)	-	360	400	440	mV
V_{CHIRPJ}	Chirp-J output voltage (Differential)	-	700	-	1100	mV
V_{CHIRPK}	Chirp-K output voltage (Differential)	-	-900	-	-500	mV
$I_{DP/DM}$	Allowable output current of DP/DM	The termination is 45 Ω ±10%.	14.55	17.78	21.79	mA
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used for the internal chip	40.5	45	49.5	Ω
Z_{HSTERM}	Differential impedance	-	76.5	90	103.5	Ω

Table 4-15 Electrical characteristic of USB 2.0 full-speed/low-speed

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Full-speed driver characteristic						
$T_{FSDRATE}$	Full-speed TX data rate	-	11.994	-	12.006	Mbps
$T_{FSRDRATE}$	Full-speed RX data rate	-	11.97	-	12.03	Mbps
t_{FR}	Rise time	CL = 50 pF 10% ~ 90% of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FF}	Fall time	CL = 50 pF 90% ~ 10% of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FRMA}	Differential rise/fall time matching (t_{FR}/t_{FF})	Excluding the first transition from the idle mode	90	-	110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from the idle mode	1.3	-	2.0	V
Low-speed driver characteristic						
$T_{LSDRATE}$	Low-speed TX data rate	-	1.49925	-	1.50075	Mbps
$T_{LSRDRATE}$	Low-speed RX data rate	-	1.49625	-	1.50375	Mbps
t_{LR}	Rise time	CL = 200 pF ~ 600 pF 10% ~ 90% of |VOH – VOL|	75	-	300	ns
t_{LF}	Fall time	CL = 200 pF ~ 600 pF 90% ~ 10% of $\|V_{OH} - V_{OL}\|$	75	-	300	ns
t_{LRMA}	Differential rise/fall time matching (t_{LR}/t_{LF})	Excluding the first transition from the idle mode	80	-	125	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from the idle mode	1.3	-	2.0	V
Input level of differential receiver						
V_{DI}	Differential input sensitivity	$\|V_{I(DP)} - V_{I(DM)}\|$	0.2	-	-	V
V_{CM}	Differential common-mode voltage	-	0.8	-	2.5	V
ZHSDRV	Driver output resistance	Equivalent resistance used for the internal chip	40.5	45	49.5	Ω
RPU1	Pull-up resistor during idle	Equivalent resistance used for the	900	-	1575	Ω

		internal chip				
RPU2	Driver output resistance	Equivalent resistance used for the internal chip	525	-	1515	Ω
RPD	Driver output resistance	Equivalent resistance used for the internal chip	14.25	-	24.8	kΩ
Input level of single-ended receiver						
V_{SE}	Single-ended receiver threshold	-	0.8	-	2.0	V
Output level						
V_{OL}	Low-level output voltage	-	0	-	0.3	V
V_{OH}	High-level output voltage	-	2.8	-	3.6	V

4.9 PCIe Electrical Characteristics

Table 4-16 Electrical characteristic of PCIe

Symbol	Description	Condition	Min.	Type	Max.	Unit
Input level						
$V_{RX-DIFF}$	High speed differential input signals	$\|V_{RX(DIP)} - V_{RX(DIN)}\|$, measured at the connection of receiver's near end.	87.5	-	600	mV
T_{RX-EYE}	Receiver eye time opening	Minimum eye time at Rx pins to yield a 10E-12 BER	0.4	-	-	UI
V_{IDLE}	Electrical idle detect threshold	IDLE detected	-	-	87.5	mV
		Non IDLE detected	87.5	-		mV
$V_{RX-CM-AC}$	RX and AC common-mode voltage	Peak voltage	-	-	150	mV
Output levels						
$V_{TX-DIFF}$	High speed differential output signal	$\|V_{TX(DOP)} - V_{TX(DON)}\|$, measured at the connection of transmitter's near end.	400	-	600	mV
T_{TX-EYE}	Transmitter eye time opening	Minimum eye time at Rx pins to yield 10E-12 BER	0.75	-	-	UI
$V_{TX-IDLE-AC}$	Electrical idle differential peak output voltage	-	-	-	20	mV
V_{T-D-R}	The amount of voltage change allowed during receiver detection	The total amount of voltage change during TX-Detect-RX	-	-	600	mV
$V_{TX\_CM\_AC}$	Transmitter AC common-mode voltage	AC RMS value	-	-	20	mV
V_{TX_DEM}	TX de-emphasis level		-3	-	-4	dB
F_{BEACON}	Frequency of beacon signaling	-	2	-	150	MHz
Resistance						
R_{RX}	Built-in receiver input impedance	-	40	50	60	Ω
R_{TX}	Built-in driver output impedance	-	40	50	60	Ω
Capacitance						
C_{TX}	AC coupling capacitor	-	75	-	200	nF

5. PCI Express Registers

5.1 PCI Express Configuration Register Map

FL1009 xHCI controller is a PCI-based xHC (extended Host Controller) which is required to implement a PCI, Type 0 PCI device header as Table 5-1. FL1009 also implements two Base Address Registers (BAR 0 and BAR 1) to enable 64-bit addressing. These Base Address Registers are used to point to the start of the host controllers memory-mapped Input/Output (MMIO) register spaces, as described in section 5.1.1.39.

Table 5-1 PCIe Configuration Register Map

Registers (31 … 0)				Offset
Device ID		Vendor ID		000h
Status		Command		004h
Class Code			Revision ID	008h
BIST	Header type	Latency Timer	Cache Line Size	00Ch
Base Address Registers (BAR)				010h
				014h
				018h
				01Ch
				020h
				024h
Reserved				028h
Subsystem ID		Subsystem Vendor ID		02Ch
Reserved				030h
Reserved			Capabilities Pointer	034h
Reserved				038h
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	03Ch
Power Management Capability		Next Capability Pointer	PM Cap ID	40h
PM Data	PMCSR_BSE	Power Management Control/Status		44h
Reserved				48h
				4Ch
MSI Message Data		Next Capability Pointer	MSI Cap ID	50h
Reserved				5Ch
Reserved		FLADJ	SBRN	60h
Reserved				64h
				68h
				6Ch
PCI Express Capability Register		Next Capability Pointer	PCI Express Cap ID	70h
Device Capabilities				74h
Device Status		Device Control		78h
Link Capabilities				7Ch
Link Status		Link Control		80h

Reserved			84h … 90h
Device Capabilities 2			94h
Device Status 2	Device Control 2		98h
Link Capability 2			9Ch
Link Status 2	Link Control 2		A0h
Reserved			A4h A8h ACh
MSI-X Message Control	Next Item Pointer	MSI-X Cap ID	B0h
MSI-X Table Offset and BIR			B4h
MSI-X PBA Offset and BIR			B8h
Reserved			BCh …
EEPROM Control			F0h
Programmability Offset			F4h
Programmability Data			F8h
Reserved			FCh

5.1.1 PCI Express Configuration Register Description

5.1.1.1 Vendor ID Register

Address Offset:	00h	**Attribute:**	RO
Default value:	1B73h	**Size:**	16 bits

Bit	Description	Attribute
15:0	Vendor ID. A 16-bit value assigned to Fresco Logic Inc: 1B73h.	RO

5.1.1.2 Device ID Register

Address Offset:	02h	**Attribute:**	RO
Default value:	1009h	**Size:**	16 bits

Bit	Description	Attribute
15:0	Device ID. A 16-bit value assigned to FL1009: 1009h.	RO

5.1.1.3 Command Register

Address Offset:	04h	**Attribute:**	RW, RO
Default value:	0000h	**Size:**	16 bits

Bit	Description	Attribute
8	SERR# Enable	RW
6	Parity Error Response	RW
2	Bus Master Enable. Default value of this bit is 0b.	RO
Other bits	Reserved	RO

5.1.1.4 Status Register

Address Offset:	06h	**Attribute:**	RW1C, RO
Default value:	0000h	**Size:**	16 bits

Bit	Description	Attribute
15	Detected Parity Error	RW1C (Read, Write 1 to Clear)
14	Signaled System Error	RW1C
13	Received Master Abort	RW1C
12	Received Target Abort	RW1C
11	Signaled Target Abort	RW1C
8	Master Data Parity Error	RW1C
4	Capabilities List	RO
3	Interrupt Status	RO
Other bits	Reserved	RO

5.1.1.5 Revision ID Register

Address Offset:	08h	**Attribute:**	RO
Default value:	02h	**Size:**	8 bits

Bit	Description	Attribute
7:0	Silicon Revision. FL1009-2Q0 is read 02h	RO

5.1.1.6 Class Code Register

Address Offset:	09	**Attribute:**	RO
Default value:	0C 0330h	**Size:**	24 bits

Bit	Description	Attribute
23:16	Base Class Code (BASEC). 0Ch = Serial Bus controller.	RO
15:8	Sub-Class Code (SCC). 03h = Universal Serial Bus Host Controller.	RO
7:0	Programming Interface (PI). 30h = USB 3.0 Host Controller that conforms to this specification	RO

5.1.1.7 Cache Line Size Register

Address Offset:	0Ch	**Attribute:**	RW
Default value:	0h	**Size:**	8 bits

Bit	Description	Attribute
7:0	This field is implemented by PCI Express devices as a read-write field for legacy compatibility purposes but not applied to FL1009 functionalities.	RW

5.1.1.8 Latency Timer Register

Address Offset:	0Dh	**Attribute:**	RO
Default value:	0h	**Size:**	8 bits

Bit	Description	Attribute
7:0	Not applied on FL1009.	RO

5.1.1.9 Header Type Register

Address Offset:	0Eh	Attribute:	RO
Default value:	0h	Size:	8 bits

Bit	Description	Attribute
7:0	FL1009 supports type 0 PCI header.	RO

5.1.1.10 BIST

Address Offset:	0Fh	Attribute:	RO
Default value:	0h	Size:	8 bits

Bit	Description	Attribute
7:0	Not applied on FL1009	RO

5.1.1.11 Base Address Register 0

Address Offset:	10h	Attribute:	RO, RW
Default value:	0000 0004h	Size:	32 bits

Bit	Description	Attribute
31:4	Base address	RW
3	Prefetchable	RO
2:1	Memory Type. This field is read 10b to indicate the memory can be located anywhere in 64-bit space	RO
0	Memory space indicator	RO

5.1.1.12 Base Address Register 1

Address Offset:	14h	Attribute:	RW
Default value:	0000 0000h	Size:	32 bits

Bit	Description	Attribute
31:0	Base address of upper 32 bit of the 64 bit memory address.	RW

5.1.1.13 Base Address Register 2

Address Offset:	18h	Attribute:	RO, RW
Default value:	0000 0004h	Size:	32 bits

Bit	Description	Attribute
31:4	Base address	RW
3	Prefetchable	RO
2:1	Memory Type. This field is read 10b to indicate the memory can be located anywhere in 64-bit space	RO
0	Memory space indicator	RO

5.1.1.14 Base Address Register 3

Address Offset:	1Ch	**Attribute:**	RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:0	Base address of upper 32 bit of the 64 bit memory address.	RW

5.1.1.15 Base Address Register 4

Address Offset:	20h	**Attribute:**	RO, RW
Default value:	0000 0004h	**Size:**	32 bits

Bit	Description	Attribute
31:4	Base address	RW
3	Prefetchable	RO
2:1	Memory Type. This field is read 10b to indicate the memory can be located anywhere in 64-bit space	RO
0	Memory space indicator	RO

5.1.1.16 Base Address Register 5

Address Offset:	24h	**Attribute:**	RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:0	Base address of upper 32 bit of the 64 bit memory address.	RW

5.1.1.17 Subsystem Vendor ID (SVID)

Address Offset:	2Ch	**Attribute:**	RO
Default value:	1B73	**Size:**	16 bits

Bit	Description	Attribute
15:0	Defines the system manufacturer. This field should be chanced through programmability register.	RO

5.1.1.18 Subsystem ID (SSID)

Address Offset:	2Eh	**Attribute:**	RO
Default value:	0000	**Size:**	16 bits

Bit	Description	Attribute
15:0	System Manufacturer defined Device ID. This field should be chanced through programmability register.	RO

5.1.1.19 Capability Pointer

Address Offset:	34h	**Attribute:**	RO
Default value:	40h	**Size:**	16 bits

Bit	Description	Attribute

15:0	Offset Pointer to PCIe configuration header.	RO

5.1.1.20 Interrupt Line Register

Address Offset:	3Ch	**Attribute:**	RO
Default value:	00h	**Size:**	8 bits

Bit	Description	Attribute
7:0	Interrupt line from FL1009 to issue interrupt to system software.	RO

5.1.1.21 Interrupt Pin Register

Address Offset:	3Dh	**Attribute:**	RO
Default value:	01h	**Size:**	8 bits

Bit	Description	Attribute
7:0	This field is read 01 to indicate FL1009 uses INTA.	RO

5.1.1.22 Min_Gnt Register

Address Offset:	3Eh	**Attribute:**	RO
Default value:	00h	**Size:**	8 bits

Bit	Description	Attribute
7:0	Not applied on FL1009	RO

5.1.1.23 Max_Lat Register

Address Offset:	3Fh	**Attribute:**	RO
Default value:	0000h	**Size:**	8 bits

Bit	Description	Attribute
7:0	Not applied on FL1009	RO

5.1.1.24 PM Capability Identifier

Address Offset:	40h	**Attribute:**	RO
Default value:	01h	**Size:**	8 bits

Bit	Description	Attribute
7:0	Capability ID, this register is read 01h to identify this address is PCI Power Management registers	RO

5.1.1.25 Next Capability Pointer

Address Offset:	41h	**Attribute:**	RO
Default value:	50h	**Size:**	8 bits

Bit	Description	Attribute
7:0	Next Item Pointer Offset to point to the next MSI capability registers.	RO

5.1.1.26 Power Management Capability Register

Address Offset:	42h	Attribute:	RO
Default value:	DBC3h	Size:	16 bits

Bit	Description	Attribute
15:11	PME Support This field is read 11011b. FL1009 support D0, D1, D3hot and D3cold	RO
10	D2 Support This bit is read 0b to indicate FL1009 doesn't support D2 state	RO
9	D1 Support This bit is read 1b to indicate FL1009 support D1 state	RO
8:6	AUX current This field is read 111b. FL1009 required 375mA AUX current	RO
5	Device Specific Initialization (DSI)	RO
4	Reserved	RO
3	PME clock, tied 0 on PCIe device	RO
2:0	PM Version This field is read 011b to indicate FL1009 is compliant with PCI Power Management Interface Specification Revision 1.2	RO

5.1.1.27 Power Management Control/Status Register

Address Offset:	44h	Attribute:	RO, RWC, RW
Default value:	0000h	Size:	16 bits

Bit	Description	Attribute
15	PME_Status	RWC (Read, Write to clear)
14:13	Data_Scale, not supported by FL1009, read 00b	RO
12:9	Data_Select, not supported by FL1009, read 0000b	RO
8	PME# enable	RW
7:4	Reserved	RO
3	No_Soft_Reset	RO
2	Reserved	RO
1:0	PowerState 00b: D0 01b: D1 10b: D2 11b: D3hot	RW

5.1.1.28 SBRN (Serial Bus Release Number) Register

Address Offset:	60h	Attribute:	RO
Default value:	30h	Size:	8 bits

Bit	Description	Attribute
7:0	Serial Bus Specification Release Number 30h = Release 3.0, FL1009 is compliance to USB 3.0 specification	RO

	All other combinations are reserved	

5.1.1.29 FLADJ (Frame Length Adjustment) Register

Address Offset:	61h	**Attribute:**	RWS
Default value:	20h	**Size:**	8 bits

Bit	Description	Attribute
7:6	Reserved.	
5:0	Frame Length Timing Value. Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF microframe length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000 (125us). **Frame Length** **# HS bit times in decimal** / **FLADJ value decimal, (heximal)** 59488 / 0 (00h) 59504 / 1 (01h) 59520 / 2 (02h) … / … 59984 / 31 (1Fh) 60000 (125us) / 32 (20h) … / … 60480 / 62 (3Eh) 60496 / 63 (3Fh)	RO

5.1.1.30 PCI Express Capability ID

Address Offset:	70h	**Attribute:**	RO
Default value:	10h	**Size:**	8 bits

Bit	Description	Attribute
7:0	Return 10h to indicate this is a PCI Express Capability Structure	RO

5.1.1.31 Next Capability Pointer

Address Offset:	71h	**Attribute:**	RO
Default value:	B0h	**Size:**	8 bits

Bit	Description	Attribute
7:0	Next Item Pointer Offset to point to the next MSI-X capability registers.	RO

5.1.1.32 PCI Express Capability Register

Address Offset:	72h	**Attribute:**	RO
Default value:	0002h	**Size:**	16 bits

Bit	Description	Attribute

15:14	Reserved	
13:9	Interrupt Message Number	RO
8	Slot Implemented Not applicable on FL1009, return 0.	RO
7:4	Device/Port type FL1009 returns 0h to indicate a PCIe Express Endpoint	RO
3:0	Capability version. FL1009 returns 2h to indicate compliant to PCIe Base R2.1	RO

5.1.1.33 Device Capabilities Register

Address Offset:	74h	**Attribute:**	RO
Default value:	00288FC2h	**Size:**	32 bits

Bit	Description	Attribute
31:29	Reserved	RO
28	Function Level Reset Capability	RO
27:26	Captured Slot Power Limit Scale	RO
25:18	Captured Slot Power Limit Value	RO
17:16	Reserved	RO
15	Role-Based Error Reporting	RO
14:12	Reserved	RO
11:9	Endpoint L1 Acceptable Latency	RO
8:6	Endpoint L0s Acceptable Latency	RO
5	Extended Tag Field Supported	RO
4:3	Phantom Function Supported FL1009 returns 00b to advertise no function number bits are used for Phantom Functions	RO
2:0	Max Payload Size Supported FL1009 returns 010b to advertise 512 bytes max payload	RO

5.1.1.34 Device Control Register

Address Offset:	78h	**Attribute:**	RW, RO
Default value:	2810h	**Size:**	16 bits

Bit	Description	Attribute
15	Reserved	RO
14:12	Max Read Request Size	RW
11	Enable No Snoop	RW
10	AUX Power PM Enable	RW
9	Phantom Functions Enable	RW
8	Extended Tag Field Enable	RW
7:5	Max Payload Size	RW
4	Enable Relaxed Ordering	RW
3	Unsupported Request Reporting Enable	RW
2	Fatal Error Reporting Enable	RW
1	Non-Fatal Error Reporting Enable	RW

0	Correctable Error Reporting Enable	RW

5.1.1.35 Device Status Register

Address Offset:	7Ah	**Attribute:**	RO, RW1C
Default value:	0010h	**Size:**	16 bits

Bit	Description	Attribute
15:6	Reserved	RO
5	Transaction Pending	RO
4	AUX Power Detected	RO
3	Unsupported Request Detected	RW1C (Read, Write 1 to Clear)
2	Fatal Error Detected	RW1C
1	Non-Fatal Error Detected	RW1C
0	Correctable Error Detected	RW1C

5.1.1.36 Link Capabilities Register

Address Offset:	7Ch	**Attribute:**	RO
Default value:	0003 FC12h	**Size:**	32 bits

Bit	Description	Attribute
31:24	Port Number	RO
23:22	Reserved	RO
21	Link Bandwidth Notification Capability	RO
20	Data Link Layer Link Active Reporting Capable	RO
19	Surprise Down Error Reporting Capable	RO
18	Clock Power Management	RO
17:15	L1 Exit Latency L1 Exit Latency of FL1009 is more than 64us (111b)	RO
14:12	L0s Exit latency L0s Exit Latency of FL1009 is more than 4us (111b)	RO
11:10	ASPM Support FL1009 returns 11b to support ASPM L0s and L1	RO
9:4	Max Link Width FL1009 returns 000001b to indicate supporting of x1 link	RO
3:0	Supported Link Speeds FL1009 returns 0010b to indicate supporting of 5GT/s and 2.5GT/s	RO

5.1.1.37 Link Control Register

Address Offset:	80h	**Attribute:**	RW, RO
Default value:	0040h	**Size:**	16 bits

Bit	Description	Attribute
15:12	Reserved	RO
11	Link Autonomous Bandwidth Interrupt Enable	RW
10	Link Bandwidth Management Interrupt Enable	RW

9	Hardware Autonomous Width Disable	RW
8	Enable clock power management	RW
7	Extended Synch	RW
6	Common Clock Configuration	RW
5	Retrain Link	RW
4	Link Disable	RW
3	Read Completion Boundary (RCB)	RW
2	Reserved	
1:0	ASPM Control 00b: disable 01b: L0s enable 10b: L1 enable 11b: L0s and L1 enable	RW

5.1.1.38 Link Status Register

Address Offset:	82h	**Attribute:**	RO, RW1C
Default value:	1012h	**Size:**	16 bits

Bit	Description	Attribute
15	Link Autonomous Bandwidth Status	RW1C
14	Link Bandwidth Management Status	RW1C
13	Data Link Layer Link Active	RO
12	Set Clock Configuration	RO
11	Link Training	RO
10	Reserved	RO
9:4	Negotiated Link Width 000001b: x1	RO
3:0	Current Link Speed 0001: 2.5GT/s 0010: 5GT/s	RO

5.1.1.39 Device Capabilities 2 Register

Address Offset:	94h	**Attribute:**	RO
Default value:	0000 0010h	**Size:**	32 bits

Bit	Description	Attribute
31:24	Reserved	RO
23:22	Max End-End TLP Prefixes	RO
21	End-End TLP Prefix Supported	RO
20	Extended Fmt Field Supported	RO
13:12	TPH Completer Supported	RO
11	LTR Mechanism Supported	RO
10	No RO-enabled PR-PR Passing	RO
9	128-bit CAS Completer Supported	RO
8	64-bit AtomicOp Completer Supported	RO
7	32-bit AtomicOp Completer Supported	RO

6	AtomicOp Routing Supported	RO
5	ARI Forwarding Supported	RO
4	Completion Timeout Disable Supported	RO
3:0	Completion Timeout Ranges Supported	RO

5.1.1.40 Device Control 2 Register

Address Offset:	98h	**Attribute:**	RO
Default value:	0000h	**Size:**	16 bits

Bit	Description	Attribute
15	End-End TLK Prefix Blocking	RO
14:11	Reserved	RO
10	LTR Mechanism Enable	RO
9	IDO Completion Enable	RO
8	IDO Request Enable	RO
7	AtomicOp Egress Blocking	RO
6	AtomicOp Requester Enable	RO
5	ARI Forwarding Enable	RO
4	Completion Timeout Disable	RO
3:0	Completion Timeout Value	RO

5.1.1.41 Device Status 2 Register

Address Offset:	9Ah	**Attribute:**	RO
Default value:	0000h	**Size:**	16 bits

Bit	Description	Attribute
15:0	Reserved	RO

5.1.1.42 Link Capabilities 2 Register

Address Offset:	9Ch	**Attribute:**	RO
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:0	Reserved	RO

5.1.1.43 Link Control 2 Register

Address Offset:	A0h	**Attribute:**	RWS, RO
Default value:	0002h	**Size:**	16 bits

Bit	Description	Attribute
15:13	Reserved	RO
12	Compliance De-emphasis	RWS
11	Compliance SOS	RWS
10	Enter Modified Compliance	RWS
9:7	Transmit Margin	RWS
6	Selectable De-emphasis	RO

5	Hardware Autonomous Speed Disable	RWS
4	Enter Compliance	RWS
3:0	Target Link Speed This field is read 0010b to indicate FL1009 support 5.0GT/s Target Link Speed	RWS

5.1.1.44 Link Status 2 Register

Address Offset:	A2h	**Attribute:**	RO
Default value:	0001h	**Size:**	16 bits

Bit	Description	Attribute
15:1	Reserved	RO
0	Current De-emphasis Level 1b: -3.5 dB; 0b:-6 dB	RO

5.1.1.45 MSI-X Capability ID

Address Offset:	B0h	**Attribute:**	RO
Default value:	11h	**Size:**	8 bits

Bit	Description	Attribute
7:0	Return 11h to indicate this is a MSI-X Capability Structure	RO

5.1.1.46 Next Capability Pointer

Address Offset:	B1h	**Attribute:**	RO
Default value:	00h	**Size:**	8 bits

Bit	Description	Attribute
7:0	Next Item Pointer Return 00h for the final item in the list.	RO

5.1.1.47 MSI-X Message Control Register

Address Offset:	B2h	**Attribute:**	RW, RO
Default value:	0007h	**Size:**	16 bits

Bit	Description	Attribute
15	MSI-X Enable	RW
14	Function Mask	RW
13:11	Reserved	RO
10:0	MSI-X Table Size	RO

5.1.1.48 MSI-X Table Offset and BIR Register

Address Offset:	B4h	**Attribute:**	RO
Default value:	0000 0002h	**Size:**	32 bits

Bit	Description	Attribute
31:3	Table Offset	RO
2:0	Table BIR (Bar Indicator Register)	RO

5.1.1.49 MSI-X PBA Offset and BIR Register

Address Offset:	B8h	**Attribute:**	RO
Default value:	0000 0004h	**Size:**	32 bits

Bit	**Description**	**Attribute**
31:3	PBA (Pending Bit Array) Offset	RO
2:0	PBA BIR	RO

5.2 Memory-Mapped I/O Register Map

5.2.1 Host Controller Capability Registers

These registers specify the limits and capabilities of the FL1009 USB host controller implementation. All Capability Registers are Read-Only (RO). Please refer to section 5.3 of xHCI Specification Rev 1.0 for detail.

Table 5-2 Host controller capability registers

Register Symbol	Register Name	Base offset start	Base offset end	Default Value
CAPLENGTH	Capability Registers Length	00h	00h	80h
HCIVERSION	Host Controller Interface Version Number	02h	03h	0100h
HCSPARAMS1	Structural Parameters 1	04h	07h	0400081Fh
HCSPARAMS2	Structural Parameters 2	08h	0Bh	FC000054h
HCSPARAMS3	Structural Parameters 3	0Ch	0Fh	00040001h
HCCPARAMS	Capability Parameters	10h	13h	200073A1h
DBOFF	Doorbell Offset	14h	17h	00003000h
RTSOFF	Runtime Register Space Offset	18h	1Bh	00002000h

5.2.1.1 CAPLENGTH - Capability Registers Length

Address Offset:	0h	**Attribute:**	RO
Default value:	80h	**Size:**	8 bits

Bit	Description	Attribute
7:0	Capability Registers Length (CAPLENGTH)	RO

This register is modified and maintained by BIOS

5.2.1.2 HCIVERSION - Host Controller Interface Version Number

Address Offset:	02h	**Attribute:**	RO
Default value:	0100h	**Size:**	16 bits

Bit	Description	Attribute
15:0	Host Controller Interface Version Number (HCIVERSION) FL1009 is compliant with xHCI version 1.0	RO

This register is modified and maintained by BIOS

5.2.1.3 HCSPARAMS1 - Structural Parameters 1

Address Offset:	04h	**Attribute:**	RO
Default value:	0400 081Fh	**Size:**	32 bits

Bit	Description	Attribute
31:24	Number of ports (MaxPorts)	RO
23:19	Reserved	RO
18:8	Number of interrupters (MaxIntrs)	RO

7:0	Number of device slots (MaxSlots)	RO

This register is modified and maintained by BIOS

5.2.1.4 HCSPARAMS2 - Structural Parameters 2

Address Offset:	08h	**Attribute:**	RO
Default value:	FC00 0054h	**Size:**	32 bits

Bit	Description	Attribute
31:27	Max Scratchpad Buffers (MaxScratchpadBufs)	RO
26	Scratchpad Restore (SPR)	RO
25:8	Reserved	RO
7:4	Event Ring Segment Table Max (ERSTMax)	RO
3:0	Isochronous Scheduling Threshold (IST)	RO

This register is modified and maintained by BIOS

5.2.1.5 HCSPARAMS3 - Structural Parameters 3

Address Offset:	0Ch	**Attribute:**	RO
Default value:	0004 0001h	**Size:**	32 bits

Bit	Description	Attribute
31:16	U2 Device Exit Latency (U2DEL). Worst case latency to transition a root hub Port Link Stat (PLS) from U2 to U0. Applies to all root hub ports. FL1009 has default set as Less than 4us.	RO
15:8	Reserved	RO
7:0	U1 Device Exit Latency (U1DEL) Worst case latency to transition a root hub Port Link Stat (PLS) from U2 to U0. Applies to all root hub ports. FL1009 has default set as Less than 1us.	RO

This register is modified and maintained by BIOS

5.2.1.6 HCCPARAMS - Capability Parameters

Address Offset:	10h	**Attribute:**	RO
Default value:	2000 73A1h	**Size:**	32 bits

Bit	Description	Attribute
31:16	xHCI Extended Capabilities Pointer (xECP)	RO
15:12	Maximum Primary Stream Array Size (MaxPSASize)	RO
11:8	Reserved	RO
7	No Secondary SID Support (NSS)	RO
6	Latency Tolerance Messaging Capability (LTC)	RO
5	Light HC Reset Capability (LHRC)	RO
4	Port Indicators (PIND)	RO
3	Port Power Control (PPC)	RO

2	Context Size (CSZ)	RO
1	BW Negotiation Capability (BNC)	RO
0	64-bit Addressing Capability (AC64)	RO

This register is modified and maintained by BIOS

5.2.1.7 DBOFF - Doorbell Offset

Address Offset:	14h	**Attribute:**	RO
Default value:	0000 3000h	**Size:**	32 bits

Bit	Description	Attribute
31:2	Doorbell Array Offset (DBAO)	RO
1:0	Reserved	RO

5.2.1.8 RTSOFF - Runtime Register Space Offset

Address Offset:	18	**Attribute:**	RO
Default value:	0000 2000h	**Size:**	32 bits

Bit	Description	Attribute
31:5	Runtime Register Space Offset (RTRSO)	RO
4:0	Reserved	RO

5.2.2 Host Controller Operational Registers

This section defines the xHCI Operational Registers. All registers are multiples of 32 bits in length. Unless otherwise stated, all registers should be accessed as a 32-bit width on reads with an appropriate software mask, if needed. A software read/modify/write mechanism should be invoked for partial writes. Please refer to section 5.4 of xHCI Specification Rev 1.0 for detail.

Table 5-3 Host controller operational registers

Register Symbol	Register Name	Base offset start	Base offset end	Default Value
USBCMD	USB Command	80h	83h	00000000h
USBSTS	USB Status	84h	87h	00000001h
PAGESIZE	Page Size	88h	8Bh	00000001h
DNCTRL	Device Notification Control	94h	97h	00000000h
CRCR_LO	Command Ring Low	98h	9Bh	00000000h
CRCR_HI	Command Ring High	9Ch	9Fh	00000000h
DCBAAP_LO	Device Context Base Address Array Pointer Low	B0h	B3h	00000000h
DCBAAP_HI	Device Context Base Address Array Pointer High	B4h	B7h	00000000h
CONFIG	Configure	B8h	BBh	00000000h
PORTSC1USB2	Port 1 Status and Control USB2	480h	483h	000002A0h
PORTPMSC1USB2	Port 1 Power Management Status and Control USB2	484h	487h	00000000h
PORTSC2USB2	Port 2 Status and Control USB2	490h	493h	000002A0h
PORTPMSC2USB2	Port 2 Power Management Status and Control USB2	494h	497h	00000000h
PORTSC1USB3	Port 1 Status and Control USB3	4A0h	4A3h	000002A0h
PORTPMSC1	Port 1 Power Management Status and Control	4A4h	4A7h	00000000h
PORTLI1	Port 1 Link Info	4ACh	4AFh	00000000h
PORTSC2USB3	Port 2 Status and Control USB3	4B0h	4B3h	000002A0h
PORTPMSC2	Port 2 Power Management Status and Control	4B4h	4B7h	00000000h
PORTLI2	Port 2 Link Info	4BCh	4BFh	00000000h

5.2.2.1 USBCMD - USB Command

Address Offset:	80h	**Attribute:**	RW, RO
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:12	Reserved	RO
11	Enable U3 MFINDEX Stop (EU3S)	RW
10	Enable Wrap Event (EWE)	RW
9	Controller Restore State (CRS)	RW
8	Controller Save State (CSS)	RW
7	Light Host Controller Reset (LHCRST)	RW
6:4	Reserved	RO

3	Host System Error Enable (HSEE)	RW
2	Interrupter Enable (INTE)	RW
1	Host Controller Reset (HCRST)	RW
0	Run/Stop (RS)	RW

5.2.2.2 USBSTS - USB Status

Address Offset:	84h	**Attribute:**	RO, RW1C
Default value:	0000 0001h	**Size:**	32 bits

Bit	Description	Attribute
31:13	Reserved	RO
12	Host Controller Error (HCE) This bit is not preset in HC, this is deviation from xHCI 1.0 spec.	RO
11	Controller Not Ready (CNR) This is deviation from xHCI 1.0 spec.	RO
10	Save/Restore Error (SRE)	RW1C
9	Restore State Status (RSS)	RO
8	Save State Status (SSS)	RO
7:5	Reserved	RO
4	Port Change Detect (PCD)	RW1C
3	Event Interrupt (EINT)	RW1C
2	Host System Error (HSE)	RW1C
1	Reserved	RO
0	HCHalted (HCH)	RO

5.2.2.3 PAGESIZE - Page Size

Address Offset:	88h	**Attribute:**	RO
Default value:	0000 0001h	**Size:**	32 bits

Bit	Description	Attribute
31:16	Reserved	RO
15:0	Page Size (PAGESIZE)	RO

5.2.2.4 DNCTRL - Device Notification Control

Address Offset:	94h	**Attribute:**	RO, RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:16	Reserved	RO
15:0	Notification Enable (N0_N15)	RW

5.2.2.5 CRCR_LO - Command Ring Low

Address Offset:	98h	**Attribute:**	RO, RW, RW1S
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute

31:6	Command Ring Pointer (CRP)	RW
5:4	Reserved	RO
3	Command Ring Running (CRR)	RO
2	Command Abort (CA)	RW1S
1	Command Stop (CS)	RW1S
0	Ring Cycle State (RCS)	RW

5.2.2.6 CRCR_HI - Command Ring High

Address Offset:	9Ch	**Attribute:**	RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:0	Command Ring Pointer (CRP)	RW

5.2.2.7 DCBAAP_LO - Device Context Base Address Array Pointer Low

Address Offset:	B0h	**Attribute:**	RO, RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:6	Device Context Base Address Array Pointer (DCBAAP)	RW
5:0	Reserved	RO

5.2.2.8 DCBAAP_HI - Device Context Base Address Array Pointer High

Address Offset:	B4h	**Attribute:**	RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:0	Device Context Base Address Array Pointer (DCBAAP)	RW

5.2.2.9 CONFIG – Configure

Address Offset:	B8h	**Attribute:**	RO, RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:8	Reserved	RO
7:0	Max Device Slots Enabled (MaxSlotsEn)	RW

5.2.2.10 PORTSC1USB2 - Port 1 Status and Control USB2

Address Offset:	480h	**Attribute:**	RO, RW, RWS, RW1S, RW1CS, ROS,
Default value:	0000 02A0h	**Size:**	32 bits

Bit	Description	Attribute
31	Warm Port Reset (WPR)	RW1S
30	Device Removable (DR)	RO
29:28	Reserved	RO

27	Wake on Over-current Enable (WOE)	RWS
26	Wake on Disconnect Enable (WDE)	RWS
25	Wake on Connect Enable (WCE)	RWS
24	Cold Attach Status (CAS)	RO
23	Port Config Error Change (CEC)	RW1CS
22	Port Link State Change (PLC)	RW1CS
21	Port Reset Change (PRC)	RW1CS
20	Over-current Change (OCC)	RW1CS
19	Warm Port Reset Change (WRC)	RW1CS
18	Port Enabled Disabled Change (PEC)	RW1CS
17	Connect Status Change (CSC)	RW1CS
16	Port Link State Write Strobe (LWS)	RW
15:14	Port Indicator Control (PIC)	RWS
13:10	Port Speed (Port_Speed) This field identifies the speed of the attached USB Device. This field is only relevant if a device is attached (CCS = '1') in all other cases this field shall indicate Undefined Speed. 1: Full-speed 2: Low-speed 3: High-speed 3: SuperSpeed	ROS
9	Port Power (PP)	RWS
8:5	Port Link State (PLS) Read Value Meaning 0: Link is in the U0 State 1: Link is in the U1 State 2: Link is in the U2 State 3: Link is in the U3 State (Device Suspend) 4: Link is in the Disabled State 5: Link is in the RxDetect State 6: Link is in the Inactive State 7: Link is in the Polling State 8: Link is in the Recovery State 9: Link is in the Hot Reset State 10: Link is in the Compliance Mode State 11: Link is in the Test Mode State 12:14 Reserved 15 Link is in the Resume State	RWS
4	Port Reset (PR) 1: Port Reset signaling is asserted. 0: Port is not in Reset. When software writes a '1' to this bit (from a '0') the bus reset sequence is initiated	RW1S
3	Over-current Active (OCA) This port currently has an over-current condition. '0' = This port does not have an over-current condition. This bit shall automatically transition from a '1' to a '0' when the over-current condition is removed.	ROS
2	Reserved	RO

1	Port Enabled/Disabled (PED) Ports may only be enabled by the xHC. Software cannot enable a port by writing a '1' to this flag. A port may be disabled by software writing a '1' to this flag.	RW1CS
0	Current Connect Status (CCS) 1: Device is present on port. 0: No device is present.	ROS

5.2.2.11 PORTPMSC1USB2 - Port 1 Power Management Status and Control USB2

Address Offset:	484h	**Attribute:**	RO, RWS, ROS
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:28	Port Test Control (PTC)	RWS
27:17	Reserved	RO
16	Hardware LPM Enable (HLE)	RO
15:8	L1 Device Slot (L1DS)	RWS
7:4	Host Initiated Resume Duration (HIRD)	RWS
3	Remote Wake Enable (RWE)	RWS
2:0	L1 Status (L1S)	ROS

5.2.2.12 PORTSC2USB2 - Port 2 Status and Control USB2

Address Offset:	490h	**Attribute:**	RO, RW, RWS, RW1S, RW1CS, ROS,
Default value:	0000 02A0h	**Size:**	32 bits

Bit	Description	Attribute
31	Warm Port Reset (WPR)	RW1S
30	Device Removable (DR)	RO
29:28	Reserved	RO
27	Wake on Over-current Enable (WOE)	RWS
26	Wake on Disconnect Enable (WDE)	RWS
25	Wake on Connect Enable (WCE)	RWS
24	Cold Attach Status (CAS)	RO
23	Port Config Error Change (CEC)	RW1CS
22	Port Link State Change (PLC)	RW1CS
21	Port Reset Change (PRC)	RW1CS
20	Over-current Change (OCC)	RW1CS
19	Warm Port Reset Change (WRC)	RW1CS
18	Port Enabled Disabled Change (PEC)	RW1CS
17	Connect Status Change (CSC)	RW1CS
16	Port Link State Write Strobe (LWS)	RW
15:14	Port Indicator Control (PIC)	RWS
13:10	Port Speed (Port_Speed) This field identifies the speed of the attached USB Device. This field is only relevant if a device is attached (CCS = '1') in all other cases this field shall indicate Undefined Speed.	ROS

	1: Full-speed 2: Low-speed 3: High-speed 3: SuperSpeed	
9	Port Power (PP)	RWS
8:5	Port Link State (PLS) Read Value Meaning 0: Link is in the U0 State 1: Link is in the U1 State 2: Link is in the U2 State 3: Link is in the U3 State (Device Suspend) 4: Link is in the Disabled State 5: Link is in the RxDetect State 6: Link is in the Inactive State 7: Link is in the Polling State 8: Link is in the Recovery State 9: Link is in the Hot Reset State 10: Link is in the Compliance Mode State 11: Link is in the Test Mode State 12:14 Reserved 15 Link is in the Resume State	RWS
4	Port Reset (PR) 1: Port Reset signaling is asserted. 0: Port is not in Reset. When software writes a '1' to this bit (from a '0') the bus reset sequence is initiated	RW1S
3	Over-current Active (OCA) This port currently has an over-current condition. '0' = This port does not have an over-current condition. This bit shall automatically transition from a '1' to a '0' when the over-current condition is removed.	ROS
2	Reserved	RO
1	Port Enabled/Disabled (PED) Ports may only be enabled by the xHC. Software cannot enable a port by writing a '1' to this flag. A port may be disabled by software writing a '1' to this flag.	RW1CS
0	Current Connect Status (CCS) 1: Device is present on port. 0: No device is present.	ROS

5.2.2.13 PORTPMSC2USB2 - Port 2 Power Management Status and Control USB2

Address Offset:	494h	**Attribute:**	RO, RWS, ROS
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:28	Port Test Control (PTC)	RWS
27:17	Reserved	RO
16	Hardware LPM Enable (HLE)	RO
15:8	L1 Device Slot (L1DS)	RWS
7:4	Host Initiated Resume Duration (HIRD)	RWS

3	Remote Wake Enable (RWE)	RWS
2:0	L1 Status (L1S)	ROS

5.2.2.14 PORTSC1USB3 - Port 1 Status and Control USB3

Address Offset:	4A0h	**Attribute:**	RO, RWS, RW, RW1S, RW1CS, ROS
Default value:	0000 02A0h	**Size:**	32 bits

Bit	Description	Attribute
31	Warm Port Reset (WPR)	RW1S
30	Device Removable (DR)	RO
29:28	Reserved	RO
27	Wake on Over-current Enable (WOE)	RWS
26	Wake on Disconnect Enable (WDE)	RWS
25	Wake on Connect Enable (WCE)	RWS
24	Cold Attach Status (CAS)	RO
23	Port Config Error Change (CEC)	RW1CS
22	Port Link State Change (PLC)	RW1CS
21	Port Reset Change (PRC)	RW1CS
20	Over-current Change (OCC)	RW1CS
19	Warm Port Reset Change (WRC)	RW1CS
18	Port Enabled Disabled Change (PEC)	RW1CS
17	Connect Status Change (CSC)	RW1CS
16	Port Link State Write Strobe (LWS)	RW
15:14	Port Indicator Control (PIC)	RWS
13:10	Port Speed (Port_Speed) This field identifies the speed of the attached USB Device. This field is only relevant if a device is attached (CCS = '1') in all other cases this field shall indicate Undefined Speed. 1: Full-speed 2: Low-speed 3: High-speed 3: SuperSpeed	ROS
9	Port Power (PP)	RWS
8:5	Port Link State (PLS) Read Value Meaning 0: Link is in the U0 State 1: Link is in the U1 State 2: Link is in the U2 State 3: Link is in the U3 State (Device Suspend) 4: Link is in the Disabled State 5: Link is in the RxDetect State 6: Link is in the Inactive State 7: Link is in the Polling State 8: Link is in the Recovery State 9: Link is in the Hot Reset State	RWS

	10: Link is in the Compliance Mode State 11: Link is in the Test Mode State 12:14 Reserved 15 Link is in the Resume State	
4	Port Reset (PR) 1: Port Reset signaling is asserted. 0: Port is not in Reset. When software writes a '1' to this bit (from a '0') the bus reset sequence is initiated	RW1S
3	Over-current Active (OCA) This port currently has an over-current condition. '0' = This port does not have an over-current condition. This bit shall automatically transition from a '1' to a '0' when the over-current condition is removed.	ROS
2	Reserved	RO
1	Port Enabled/Disabled (PED) Ports may only be enabled by the xHC. Software cannot enable a port by writing a '1' to this flag. A port may be disabled by software writing a '1' to this flag.	RW1CS
0	Current Connect Status (CCS) 1: Device is present on port. 0: No device is present.	ROS

5.2.2.15 PORTPMSC1 - Port 1 Power Management Status and Control

Address Offset:	4A4h	**Attribute:**	RO, RWS, RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:17	Reserved	RO
16	Force Link PM Accept (FLA)	RW
15:8	U2 Timeout (U2TO)	RWS
7:0	U1 Timeout (U1TO)	RWS

5.2.2.16 PORTLI1 - Port 1 Link Info

Address Offset:	4A8h	**Attribute:**	RO
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:16	Reserved	RO
15:0	Link Error Count (LEC)	RO

5.2.2.17 PORTSC2USB3 - Port 2 Status and Control USB3

Address Offset:	4B0h	**Attribute:**	RO, RWS, RW, RW1S, RW1CS, ROS
Default value:	0000 02A0h	**Size:**	32 bits

Bit	Description	Attribute
31	Warm Port Reset (WPR)	RW1S
30	Device Removable (DR)	RO

29:28	Reserved	RO
27	Wake on Over-current Enable (WOE)	RWS
26	Wake on Disconnect Enable (WDE)	RWS
25	Wake on Connect Enable (WCE)	RWS
24	Cold Attach Status (CAS)	RO
23	Port Config Error Change (CEC)	RW1CS
22	Port Link State Change (PLC)	RW1CS
21	Port Reset Change (PRC)	RW1CS
20	Over-current Change (OCC)	RW1CS
19	Warm Port Reset Change (WRC)	RW1CS
18	Port Enabled Disabled Change (PEC)	RW1CS
17	Connect Status Change (CSC)	RW1CS
16	Port Link State Write Strobe (LWS)	RW
15:14	Port Indicator Control (PIC)	RWS
13:10	Port Speed (Port_Speed) This field identifies the speed of the attached USB Device. This field is only relevant if a device is attached (CCS = '1') in all other cases this field shall indicate Undefined Speed. 1: Full-speed 2: Low-speed 3: High-speed 3: SuperSpeed	ROS
9	Port Power (PP)	RWS
8:5	Port Link State (PLS) Read Value Meaning 0: Link is in the U0 State 1: Link is in the U1 State 2: Link is in the U2 State 3: Link is in the U3 State (Device Suspend) 4: Link is in the Disabled State 5: Link is in the RxDetect State 6: Link is in the Inactive State 7: Link is in the Polling State 8: Link is in the Recovery State 9: Link is in the Hot Reset State 10: Link is in the Compliance Mode State 11: Link is in the Test Mode State 12:14 Reserved 15 Link is in the Resume State	RWS
4	Port Reset (PR) 1: Port Reset signaling is asserted. 0: Port is not in Reset. When software writes a '1' to this bit (from a '0') the bus reset sequence is initiated	RW1S
3	Over-current Active (OCA) This port currently has an over-current condition. '0' = This port does not have an over-current condition. This bit shall automatically transition from a '1' to a '0' when the over-current condition is removed.	ROS

2	Reserved	RO
1	Port Enabled/Disabled (PED) Ports may only be enabled by the xHC. Software cannot enable a port by writing a '1' to this flag. A port may be disabled by software writing a '1' to this flag.	RW1CS
0	Current Connect Status (CCS) 1: Device is present on port. 0: No device is present.	ROS

5.2.2.18 PORTPMSC2 - Port 2 Power Management Status and Control

Address Offset:	4B4h	**Attribute:**	RO, RWS, RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:17	Reserved	RO
16	Force Link PM Accept (FLA)	RW
15:8	U2 Timeout (U2TO)	RWS
7:0	U1 Timeout (U1TO)	RWS

5.2.2.19 PORTLI2 - Port 2 Link Info

Address Offset:	4A8h	**Attribute:**	RO
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:16	Reserved	RO
15:0	Link Error Count (LEC)	RO

5.2.3 Host Controller Runtime Registers

This section defines the FL1009 xHCI Runtime Register space. All Runtime registers are multiples of 32 bits in length. Unless otherwise stated, all registers should be accessed with Dword references on reads, with an appropriate software mask if needed. A software read/modify/write mechanism should be invoked for partial writes. Software should write registers containing a Qword address field using only Qword references. Please refer to Section 5.5 of xHCI Specification Rev 1.0 for detail.

Table 5-4 Host controller runtime registers

Register Symbol	Register Name	Base offset start	Base offset end	Default Value
MFINDEX	Microframe Index	2000	2003	00000000h
IMAN1	Interrupter 1 Management	2020	2023	00000000h
IMOD1	Interrupter 1 Moderation	2024	2027	00000FA0h
ERSTSZ1	Event Ring 1 Segment Table Size	2028	202B	00000000h
ERSTBA_LO1	Event Ring 1 Segment Table Base Address Low	2030	2033	00000000h
ERSTBA_HI1	Event Ring 1 Segment Table Base Address High	2034	2037	00000000h
ERDP_LO1	Event Ring 1 Dequeue Pointer Low	2038	203B	00000000h
ERDP_HI1	Event Ring 1 Dequeue Pointer High	203C	203F	00000000h
IMAN2	Interrupter 2 Management	2040	2043	00000000h
IMOD2	Interrupter 2 Moderation	2044	2047	00000FA0h
ERSTSZ2	Event Ring 2 Segment Table Size	2048	204B	00000000h
ERSTBA_LO2	Event Ring 2 Segment Table Base Address Low	2050	2053	00000000h
ERSTBA_HI2	Event Ring 2 Segment Table Base Address High	2054	2057	00000000h
ERDP_LO2	Event Ring 2 Dequeue Pointer Low	2058	205B	00000000h
ERDP_HI2	Event Ring 2 Dequeue Pointer High	205C	205F	00000000h
IMAN3	Interrupter 3 Management	2060	2063	00000000h
IMOD3	Interrupter 3 Moderation	2064	2067	00000FA0h
ERSTSZ3	Event Ring 3 Segment Table Size	2068	206B	00000000h
ERSTBA_LO3	Event Ring 3 Segment Table Base Address Low	2070	2073	00000000h
ERSTBA_HI3	Event Ring 3 Segment Table Base Address High	2074	2077	00000000h
ERDP_LO3	Event Ring 3 Dequeue Pointer Low	2078	207B	00000000h
ERDP_HI3	Event Ring 3 Dequeue Pointer High	207C	207F	00000000h
IMAN4	Interrupter 4 Management	2080	2083	00000000h
IMOD4	Interrupter 4 Moderation	2084	2087	00000FA0h
ERSTSZ4	Event Ring 4 Segment Table Size	2088	208B	00000000h
ERSTBA_LO4	Event Ring 4 Segment Table Base Address Low	2090	2093	00000000h
ERSTBA_HI4	Event Ring 4 Segment Table Base Address High	2094	2097	00000000h
ERDP_LO4	Event Ring 4 Dequeue Pointer Low	2098	209B	00000000h
ERDP_HI4	Event Ring 4 Dequeue Pointer High	209C	209F	00000000h
IMAN5	Interrupter 5 Management	20A0	20A3	00000000h
IMOD5	Interrupter 5 Moderation	20A4	20A7	00000FA0h
ERSTSZ5	Event Ring 5 Segment Table Size	20A8	20AB	00000000h
ERSTBA_LO5	Event Ring 5 Segment Table Base Address Low	20B0	20B3	00000000h

ERSTBA_HI5	Event Ring 5 Segment Table Base Address High	20B4	20B7	00000000h
ERDP_LO5	Event Ring 5 Dequeue Pointer Low	20B8	20BB	00000000h
ERDP_HI5	Event Ring 5 Dequeue Pointer High	20BC	20BF	00000000h
IMAN6	Interrupter 6 Management	20C0	20C3	00000000h
IMOD6	Interrupter 6 Moderation	20C4	20C7	00000FA0h
ERSTSZ6	Event Ring 6 Segment Table Size	20C8	20CB	00000000h
ERSTBA_LO6	Event Ring 6 Segment Table Base Address Low	20D0	20D3	00000000h
ERSTBA_HI6	Event Ring 6 Segment Table Base Address High	20D4	20D7	00000000h
ERDP_LO6	Event Ring 6 Dequeue Pointer Low	20D8	20DB	00000000h
ERDP_HI6	Event Ring 6 Dequeue Pointer High	20DC	20DF	00000000h
IMAN7	Interrupter 7 Management	20E0	20E3	00000000h
IMOD7	Interrupter 7 Moderation	20E4	20E7	00000FA0h
ERSTSZ7	Event Ring 7 Segment Table Size	20E8	20EB	00000000h
ERSTBA_LO7	Event Ring 7 Segment Table Base Address Low	20F0	20F3	00000000h
ERSTBA_HI7	Event Ring 7 Segment Table Base Address High	20F4	20F7	00000000h
ERDP_LO7	Event Ring 7 Dequeue Pointer Low	20F8	20FB	00000000h
ERDP_HI7	Event Ring 7 Dequeue Pointer High	20FC	20FF	00000000h
IMAN8	Interrupter 8 Management	2100	2103	00000000h
IMOD8	Interrupter 8 Moderation	2104	2107	00000FA0h
ERSTSZ8	Event Ring 8 Segment Table Size	2108	210B	00000000h
ERSTBA_LO8	Event Ring 8 Segment Table Base Address Low	2110	2113	00000000h
ERSTBA_HI8	Event Ring 8 Segment Table Base Address High	2114	2117	00000000h
ERDP_LO8	Event Ring 8 Dequeue Pointer Low	2118	211B	00000000h
ERDP_HI8	Event Ring 8 Dequeue Pointer High	211C	211F	00000000h
DOORBELL1, ... 32	Door Bell 1, ..., 32	3000, ..., 307C	3003, ..., 307F	00000000h

5.2.3.1 MFINDEX - Microframe Index

Address Offset:	2000h	**Attribute:**	RO
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:14	Reserved	RO
13:0	Microframe Index (MI)	RO

5.2.3.2 IMANx - Interrupter x Management

There are 8 IMAN registers: x = 1, 2, 3, …, 8.

Address Offset:	x=1, 2020h-2023h x=2, 2040h-2043h x=3, 2060h-2063h … x=8, 2100h-2103h	**Attribute:**	RO, RW, RW1C
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:2	Reserved	RO
1	Interrupt Enable (IE)	RW
0	Interrupt Pending (Interrupt Pending)	RW1C

5.2.3.3 IMODx - Interrupter x Moderation

There are 8 IMOD registers: x = 1, 2, 3, …, 8.

Address Offset:	x=1, 2024h-2027h x=2, 2044h-2047h x=3, 2064h-2067h … x=8, 2104h-2107h	**Attribute:**	RW
Default value:	0000 0FA0h	**Size:**	32 bits

Bit	Description	Attribute
31:16	Interrupt Moderation Counter (IMODC)	RW
15:0	Interrupt Moderation Interval (IMODI)	RW

5.2.3.4 ERSTSZx - Event Ring Segment Table Size x

There are 8 ERSTSZ registers: x = 1, 2, 3, …, 8.

Address Offset:	x=1, 2028h-202Bh x=2, 2048h-204Bh x=3, 2068h-206Bh … x=8, 2108h-210Bh	**Attribute:**	RW, RO
Default value:	00000000h	**Size:**	32 bits

Bit	Description	Attribute
31:16	Reserved	RO
15:0	Event Ring Segment Table Size (ERSTS)	RW

5.2.3.5 ERSTBA_LOx - Event Ring Segment Table Base Address Low x

There are 8 ERSTBA_LO registers: x = 1, 2, 3, …, 8.

Address Offset:	x=1, 2030h-2033h x=2, 2050h-2053h x=3, 2070h-2073h … x=8, 2110h-2113h	**Attribute:**	RW, RO
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:6	Event Ring Segment Table Base Address Register (ERSTBA_LO)	RW
5:0	Reserved	RO

5.2.3.6 ERSTBA_HIx - Event Ring Segment Table Base Address High x

There are 8 ERSTBA_HI registers: x = 1, 2, 3, …, 8.

Address Offset:	x=1, 2034h-2037h x=2, 2054h-2057h x=3, 2074h-2077h … x=8, 2114h-2117h	**Attribute:**	RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:0	Event Ring Segment Table Base Address (ERSTBA_HI)	RW

5.2.3.7 ERDP_LOx - Event Ring Dequeue Pointer Low x

There are 8 ERDP_LO registers: x = 1, 2, 3, …, 8.

Address Offset:	x=1, 2038h-203Bh x=2, 2058h-205Bh x=3, 2078h-207Bh … x=8, 2118h-211Bh	**Attribute:**	RW, RW1C
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:4	Event Ring Dequeue Pointer (ERDP)	RW
3	Event Handler Busy (EHB)	RW1C
2:0	Dequeue ERST Segment Index (DESI)	RW

5.2.3.8 ERDP_HIx - Event Ring Dequeue Pointer High x

There are 8 ERDP_HI registers: x = 1, 2, 3, …, 8.

Address Offset:	x=1, 203Ch-203Fh x=2, 205Ch-205Fh x=3, 207Ch-207Fh … x=8, 211Ch-211Fh	**Attribute:**	RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:0	Event Ring Dequeue Pointer (ERDP)	RW

5.2.3.9 DOORBELLx - Door Bell Registers x

There are 32 DOORBELL registers: x = 1, 2, 3,…, 32

Address Offset:	x=1, 3000h-3003h x=2, 3004h-3007h x=3, 3008h-300Bh	**Attribute:**	RW, RO

	… x=32, 307Ch-307Fh		
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:16	DB Stream ID (DBSID)	RW
15:8	Reserved	RO
7:0	DB Target (DBT)	RW

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Appendix A Mechanical

A.1 Package Outline

Please refer to the last page of this document.

A.2 Reference of Amkor PCB footprint

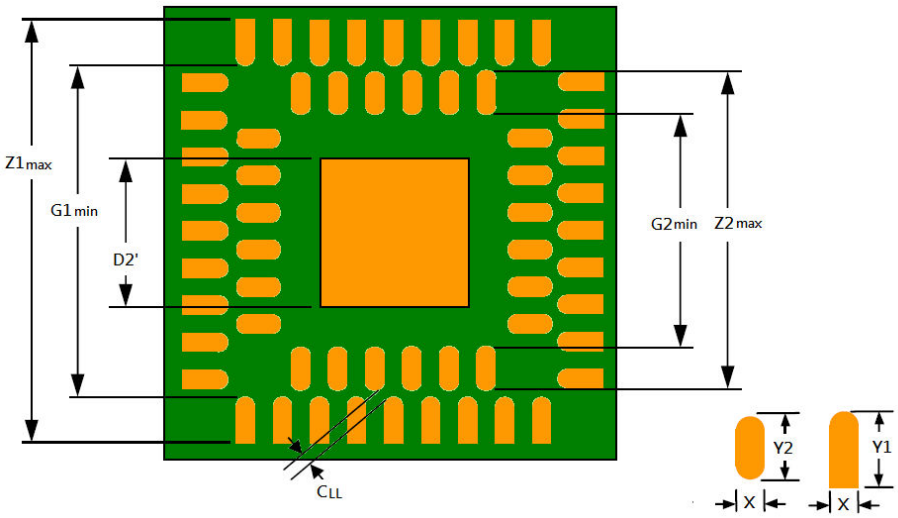


Figure 6

Refer to Figure 6, according to supplier Amkor's recommendation; the land width (X) for both inner and outer rows is needed. Based on history of single row QFN, a lead width (X) of 0.280mm was chosen for 0.500mm pitch. Outer row land pattern dimension Z1Max is calculated using standard IPC methodology and expressed in terms of nominal body size dimension:

$$Z1_{Max} = D_{Min} + 2J_T + \sqrt{C_L^2 + F^2 + P^2}$$

$$D_{Min} = BODYSIZE - \frac{C_L}{2}$$

$$Z1_{Max} = BODYSIZE + 0.340mm$$

For G1Min and Z2Max values, a minimum clearance of 0.200 mm between inner and outer leads must be maintained. For a 0.280 mm lead width and 0.650 mm row pitch, a spacing of 0.130 mm between the inner and outer row leads must be maintained (i.e. 1/2 (G1Min - Z2Max) ≥ 0.13 mm). The nominal distance between package leads is 0.250 mm. Thus the extra 0.120 mm space for toe and heel fillets must be partitioned between the inner and outer leads. Because the toe fillet is more important to solder joint reliability, a design rule of JT ≥ 2 JH is used (i.e. JT = 0.080 mm, JH = 0.040 mm). This results in the following:

$$G1Max = BODYSIZE - 0.880\ mm$$

$$Z2Max = BODYSIZE - 1.140\ mm$$

For G2Min dimension, the heel fillet is limited to conserve space for inner row vias between the leads and the thermal pad. A value similar to the toe fillet is chosen, JH = 0.080 mm. This results in the following:

$$G2_{Min} = BODYSIZE - 2.260\ mm$$

The individual lead dimensions derived from these values are:

Outer row leads: 0.280 x 0.610 mm

Inner row Lead: 0.280 x 0.560 mm

Figure 7 shows the land pattern in graphical format.

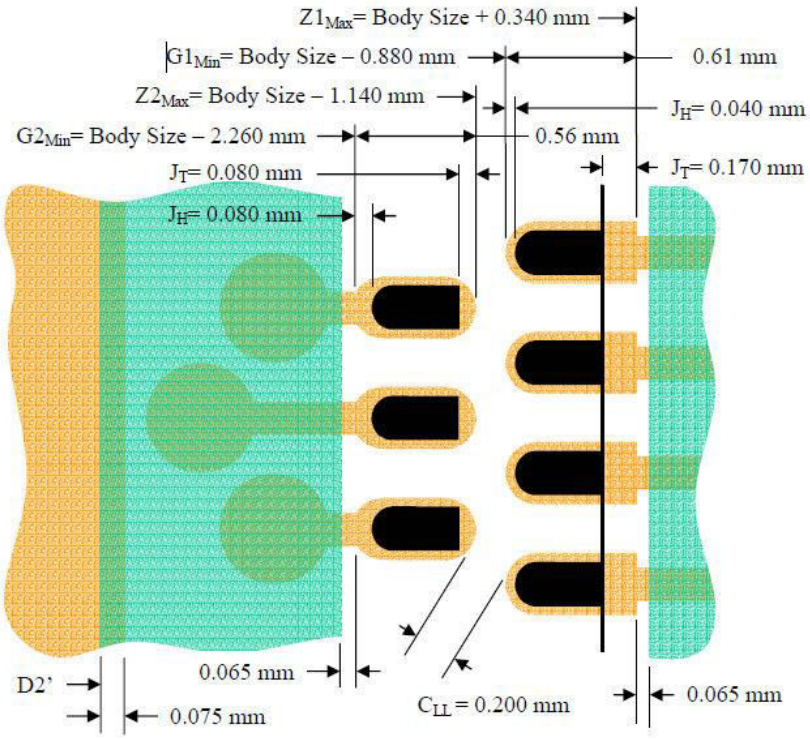


Figure 7 Land pattern of PCB for 0.5mm pitch DRQFN

For some case, we can fine tune pad length for enough CLL value in layout. Here is a PCB pad footprint that use on Fresco Logic's ECB for reference as Figure 8.

SYMBOL	PITCH VARIATION		
	MIN.	NOM.	MAX.
eT		0.50 BSC	
eR		0.715 BSC	
N		116	
NDa		16	
NDb		13	
NEa		16	
NEb		13	
La		0.61	
Lb		0.56	
b		0.28	
D2		3.90	
E2		3.90	

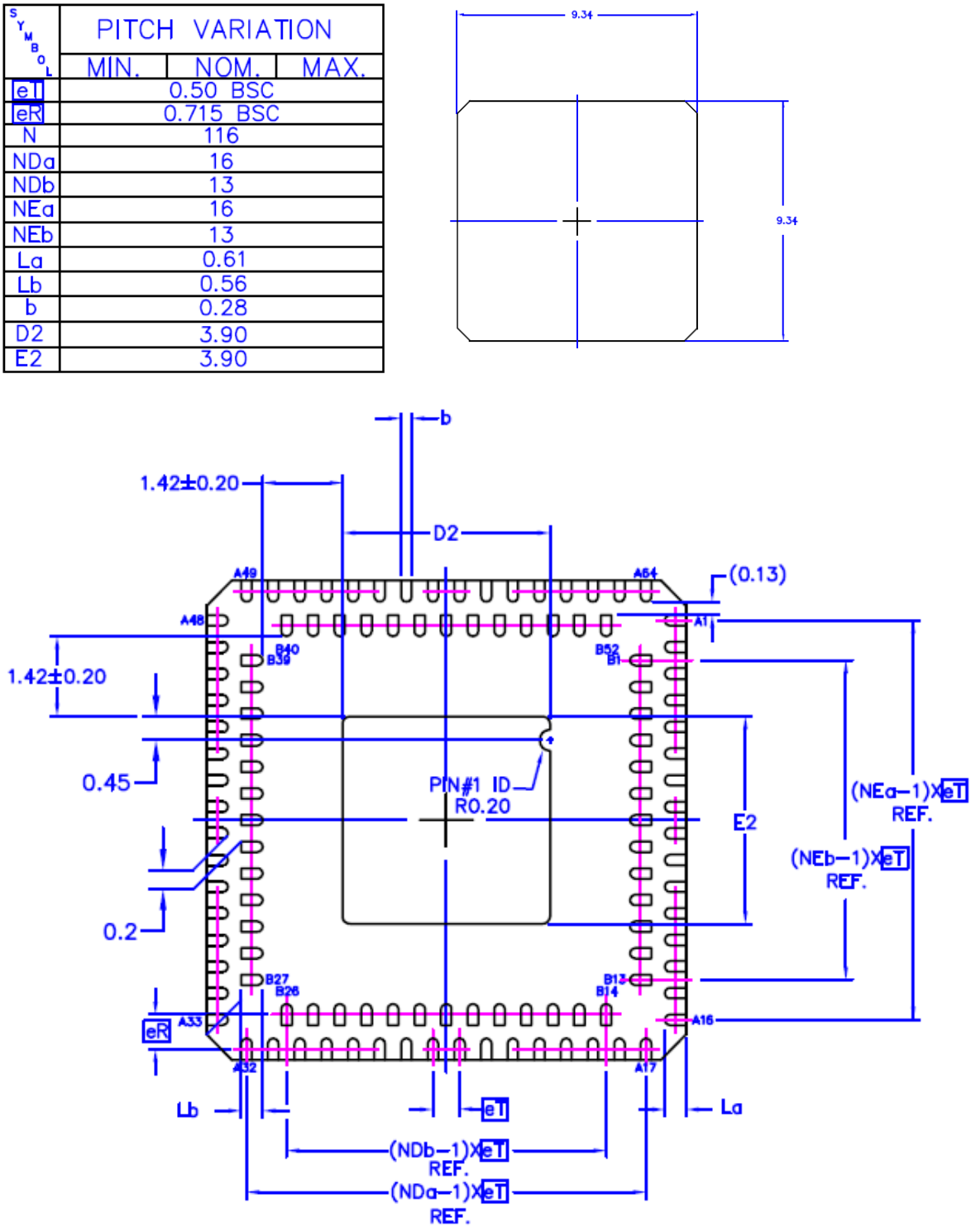


Figure 8 PCB footprint of DRQFN

Appendix B Moisture Sensitive Level

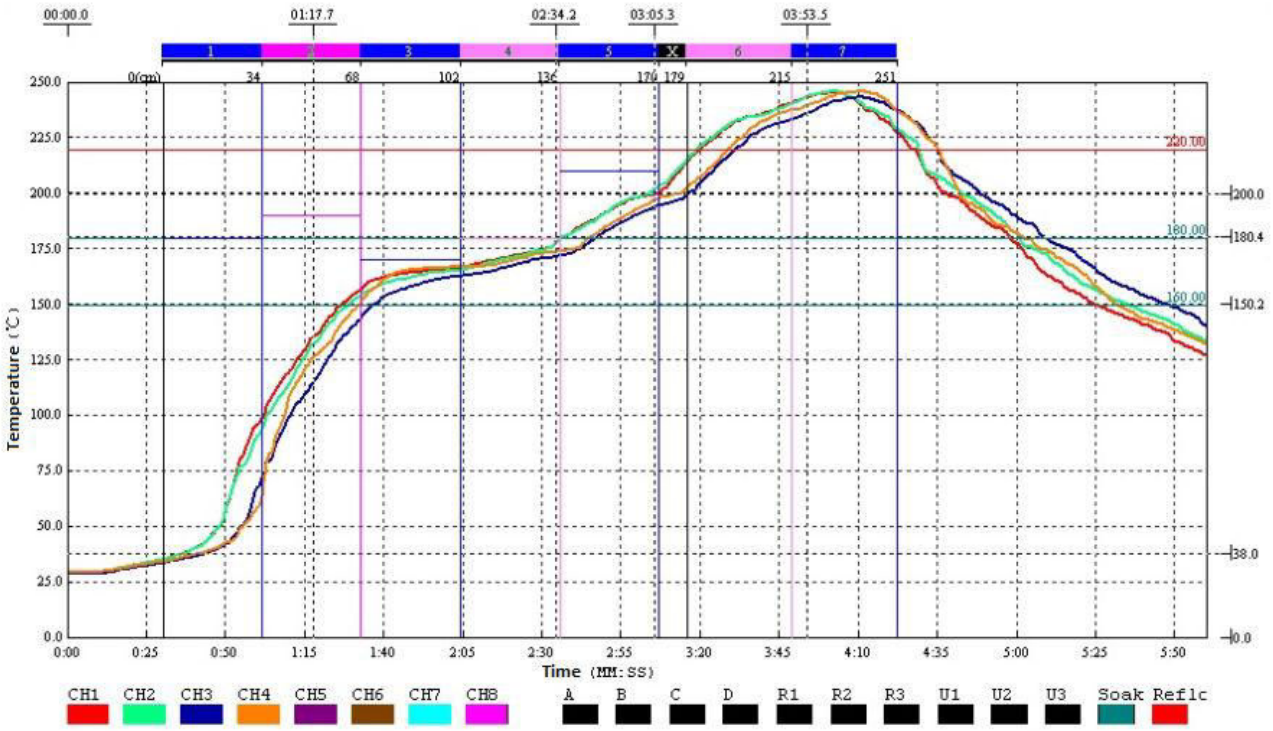
LEVEL

3

FL1009 is **MOISTURE SENSITIVE DEVICE** and should meet **LEVEL 3** requirement as following:

1. Calculated shelf life in sealed bag: 12 months at < 40 ℃ and < 90% RH.
2. After bag opened, devices that will be subjected to reflow solder or other high temperature process must be:
   a. Mounted within 168 hours of factory conditions ≦ 30℃/ 60% RH.
   b. Stored at < 10% RH.
3. Reflow condition: Please refer to IPC / JEDEC J-STD-020.
4. Devices required baking, before mounting if:
   a. Humidity indicator card is > 20% RH when read at 23 +/-5℃, or
   b. 2.a or 2.b is not met.
5. If baking is required, devices may be baked for 12 hours at 125+/-5℃.

Appendix C SMT Thermal Profile



Thermal Profile on Fresco Logic's standard EVB add-in card.

The soldering and void control in QFN package:

Quad Flat No Leads (QFN) package designs got more and more popular in electronic industry nowadays. The most challenges are in soldering and voiding control besides a number of benefits including (1) small size, such as a near die-sized footprint, thin profile, and light weight; (2) easy PCB trace routing due to the use of perimeter I/O pads; (3) reduced lead inductance; (4) easy PCB trace routing; and (5) good thermal and electrical performance due to the adoption of exposed copper die-pad technology. There are some attentions providing when using QFN package in design and SMT process to improve soldering and reduce voids.

1. QFN IC should by well packing due to it's a MSL 3 moisture sensitive component as defined by JTD-020 standard. The cleanness and roughness of pad of QFN will impact soldering.
2. Before SMT, bare PCB baking by 120 +/- 5˚C will help.
3. PCB design:
   - 3.1 Signal pad should use NSMD (Non Solder Mask Defined), die paddle should use SMD (Solder Mask Defined)
   - 3.2 Pad of PCB could be larger than pad of QFN, but limit is equal to.
   - 3.3 Pad of die paddle should match the dimension.
4. Stencil opening:

4.1 Stencil thickness often use 0.13 um is enough.

4.2 Signal pad & die paddle of stencil opening should match the dimensions.

4.3 Die paddle of stencil opening should be web shape to force a similar volume of solder paste to be deposited on all contacts for the QFN package. This is to prevent a stand-off situation where different solder paste heights on the Die Paddle and the Signal Pad contacts causes failure of some or all of the Signal Pad joints to form correctly.

5. Depends on PCB size, trace layout & component numbers and package type to fine tune SMT thermal profile. And long hot SMT thermal profile will help improving soldering and reducing void issue.

   5.1 Long: Increase the time of P2 (Solder Paste Dry, ~100 Seconds) will helping

   5.2 Hot: Up to 250˚C will helping.

6. Solder cream (paste) type: high activity type will better.

7. Usage and storage of solder cream:

   7.1 It should be well storage in 0~10˚C with well sealed.

   7.2 Return to room temp should place 4 hrs before using.

   7.3 When sealed is opened, the environment should controlled under 20~27˚C, 40~80%RH, within 1 hr. Then should return to 0~10˚C.

   7.4 Stir solder cream at least 5 minutes.

8. All vias must be fully tented, especially those in the die paddle area and those close to the Signal Pad contacts.

9. Bow and warp spec of PCB should be careful defined.

10. Recommendations for QA engineering:

    10.1 In-coming Inspection should pay special attention to the Bow and Warp characteristics of PCBs using this package;

    10.2 Normal 2D X-Ray inspection will detect alignment issues between the QFN package and the PCB and can detect solder bridges easily and reliably. This technique will not adequately pick up solder deficiencies or improper wetting of solder pads. To find these types of defect, micro-sectioning of the solder joints is the usual preferred analytical method.

    10.3 During the first few months of introduction of this package type, frequent sampling and destructive testing are strongly recommended to ensure good solder joints are being formed across normal variations in the manufacturing process. This is of particular significance for the solder joints at the corners of the package. Dependent upon facilities available, micro-sectioning along the center-lines of both Signal Pad contacts is preferred, but a lower-cost solution is to break the package from the PCB and visually inspect the joints with a microscope. This technique will pick up extreme failures, so occasional micro-sectioning is still recommended.

Please refer to Fresco Logic's "DRQFN package application reference" for more information.

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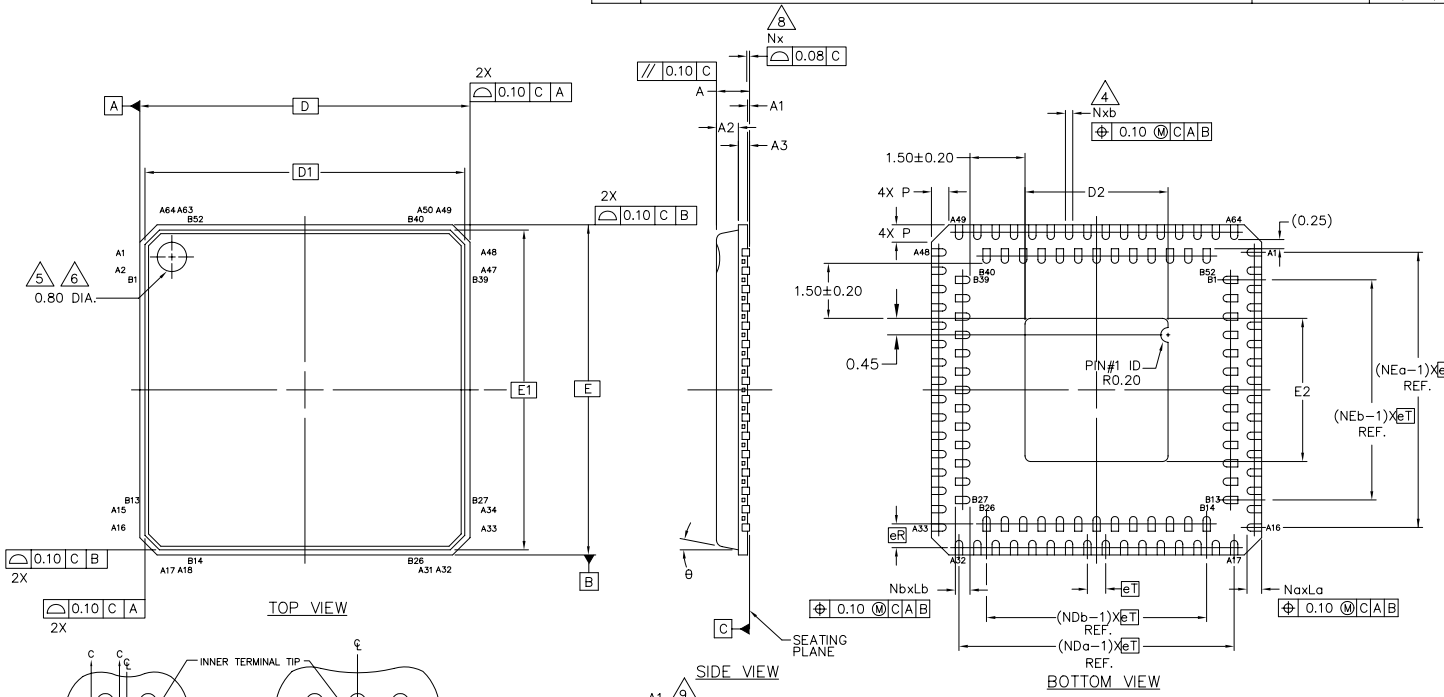
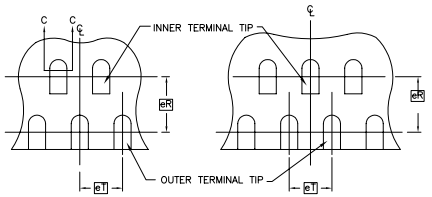
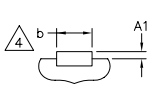
REVISION HISTORY			
REV	DESCRIPTION	ORIGINATOR	DATE
0A	INITIAL REVIEW	HIJEON	09/09/10

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.85	0.90	
A1	0.00	0.01	0.05	8
A2	0.55	0.60	0.65	
A3		0.25 REF.		
D		9.00 BSC		
D1		8.73 BSC		
E		9.00 BSC		
E1		8.73 BSC		

SYMBOL	PITCH VARIATION			NOTE
	MIN.	NOM.	MAX.	
eT		0.50 BSC		
eR		0.65 BSC		
N		116		3
NDa		16		3
NDb		13		3
NEa		16		3
NEb		13		3
La	0.30	0.40	0.50	
Lb	0.30	0.40	0.50	
b	0.18	0.22	0.30	4
D2	3.80	3.90	4.00	
E2	3.80	3.90	4.00	
θ	–	–	12°	
P	0.24	0.42	0.60	







NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   NDa, NDb ARE THE NUMBER OF TERMINALS IN X-DIRECTION &
   NEa, NEb ARE THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. UNILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
9. APPLIED ONLY FOR TERMINALS.

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS

DECIMAL
X.X ±0.1
X.XX ±0.05
X.XXX ±0.030

ANGULAR ±1°

INTERPRET DIM AND TOL PER ASME Y14.5M – 1994

DRAWING TYPE

PACKAGE OUTLINE

PACKAGE GROUP	BODY X	BODY Y	BODY Z
DRQFN (DRMLF)	9.00	9.00	0.85

BALL PITCH	RAW BALL SIZE	BALL COUNT	BALL MATRIX
0.50/0.65	N/A	116	N/A

SIZE	SCALE		
A3	7.5:1	427134P0	0A

SHEET 1 OF 1