SILICON LABORATORIES

AN124

PIN SHARING TECHNIQUES FOR THE C2 INTERFACE

Relevant Devices

This application note applies to the following devices: C8051F300, C8051F301, C8051F302, and C8051F303.

Introduction

C8051F30x devices include an on-chip Silicon Labs 2-Wire (C2) Interface for in-system programming, debugging, and boundary scan testing. Two signals are associated with the C2 Interface: C2 Clock (C2CK) and C2 Data (C2D). To preserve package pins, the C2CK and C2D pins also function as the user pins /RST and P0.7, respectively.

To enable in-system programming, debugging, and/or boundary scan functions, external resistors are typically used to isolate C2 traffic from the external system. The isolation configuration depends on the user function associated with the /RST and P0.7 pins on the target device. This application note discusses C2 isolation configurations for each user function. If pins /RST and P0.7 are not occupied by user functions, no isolation circuitry is needed.

Key Points

- Pins /RST and P0.7 are 'borrowed' by the C2 Interface during C2 communication.
- Isolation resistors are typically required to perform in system programming, debugging, or boundary scan testing via C2.
- The C2 isolation configuration depends on the user function associated with pins /RST and P0.7.

About the C2 Pins

When C2 communication is idle, the C2 pins (C2CK and C2D) function as user pins /RST and P0.7, respectively. The interface master initiates C2 communication by generating an active-low strobe on the C2CK pin. Following this strobe, the interface master may safely 'borrow' the C2 pins without disturbing the user functions.

C2CK (/RST)

The C2CK signal provides the clock for all C2 communications. When C2 communication is idle, the C2CK pin functions as the active-low reset I/O pin (/RST).

As a user input, the C2CK pin is used to generate a device reset when held low for more than 20 µs. As a user output, the C2CK pin may be driven low by the on-chip 'F30x VDD monitor. When the C2CK pin is not being driven, an internal (weak) pull-up resistor pulls the C2CK pin high. For in-system debugging, an external pull-up resistor is required (see Figure 6).

C2 events on C2CK are ignored by the reset hardware as long as C2CK is low for less than 5 µs. Since the C2CK pin is always an open-drain output, the interface master may initiate C2 communication at any time with an active-low strobe on C2CK.

C2D (P0.7)

The C2D signal serves as the data bus for all C2 communications. When C2 communication is idle, the C2D pin functions as the Port pin P0.7.

When a C2 event is detected on the C2CK pin, the target device automatically configures the C2D pin

to accept C2 data. During C2 communication, the C2 Interface controls the C2D pin; following each C2D communication frame, the C2D pin is restored to the user-defined (P0.7) state.

Pin Sharing Configurations

This section describes the isolation configurations for different user functions on C2-shared pins. Each of the following illustrations describe the pin sharing configuration for a single C2 pin; these illustrations may be applied to C2CK and/or C2D.

The required isolation configuration depends on the signal direction of the associated user pin. Each signal direction (input, output, and bi-directional) is discussed.

Resistors R1 and R2 serve to limit the current sunk/sourced by the interface master and external system; resistor values should be chosen according to the capabilities of the interface master and external system drivers (if applicable). For applications using the Silicon Labs EC-2 as the interface master, resistors R1 and R2 should be a minimum of 1 kΩ.

Input Only

A pin is considered an input if the target device never drives the logic level of the pin. For the input only case, one resistor is required. See Figure 1.

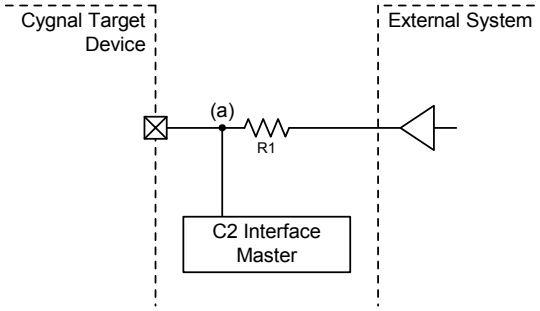

Figure 1. Input Only Configuration

The interface master controls the logic level at node (a) during C2 communication; the isolation resistor R1 ensures that no contention occurs between the interface master and the external system.

Output Only

A pin is considered an output only if the external system never drives the logic level of the pin. The typical output case is shown in Figure 2.

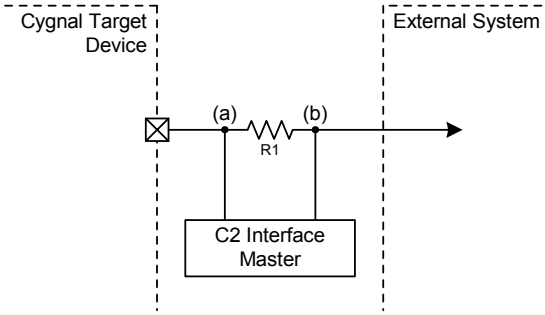

Figure 2. Output Only Case 1

The configuration in Figure 2 assumes that the logic level seen by the external system should not change during C2 communication (toggling at node (b) during C2 communication would disturb the external system). In this case, the interface master samples the logic level at node (a) and drives the same logic level at (b) before initiating C2 communication at node (a). The master may then communicate with the target device at node (a) while the isolation resistor R1 ensures that the external system is not disturbed.

If the logic level seen by the external system is allowed to change during C2 communication, the

pin sharing configuration reduces to that shown in Figure 3.

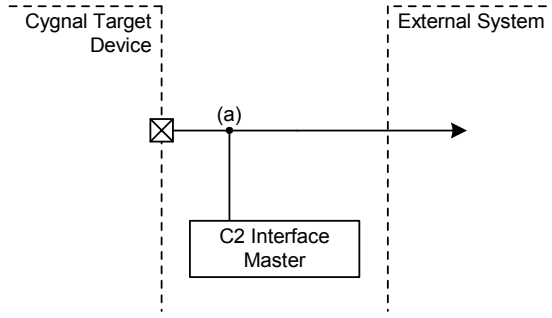

Figure 3. Output Only Case 2

Bi-directional

A pin is considered bi-directional if both the target device and the external system may drive the pin. In this case, two isolation resistors are typically required, as shown in Figure 3.

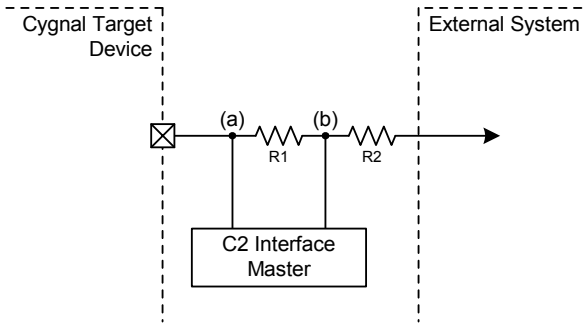

Figure 4. Bi-directional Case 1

The configuration in Figure 4 assumes that the logic level seen by the external system should not change during C2 communication. In this case, the interface master samples the logic level at (a) and then drives that logic level at (b) before initiating C2 communication at node (a). Isolation resistor R2 ensures that no contention occurs between the interface master and the external system at node (b).

If the logic level seen by the external system is allowed to change during C2 communication, the pin sharing configuration reduces to that shown in Figure 5.

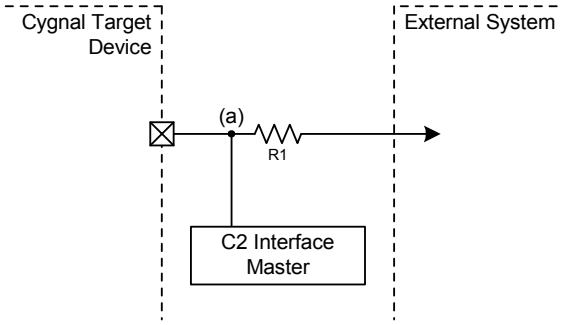

Figure 5. Bi-directional Case 2

Here the interface master may communicate with the target device at node (a), while isolation resistor R1 ensures that no contention occurs between the interface master and the external system.

About the Interface Master

C2 pin sharing is applicable to each of the following: in-system programming, in-system debugging, and boundary scan testing. Each task includes C2 communication between a target Silicon Labs C2 device and a C2 interface master. For in-system debugging, the interface master must be the Silicon Labs Serial Adapter (EC-2). For in-system programming, the interface master may be the Silicon Labs Serial Adapter (EC-2) or any user device configured to operate as a C2 master. For boundary scan testing, the interface master is any user device configured to perform boundary scan functions via the C2 Interface.

Figure 6 shows the necessary connections for the 10-pin connector used with the Silicon Labs Serial Adapter (EC-2). Note that to perform in-system debugging, an external pull-up resistor should be connected between the C2CK pin and VDD as shown in Figure 6. The C2CK pull-up resistor R3 should be a maximum of 10 kΩ.

Shaded areas in Figure 6 indicate connections/components that are application-dependent (see the pre-

vious section, ““Pin Sharing Configurations” ”).
All other connections are required.

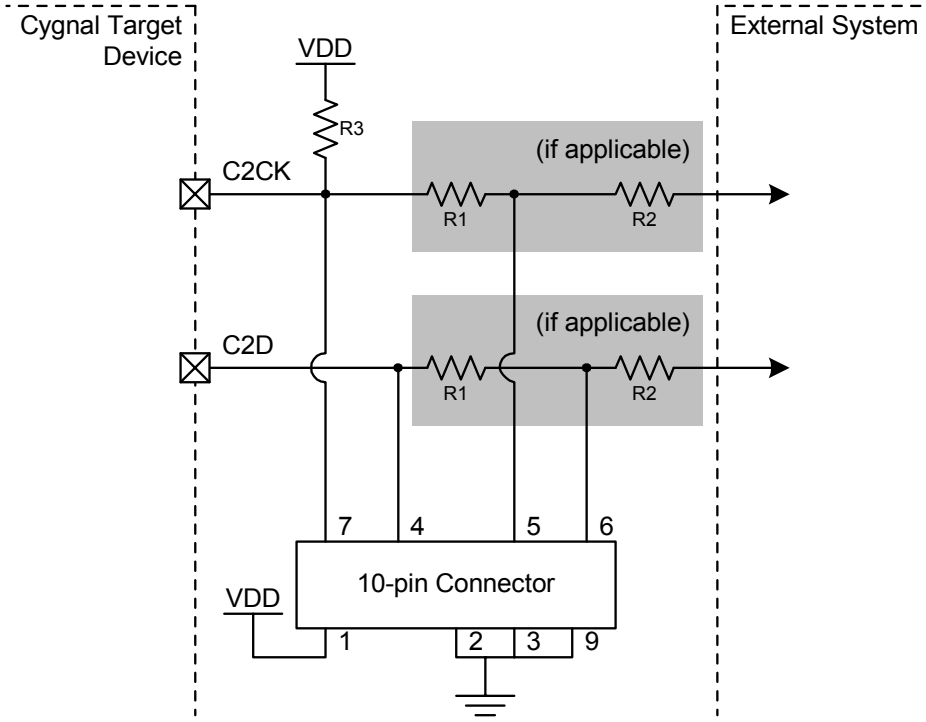

Figure 6. 10-pin Header Connections for use with EC-2

Notes:

Contact Information

Silicon Laboratories Inc.
4635 Boston Lane
Austin, TX 78735
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032
Email: productinfo@silabs.com
Internet: www.silabs.com