AN119

CALCULATING SETTLING TIME FOR SWITCHED CAPACITOR ADCS

Relevant Devices

This application note applies to the following devices:

C8051F000, C8051F001, C8051F002, C8051F005, C8051F006, C8051F007, C8051F010, C8051F011, C8051F012, C8051F015, C8051F016, C8051F017, C8051F206, C8051F220, C8051F221, and C8051F226.

Introduction

Many of Silicon Lab's devices feature an on-chip SAR analog-to-digital converter (ADC). These ADC's use a *sample capacitor* that is charged to the voltage of the input signal that is used by the SAR logic to perform its data conversion. Due to the ADC's sample capacitance, input impedance, and the external input circuitry, there will be a *settling time* required for the sample capacitor to assume the measured input signal voltage. This application note describes a method for calculating the required settling time for good ADC measurements and methods to achieve meeting settling time requirements.

Key Points

- The application must allot for settling time for both the on-chip ADC circuitry and the off-chip input circuitry (e.g., anti-alias filter)
- The *minimum* settling time for the ADC input circuitry is 1.5 µs.
- A Thevenin equivalent of the input circuitry is used to estimate the required settling time for the desired accuracy.

Equivalent Circuit

In order to calculate the estimated settling time, we present an equivalent circuit that approximates the impedance and capacitance of the ADC tracking circuit (i.e., the analog multiplexer (AMUX), transmission gates, parasitic capacitance, sample capacitance, etc.) An equivalent circuit that approximates these parameters in lumped elements is shown in Figure 1 below. The input signal will typically be filtered through some external input circuitry as determined by the system designer. Most often this will include an anti-alias filter connected to the input pin of the device. The AMUX routes the input signal from the input pin to the ADC. As a conservative estimate, the impedance and capacitance is equivalent to a 5 kΩ resistor and 10 pF capacitor in series. Note this is a simplified representation of the ADC circuit in tracking mode.

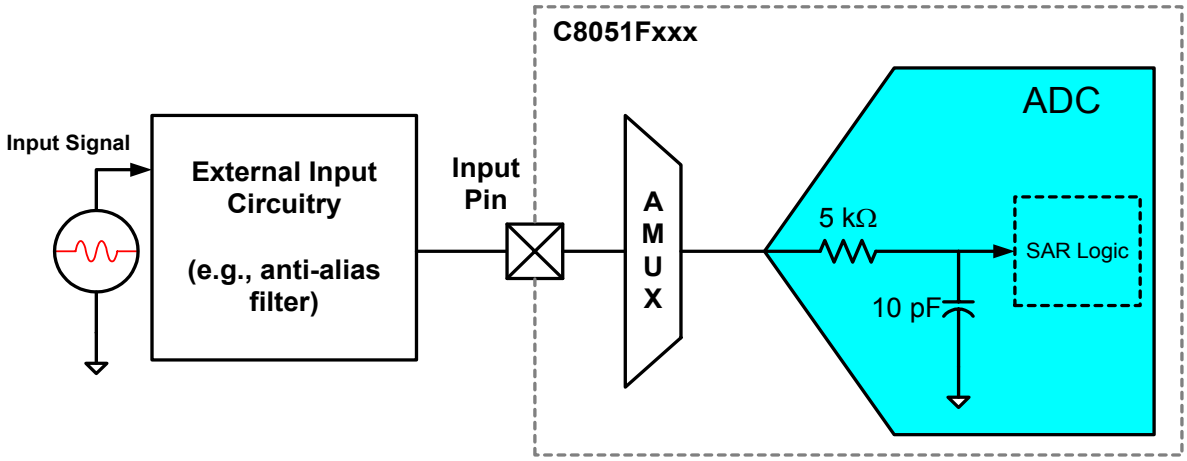

Figure 1. Equivalent ADC Circuit For Estimating Settling Time

Differential Ended Measurement

Figure 1 illustrates the equivalent tracking mode approximation in a single-ended measurement with respect to ground. This is a good approximation for many types of measurements using the ADC. The time constant of the Thevenin equivalent will be the product of the resistance and capacitance shown. However, many Silicon Labs ADC's also have the ability to make *differential* measurements. In this case, the equivalent circuit is different as shown in Figure 2. To observe how this affects settling time, we calculate the new time constant. As shown, the time constant of the new equivalent circuit is the same as in a single-ended measurement. This circuit will have a different resistance and capacitance, but the product will be the same thus the settling time will be the same:

$$\tau_{differential} = (2R) \cdot (C/2) = RC = \tau_{single}$$

Determining Settling Time

The settling time required for a given application is determined by the ADC input circuit, external circuitry (e.g., anti-alias filter), and the ADC settling time specification. If proper settling requirements are not met, then the ADC may not meet the specifications posted in the data sheet. We must consider the settling time of the ADC input circuit, external circuitry, and the minimum required by the ADC specification in order to calculate settling time requirements. We design to the most restrictive requirement.

Minimum Settling Time Specification

Silicon Lab's ADC specification requires a 1.5 µs tracking time. Even though Figure 1 presents an equivalent circuit for settling time estimation, the actual ADC peripheral has numerous components that affect settling time such as switched capacitors, transmission gates, etc. Thus, the minimum specified settling time is 1.5 µs. If the calculated settling time using the equivalent circuit in Figure 1 or the external circuit is greater than 1.5 µs, then the settling time will be dictated by external components.

Settling Time of the ADC Input Circuit

Because the equivalent input tracking circuit of the ADC is an RC circuit, we will calculate settling time in terms of time constants. It is useful to specify settling time as the number of time constants it

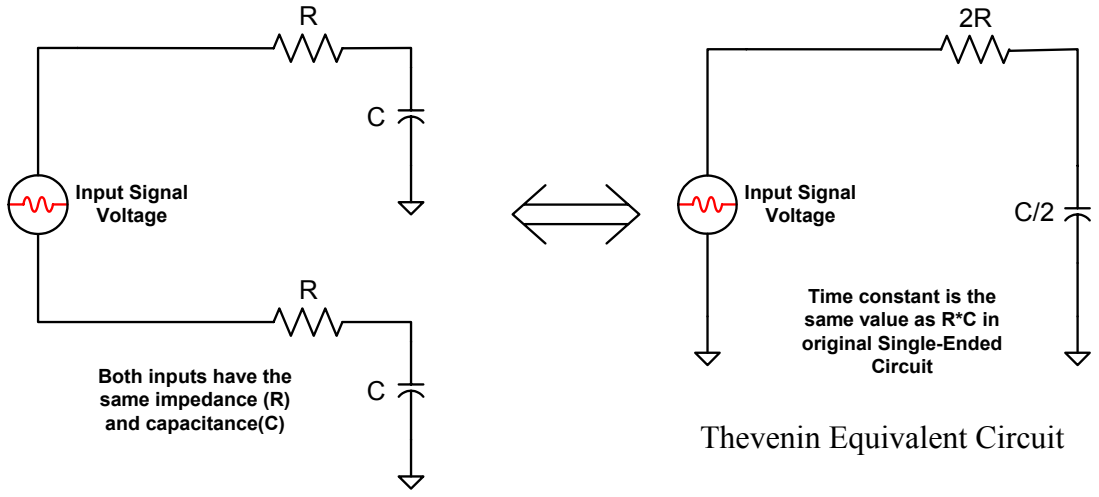

Figure 2. Differential Measurement Time Constant

will take for an accuracy specified as a fraction of the least significant bit (LSB):

$$LSB = \frac{V_{ref}}{2^N}$$

Equation 1. LSB Code Width Calculation

To calculate the time (*t*) required for the sample capacitor voltage to settle to within one-fourth of an LSB of the input voltage, we derive an equation for the calculation:

$$V(t) = V_{in} \cdot (1 - e^{-t/\tau})$$

where V_{in} is the input voltage at the input pin of the device and the time constant is $\tau = RC$.

Equation 2. Charging The ADC Tracking Circuit

Solving for *t* in terms of the number of time constants, τ, we obtain the result:

$$t = -\ln\left[1 - \frac{V(t)}{V_{in}}\right]\tau$$

Equation 3. Settling Time In Terms of the Number of Time Constants, τ

To calculate the voltage to be within 1/4 LSB of the input voltage assuming a full-scale step input ($V_{in} = V_{ref}$):

$$V(t)_{\frac{1}{4}LSB} = V_{ref} \cdot \left(1 - \frac{1}{2^N \cdot 4}\right)$$

where N is the number of ADC bits

Equation 4. Voltage Calculated Within 1/4 LSB Of Measured Input Voltage

Substituting Equation 4 into Equation 3 and again assuming a full-scale step input ($V_{in} = V_{ref}$), we obtain the following result:

$$t = -\ln\left(\frac{1}{2^N \cdot 4}\right)\tau$$

where N is the number of ADC bits

Equation 5. Number of Time Constants to Settle Within 1/4 LSB

Assuming a 12-bit ADC, Equation 5 above becomes:

$$= -\ln\left(\frac{1}{4096 \cdot 4}\right)\tau = \ln(4096 \cdot 4)\tau = 9.7$$

Note that this is for the case of a 12-bit ADC where we desire 1/4 LSB accuracy. If we instead are using an 8-bit ADC and also want 1/8 LSB accuracy, then Equation 5 becomes:

$$t = \ln(256 \cdot 8)\tau = 7.6\tau$$

As shown in Figure 1, we estimate the impedance and capacitance in Equation 2 to be R = 5 kΩ and C = 10 pF. Substituting the values of R and C, τ = 50 ns. Thus, the settling time for the 12-bit ADC and 1/4 LSB accuracy is about 500 ns, and the 8-bit ADC with 1/8 LSB accuracy is 380 ns. However, the ADC specification for minimum settling time is 1.5 µs, which is more restrictive in both cases.

External Circuit Settling Time

When the external circuitry is connected to the analog input pin, the settling time may be affected. Such circuitry typically includes an anti-aliasing filter used to remove higher frequency noise that will *alias* or *fold* into the signal band of interest. There are many different filter designs, and all will affect input impedance and have a settling time associated with them. The external circuit's capacitance and output impedance will affect the settling

time. The design of anti-alias filters should be designed to drive the approximately 10 pF in the ADC input circuit. Such effects must be considered when calculating settling time of the ADC measurement. If the input filter settling time is extremely long, then this settling time will dictate the settling time of the system.

External Circuit Examples

The following are examples of common external circuits commonly interfaced with the input to an ADC.

1. Passive RC Anti-aliasing Filter:
   Such low-pass filters use passive components (resistors and capacitors). A single-pole passive filter will have a higher impedance and longer settling time. However, if the filter's capacitor is an order of magnitude higher than the sample capacitor, the filter capacitor will charge the sample capacitor quickly. Thus, once the filter settle time is satisfied, the application then switches to that input, and the filter capacitor can charge the sample capacitor within the internal ADC circuit specification time (1.5 µs).

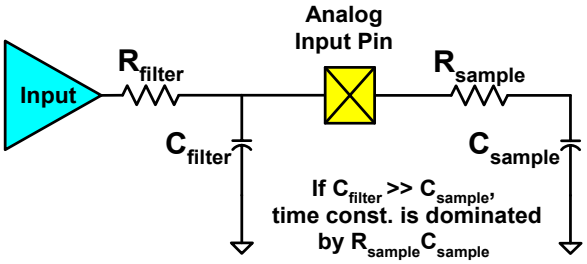

Figure 3. Passive Anti-Aliasing Filter

2. Active Anti-aliasing Filter:
   Such filter utilize operational amplifiers (op-amps) in combination with resistors and capacitors to implement low-pass filters. These filters form good buffer stages as they have higher input impedance and lower output impedance. Op-amps may introduce some noise. Refer to the manufacturer's data sheet for such information when considering design of filters with op-amps.

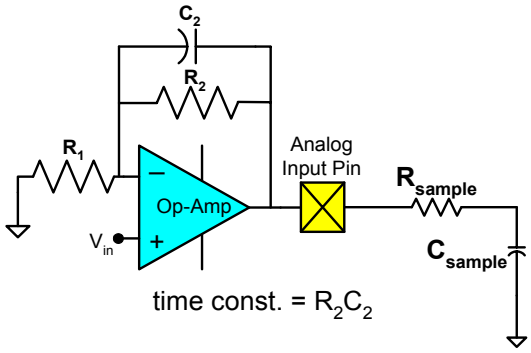

Figure 4. Active Anti-Alias Filter

3. Measurement Transducer Circuit:
   Transducers provide a measurement voltage that is proportional to a measured parameter (e.g., pressure or weight). Such devices are typically high impedance circuits represented by a voltage source and a large resistance. In this case, the settling time is dictated by the transducer's impedance.

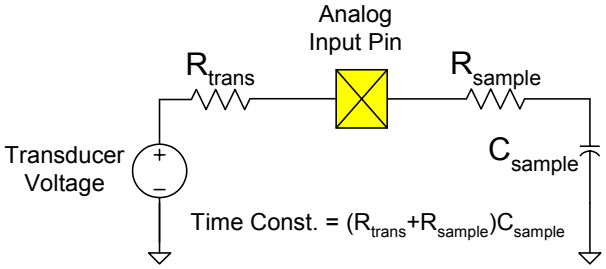

Figure 5. Transducer Circuit Equivalent

Methods For Satisfying Settling Time Specification

There are various methods for handling settling time requirements of both the tracking circuit and external circuitry. The best way to avoid settling time errors will depend on the specific application.

Low-Power Tracking Mode

Low-power tracking mode is a useful method to ensure the minimum settling time requirement is

satisfied. The ADC is placed in low-power tracking mode by setting the ADCTM = 1 in the ADC0CN special function register. When a conversion is initiated while in low-power tracking mode, the device automatically tracks for 3 SAR clock cycles before performing the data conversion. Because the maximum SAR clock frequency specification is 2 MHz, 3 SAR clock cycles will take a minimum of 1.5 µs. Thus, when using low-power tracking mode the minimum settling time specification will be met.

Low power tracking mode timing diagrams in Figure 6 and Figure 7 show the tracking and conversion timing with respect to the SAR clock and trigger source that initiates the track/convert process. Figure 6 shows the timing for an external CNVSTR signal trigger. Figure 7 shows the timing for a software initiated process triggered by ADBUSY, Timer2 overflow, or Timer3 overflow.

Manually Controlling Settling Time

Once the AMUX is set to sample an input pin, the tracking circuit will begin to charge the sample capacitor. The external input circuit should be designed to drive 10 pF in the tracking circuit, ideally within the minimum 1.5 µs settling time. If low power tracking mode is not used (ADCTM = 0 in the ADC0CN special function register), the ADC will track the input continuously and a start of conversion signal will initiate an immediate data conversion. Data conversions take 16 SAR clock cycles to complete. The timing diagrams are presented in Figure 6 and Figure 7. The user must calculate proper settling time and initiate a conversion via software (Timer2 overflow, Timer3 overflow, or ADBUSY = 1) or an external signal (CNVSTR).

Multiple ADC Inputs

Many applications will use the ADC to measure parameters from several sources by switching the ADC input analog multiplexer (AMUX). This is a useful technique, however, the settling time specifi-

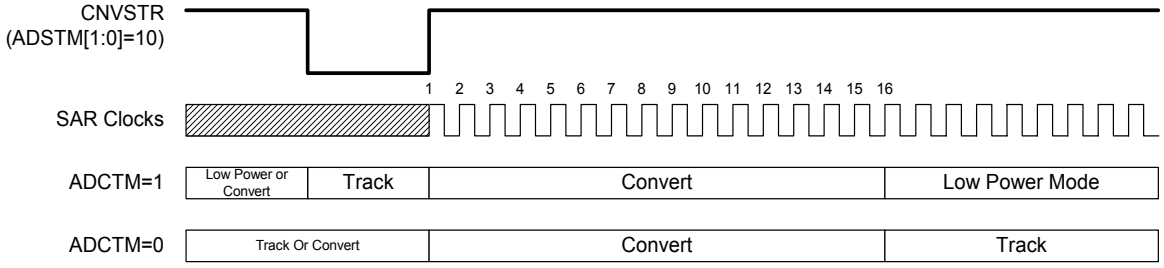

Figure 6. Low Power Timing Diagram With External CNVSTR Trigger

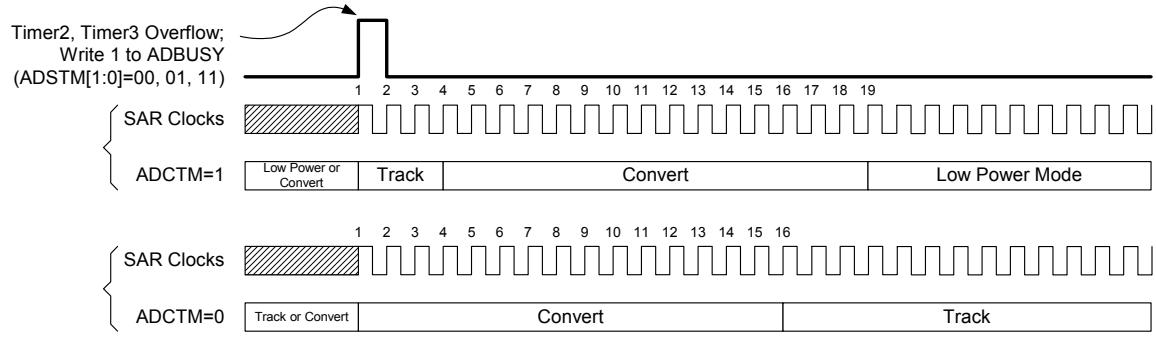

Figure 7. Low Power Timing Diagram With Software Trigger

cations must be considered when switching the AMUX settings (i.e., changing the input to the ADC). *Each time the application software switches from one ADC input to another, there must be at least 1.5 µs of settling time prior to initiating an ADC conversion.*

NOTE: Switching the input channel and initiating a data conversion without waiting for the appropriate settling time can give the appearance of sampling the previous input channel. This is because the sampling capacitor will still hold approximately the same charge from the last data conversion.

We recommend placing the ADC in low power tracking mode and initiating ADC conversions after the AMUX settings have been switched. In this way, the ADC will track for 3 SAR clock cycles before an ADC conversion after the ADC input was changed by the AMUX.

Low Power Applications

If the designer wishes to use a power saving mode (e.g., IDLE Mode), it is recommended that low-power tracking mode be used to ensure the minimum settling time requirement is met upon "waking" the device. The MCU is placed in a power saving mode between samples. After an ADC data conversion is complete, the device is placed back into NORMAL mode and the ADC sample is processed and stored. If the application polls the ADBUSY bit, then the MCU will have to be in NORMAL mode during the data conversion as well. The ADC will then track for 3 SAR clock cycles and then perform the data conversion. After the sample is processed, the device can then be placed back into a power saving mode. Thus, low power tracking can be used to ensure the minimum settling time requirements are satisfied when using the ADC in low power applications (i.e., "waking" the device from IDLE Mode only for sample processing.) See Figure 8 below.

Additionally, settling time of the external circuitry can be satisfied while the device is in a power saving mode. For example, the input signal can be allowed to settle in an anti-aliasing filter while in a power saving mode. Once this settling time has passed, the signal to "wake" the device and initiate a track and conversion is sent such that the device is in low power as long as possible, and the 1.5 µs settling time specification will be met with the external circuit settling time already satisfied.

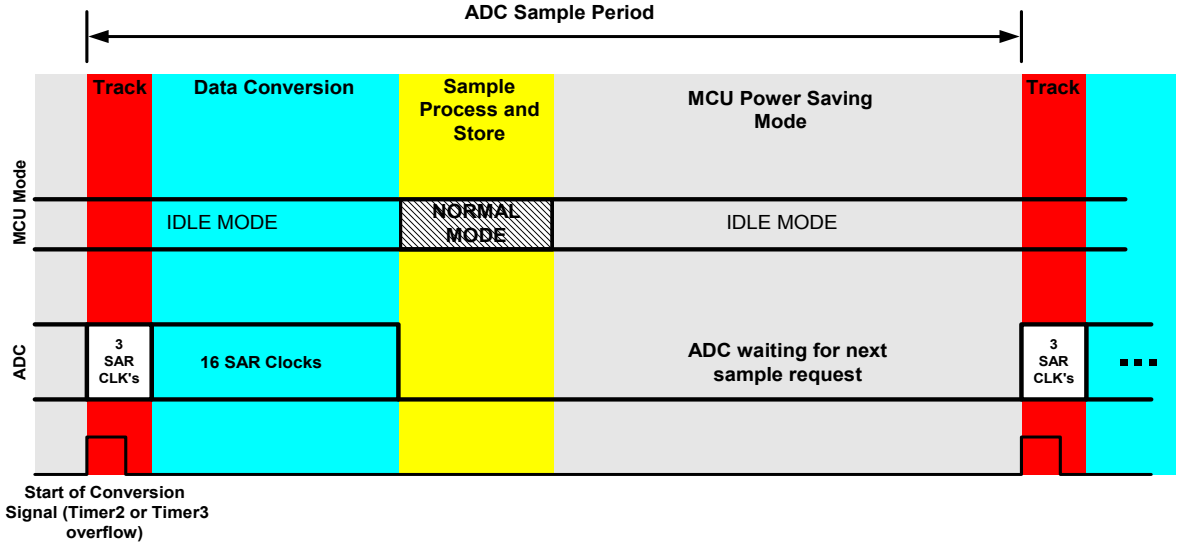

Figure 8. Low-Power Tracking Mode Used With Power Saving Mode

Summary

Settling time must be considered in designs that utilize the ADC for measurements. If settling time requirements are not met, the ADC measurements may not meet posted specifications.

The settling time requirement of a system may be affected by the external circuitry (time constant and output impedance), ADC input circuit, and the ADC settling time specification posted in the data sheet (1.5 µs).

A Thevenin equivalent circuit of the ADC input and external circuitry should be used to estimate the most conservative settling time requirement. If this settling time requirement is less than the 1.5 µs ADC specification, then the 1.5 µs specification should be used.

The following table summarizes the guidelines when determining which method will be best to satisfy the system's settling time requirements.

NOTE: 1.5 µs settling time may not be the most restrictive settling time requirement!

Table 1. Satisfying Settling Time

ADC Sample Technique	How Accomplished	Comments
Manual	Software Delay	More control for the designer, but must ensure that the ADC settling time specification of 1.5 µs is met.
Low-Power Tracking Mode	Set the ADCTM bit to '1' (in the ADC0CN SFR)	Automatically tracks for 3 SAR clocks prior to performing data conversion. Enforces the 1.5 µs settling time specification upon start of conversion signal
Multiple ADC input	Use AMUX to switch ADC input in software	Recommend using low-power tracking mode. When AMUX setting is changed, initiate conversion and ADC will track for 3 SAR clocks prior to data conversion. **Tracking of at least 1.5 µs is required each time ADC input is changed!**
Low Power Applications	Use low-power tracking mode, disable ADC when not in use, use MCU power saving modes	Use low-power tracking mode to ensure 1.5 µs settling time specification is met when "waking" device from IDLE Mode between samples. Low-power tracking saves some power (vs. continuous tracking), but it is best to disable ADC when not in use.

Contact Information

Silicon Laboratories Inc.
4635 Boston Lane
Austin, TX 78735
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032
Email: productinfo@silabs.com
Internet: www.silabs.com