AN431

C8051F93x-C8051F90x Software Porting Guide

Relevant Devices

This application note applies to the following devices:
C8051F930, C8051F931, C8051F920, C8051F921, C8051F912, C8051F911, C8051F902, C8051F901

1. Introduction

Microcontrollers in the C8051F93x-C8051F90x product family are designed to be software compatible with each other. This allows a single code base to be developed which targets MCUs that range from 8 to 64 kB in program memory size. Figure 1 shows the various memory size options in the C8051F93x-C8051F90x device family. This porting guide is designed to help the programmer easily port code between devices in the product family or write processor-independent software that can execute on any device in the product family.

This porting guide highlights differences between the various MCUs in the product family. Two devices, the C8051F912 and C8051F902, have more features than the rest of the devices in the family. The use of these "plus" features will make the software incompatible with the rest of the devices in the family. These features should only be used if there are no future plans to use the same software on a different device in the product family.

2. Key Points

- **Header File Usage**: The C8051F93x-C8051F90x family has two header files that may be used interchangeably when writing code that targets any device in the product family.
- **Plus Features**: 'F912 and 'F902 devices are more feature-rich than other devices in the C8051F93x-C8051F90x product family. To maintain code compatibility across all devices in the product family, the additional "plus" features should not be used.
- **Package**: C8051F93x-C8051F90x devices ranging from 8 to 64 kB are available in the 24-pin QFN package. These devices are pin-for-pin and software compatible with each other.
- **Power**: All devices in the C8051F93x-C8051F90x family share the same low power modes and have excellent power efficiency. The 'F912 and 'F902 have even more power saving modes than the standard devices in the C8051F93x-C8051F90x family.

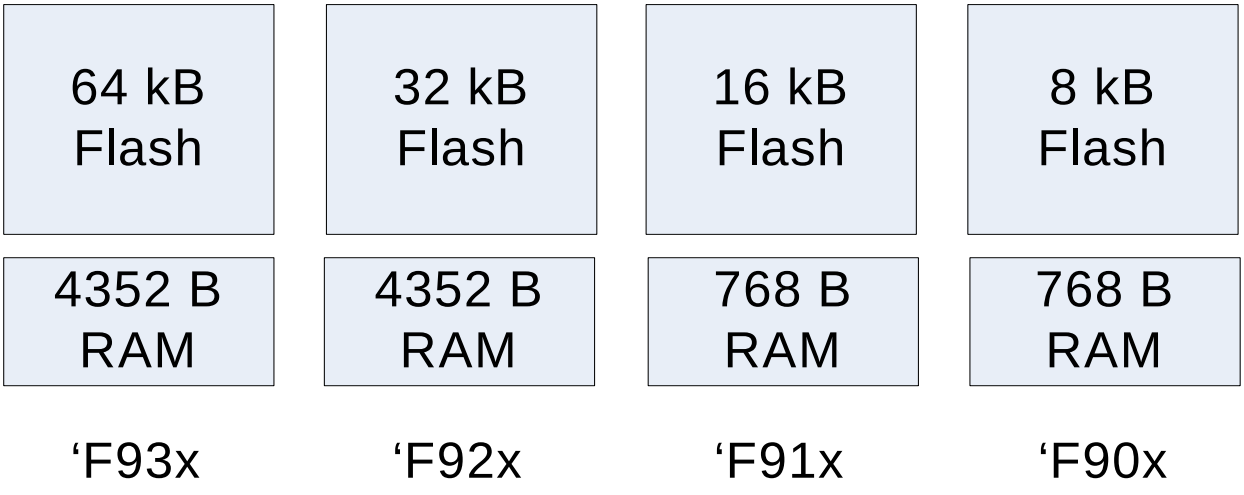

Figure 1. C8051F93x-C8051F90x MCU Family Memory Size Options

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3. Package Options

C8051F93x-C8051F90x devices are available in four package options. Table 1 describes the Flash sizes available in each package option. While the package option has little effect on device functionality, it may affect certain aspects of firmware such as the port initialization code.

Table 1. Flash Sizes Available by Package

Package	Available Flash Sizes
32-pin QFP	64 kB, 32 kB
32-pin QFN	64 kB, 32 kB
24-pin QFN	64 kB, 32 kB, 16 kB, 8 kB
24-pin QSOP	16 kB, 8 kB

Note: On the 64 kB and 32 kB versions of the 24-pin QFN package, port match capability is not available on P1.6.

4. Similarities

There are many similarities between devices in the C8051F93x-C8051F90x product family. The following list of peripherals have identical behavior between the various devices. Functions or peripherals not listed below have minor differences in implementation between devices in the C8051F93x-C8051F90x family.

- UART0
- SPI0 and SPI1
- IREF0 (when used in 6-bit mode)
- Comparator 0 and Comparator 1
- CIP-51
- Interrupt Handler
- Clocking Sources
- Timer 0, Timer 1, Timer 2, and Timer 3
- DC-DC Converter (when not using the “plus” features)
- PCA (when not using the “plus” features)
- ADC0 (when used in 10-bit mode)

5. Plus Features

C8051F912 and C8051F902 devices have a set of “plus” features that are not available on other devices in the C8051F93x-C8051F90x product family. These features include:

- 0.9 to 3.6 V continuous operating supply voltage.
- DC-DC converter bypass mode that saves power when the input voltage is higher than the programmed output voltage.
- 12-bit, 75 ksps mode on ADC0. 10-bit, 300 ksps functionality is retained.
- SmaRTClock with a built-in low frequency oscillator that only requires 250 nA of supply current.
- Buffered RTC clock output available in active and sleep mode.
- VBAT Low “warning” indicator with optional interrupt.
- Wakeup request output signal that can enable an external DC-DC converter or power switch.
- Ability to disable VBAT Supply Monitor to achieve a sleep mode current of 10 nA.

6. SFR Map

Devices in the C8051F93x-C8051F90x family share the same SFR address locations for most registers. This allows the C8051F930_defs.h and C8051F912_defs.h header files to be used interchangeably in applications that target devices in the C8051F93x-C8051F90x family. It also allows code developed on one device to be executed on any other device in the product family without modification.

There are a few minor differences between the C8051F930_defs.h and the C8051F912_defs.h header files. When writing software that targets multiple devices in the C8051F93x-C8051F90x family, the C8051F930_defs.h header file is recommended because it does not contain definitions for the “plus” registers which are only found on the ‘F912 and ‘F902 devices. When using this header file, a compiler error will be generated if any of the “plus” registers are used in the software.

Table 2 highlights the registers that are not identical on all devices in the C8051F93x-C8051F90x product family

Table 2. Select Registers with varying function

Register Name	Description of difference
Registers Found only in C8051F930_defs.h	
EMI0CF EMI0TC	Only apply to 32-pin devices. EMIF is not available on 24-pin devices.
P2SKIP P2MDIN	Only apply to 32-pin devices. On 24-pin devices, P2 does not have Crossbar or analog functionality.
Registers Found only in C8051F912_defs.h	
PMU0MD DC0MD IREF0CF	Only apply to the ‘F912 and ‘F902. Not available on the ‘F911 or ‘F901.
Registers with bit differences	
PCA0MD	On ‘F912 and ‘F902 devices, SmaRTClock/8 may be selected as the PCA timebase.
VDM0CN	On ‘F912 and ‘F902 devices, configuration bits for the VBAT supply monitor can be used to enable a VBAT low “early warning” interrupt.
DC0CF	On ‘F912 and ‘F902 devices, bit 7 enables the low power mode for the dc-dc converter. This low power mode is a “plus” feature.
ADC0AC	On ‘F912 and ‘F902 devices, bit 7 enables the 12-bit mode for ADC0. The 12-bit mode is a “plus” feature.
ADC0PWR	On ‘F912 and ‘F902 devices, bit 7 enables the low power mode for ADC0. This low power mode is a “plus” feature.
Indirect SmaRTClock registers with bit differences	
RTC0XCN	On ‘F912 and ‘F902 devices, bit 3 enables the SmaRTClock’s internal low frequency oscillator. The LFO is a “plus” feature.
RTC0PIN	On C8051F930/31/20/21 devices, this register is write only. It is R/W on all other devices.

7. Flash Memory

Devices in the C8051F93x-C8051F90x MCU family have in-system programmable Flash memory in various sizes. For 64 kB and 32 kB devices, Flash memory is organized in 1024 byte pages and the scratchpad size is 1024 bytes. For 16 kB and 8 kB devices, the Flash memory is organized in 512 byte pages and the scratchpad size is 512 bytes.

Flash security works the same way on all devices, however, the location of the lock byte will vary based on Flash size. Check the device datasheet for detailed information on Flash security and the location of the lock byte.

When creating applications that program their own Flash such as bootloaders, data loggers, etc., it is possible to write generic Flash management routines that operate on either 512 byte or 1024 byte Flash pages; however, this may not result in the most optimal memory usage. For example, in such a system, the logical Flash page size must be set to 1024 bytes. This can pose limitations on devices with a small Flash size. For example, an 8 kB device would only have 8 logical Flash pages. For larger Flash devices that have 1024 byte pages, each Flash page must be erased twice in order for the same code to support smaller devices that have 512 bytes per physical Flash page. In most applications, the most efficient method to support various devices is to use conditional compilation to tailor the Flash write/erase routines for each device.

8. RAM

All devices in the C8051F93x-C8051F90x family have 256 bytes of RAM mapped to internal DATA/IDATA space and either 4 kB (C8051F930/31/20/21) or 512 bytes (C8051F912/11/02/01) of RAM mapped to XDATA space. 32-pin devices (C8051F930/20) also have a multiplexed EMIF that supports memory mapping external devices with a 12-bit address space (8 kB address range, 4 kB on-chip and 4 kB off-chip).

9. DC-DC Converter

DC-DC converter functionality remains consistent across the C8051F93x-C8051F90x product family. ‘F912 and ‘F902 devices support additional “plus” modes that reduce supply current and allow an increased input voltage range. See the C8051F91x-90x data sheet for more information about these modes. All the standard modes are also supported on ‘F912 and ‘F902 devices.

10. Power Management Unit

The recommended procedure for entering and exiting low power modes described in “AN358: Optimizing Low Power Operation of the ‘F9xx” applies to all devices in the C8051F93x-C8051F90x family. When writing code that targets any device in the family, the entire procedure should be followed. When writing code that only targets a single power mode on a single device, some steps in the procedure may be omitted. The steps that may be omitted are outlined in AN358.

When porting existing code from C8051F930/31/20/21 devices to run on C8051F912/11/02/01 devices, it is important to note that C8051F912/11/02/01 devices require the execution of 4 NOP instructions immediately after waking up from sleep mode.

When porting existing code from C8051F912/11/02/01 devices to run on C8051F930/31/20/21 devices, it is important to note that C8051F930/31/20/21 devices require the CLKSEL register to contain a value of 0x14 when entering suspend or sleep mode and that a dummy write to the FLWR register is required after clearing the Flash one-shot timer BYPASS bit.

‘F912 and ‘F902 devices have a PMU0MD register which allows the SmaRTClock oscillator output to be routed to P0.2, a wake-up request signal to be routed to P0.3, or the VBAT supply monitor to be disabled to achieve a sleep mode current as low as 10 nA. The PMU0MD register is not available on other devices in the C8051F93x-C8051F90x family.

11. SMBus

When the hardware acknowledge feature is not used, the SMBus peripheral on all devices in the C8051F93x-C8051F90x family behave in an identical manner. If the hardware acknowledge feature is being used, then C8051F930/31/20/21 devices have errata items that need to be addressed with the proper software workaround as described in the C8051F930/31/20/21 errata sheet. The errata items do not apply to other devices in the C8051F93x-C8051F90x family, such as the C8051F912/11/02/01, and no software workaround is required to use the hardware acknowledge feature.

To write SMBus software that uses hardware acknowledge and is compatible with all devices in the product family, the workaround code should be included. The workaround code will function on devices that do not require the workaround. An example which implements the workaround code can be found in the C8051F93x/2x SMBus examples folder with the following default path:

C:\Silabs\MCU\Examples\C8051F93x_92x\SMBus

12. IREF0

When IREF0 is used in 6-bit mode, behavior is identical on all devices in the C8051F93x-C8051F90x family. ‘F912 and ‘F902 devices support a PWM Enhanced Mode which allows the IREF0 precision to be increased using a PCA channel configured to generate a PWM signal. To maintain code compatibility across all devices in the C8051F93x-C8051F90x family, use IREF0 in 6-bit mode.

13. PCA

The PCA functions identically across all devices in the C8051F93x-C8051F90x family, with the exception that ‘F912 and ‘F902 devices have the option to select SmaRTClock / 8 as a clock source for the PCA. For code compatibility across all devices in the C8051F93x-C8051F90x family, do not select SmaRTClock / 8 as the clock source for the PCA.

14. ADC

When used in 10-bit mode, the ADC on all devices in the C8051F93x-C8051F90x family behaves in the same way. ‘F912 and ‘F902 devices have an additional 12-bit mode that may be used to increase ADC resolution.

The maximum SAR clock on C8051F912/11/02/01 devices may be higher than the maximum SAR clock for C8051F930/31/20/21 devices. For code compatibility across all devices in the C8051F93x-C8051F90x family, use the ADC in 10-bit mode with the maximum SAR clock frequency specified for the C8051F930/31/20/21 devices.

15. SmaRTClock

The SmaRTClock behaves the same on all devices in the C8051F93x-C8051F90x when used with an external 32.768 kHz crystal. When used without a crystal (in self-oscillate or LFO mode), then there are differences.

To short XTAL3 and XTAL4 together on C8051F930/31/20/21 devices, write a value of 0xE7 to the write-only RTC0PIN indirect register. On C8051F912/11/02/01 devices, XTAL3 and XTAL4 can be shorted by reading the value of RTC0PIN, setting the most significant bit (value |= 0x80), then writing back the updated value. On any device, the XTAL3 and XTAL4 pins may also be shorted externally using a wire. In this case, the RTC0PIN register does not need to be modified. “F912 and ‘F901 devices also have an LFO mode that has a tighter tolerance than self-oscillate mode. See the C8051F91x-C8051F90x data sheet for details.

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