EFFECTS OF ESD PROTECTION DEVICES ON CAPACITIVE SENSING PERFORMANCE

1. Introduction

Silicon Laboratories' capacitive sensing techniques are compatible with external ESD protection methods. Designers should be aware of parasitic parameters in these circuits which affect capacitive sensing performance when implementing these protection methods. While most of the methods affect sensing performance in some way, in almost all cases an acceptable balance between performance, protection, and cost is easily achievable.

This application note describes several typical ESD protection techniques, their mode of operation, and the effects of commonly-introduced parasitic parameters on the different methods of capacitive sensing provided by Silicon Laboratories including charge rate measurement/relaxation oscillator (RO) methods and direct capacitive measurement (C2D).

2. Methods of ESD Failure and Innate Suppression

The human body model (HBM) and machine model (MM) for characterizing ESD immunity both charge a fixed capacitor to a test voltage and drive that into the device under test (DUT) through a characteristic impedance. For each test voltage, the amount of current is the same but the total amount of energy changes. At higher test voltages, a greater amount of energy must be safely dissipated. ESD protection circuits do not fail because of high voltage per se, they fail because their energy-dissipating characteristics are overloaded.

Almost all CMOS integrated circuits include high-voltage suppression circuits on input and output pins. These are active shunts which turn on whenever the pad voltage goes outside of the normal operating range. Effectiveness is limited mostly by their size: as they dissipate high-voltage energy, some of that energy is converted to heat. If these circuits get too hot, they melt. Also, these circuits have a maximum allowable current density which is also a function of their size. In an ESD event, as maximum current density is reached, the forward voltage potential across the circuit begins to rise. A highly-energetic ESD event can cause this potential to rise above the circuit's maximum allowable forward voltage, causing damage. After the IC's internal ESD protection circuits melt or break down (primary failure), any additional high energy is passed without attenuation to the device's internal circuits, damaging them as well (secondary failure).

Because of the speed of the ESD event (most last less than a microsecond), the damage from heating will tend to stay within the local region of the IC's ESD protection circuit. Also, the amount of energy any single protection circuit can carry is directly proportional to its size. ESD immunity tests introduce a single, measured amount of energy to the IC. As a result, if that energy can be spread between several protection circuits on the chip, the likelihood of damage is greatly reduced. To do this, additional internal ESD protection devices are spread around the device and shared by all of the pads. This method only works if the IC's metal interconnect for this circuit is capable of carrying the high currents, as much as several hundred milliamperes (for a very short period of time) through a narrow ribbon of metal less than a micron thick. Increasing the size of the internal protection devices and their wiring can consume a great deal of silicon area, making it very expensive to add high levels of internal ESD protection to an integrated circuit. For these reasons, the level of ESD protection designed into a product is a carefully considered trade-off: a direct function of the die area (and thus product cost) devoted to the internal protection circuits versus the cost of adding extra protection devices outside the capacitive sensing controller for those lines in the system which may be more vulnerable to ESD events.

Impedance of the integrated circuit's pin is a significant factor in the usefulness of external ESD protection circuits. External circuits can be designed to work synergistically with the complex impedance of the IC's pad circuitry and its packaging. The combination can provide an effective level of ESD control that is hard to achieve by using only on-chip, integrated protection circuitry.

Levels of ESD protection for CMOS circuits are based on a balance between product cost and expected requirements for protection in production and end-use. For applications requiring high ESD immunity on some lines, additional external protection can be provided using inexpensive methods. Properly designed, these

methods can work in synergy with the IC's package impedance and its internal ESD protection circuits to provide the most cost-effective method of ESD suppression. Silicon Laboratories' capacitive sensing products are fully compatible with the least expensive methods of suppression for highly-energetic ESD events.

3. Board-Level Methods of Suppression

3.1. Mechanical Methods of Suppression

Design for effective ESD suppression in any electronic system begins with a mechanical design that minimizes paths of travel by which high voltages can enter the system from the outside world. This is most difficult where the user is expected to touch the product, especially if there is a void or other opening in the packaging. Mechanical switches and control potentiometers are classic system entry points for ESD. Changing from mechanical controls to capacitive touch controls eliminates the voids for these traditional ESD entry paths. Touch control surfaces that are designed to fit into a panel opening require barrier shielding similar to that used for dome-switch panels.

Physical techniques for routing signals near possible ESD sources in any electronic system should be observed in products using capacitive sensing circuits. These techniques do not generally affect capacitive sensing performance except where they may add bulk capacitance and interference to the lines being routed. Adding ground shields to signal lines will add capacitance to ground; this added capacitance will appear in the measurement results as a fixed offset.

Large increases in the base capacitance of the touch sense point can swamp the small effect of a finger touch that might be sensed by RO and C2D methods. An increase in base capacitance can cause a decrease in the sample data's signal-to-noise ratio, meaning lower confidence in the results.

For conversion methods with a hard upper limit on total capacitance, adding large amounts of bulk capacitance may also raise the untouched capacitance level out of sensing range. For this reason, the systems designer should reduce stray capacitances and reduce them where possible.

3.2. Electronic Methods of Suppression

In the predominant method of external suppression, a small resistance is placed in series with the input pin to the IC. More demanding applications will supplement this by connecting external protection diodes from the input pin to the power supply. Other methods commonly employed for automotive, telecom or other application-specific situations include multi-pole low-pass filtering, inductive or optical coupling or air-gap discharge shunting. Evolving ESD suppression techniques also apply many new products including SCR/diode arrays, polymeric-gap shunts and improved options for existing products such as TVS and Schottky diodes.

Understanding and controlling parasitic parameters such as leakage and bulk capacitance are key to acceptable capacitive sensing performance. The same analysis can be used in the application of other newer or less-common suppression techniques. Highly-suppressive ESD control methods that break ac and/or dc coupling (such as inductive or optical coupling) are not compatible with capacitive sensing applications.

4. Series Resistance Protection

The most common method of external ESD protection is adding a small series resistance in-line between the source of ESD energy and the integrated circuit pin to be protected. Somewhat counter-intuitively, a resistance as small as 50 Ω can double the ESD immunity of a CMOS IC. Higher immunity is possible; a higher level of protection is somewhat proportional to increased series resistance.

This method works for two reasons. First, the series resistance works with the IC's parasitic pin capacitance (typically 5 to 10 pF) to create a single-pole low pass filter with a cutoff frequency below 1 GHz. This causes the series resistor to attenuate a majority of an ESD event's high-frequency energy (as much as 90% of the rising-edge power in an HBM discharge). Second, when the IC's protection circuits are operating normally, their impedance is very low (on the order of tens of ohms or less). This low resistance works with the series resistance to create a voltage divider, so that the high voltage from an ESD event can only bias the IC's built-in protection circuits with a portion of the total ESD voltage. This attenuation is in addition to rising-edge filtering. The sum of these effects from a simple external series resistor dramatically improves ESD performance in a demanding application.

All of the capacitance sensing methods used by Silicon Laboratories are capable of accurately sensing a capacitive load on the opposite end of a series resistance of 200 Ω (or greater). For RO, the additional series resistance causes a delay in rise and fall times, which slows oscillation by a fixed amount. This frequency offset can be removed in the normal characterization process. The decrease in rate will not significantly affect sensitivity.

The C2D circuit operates differently. It drives charge into the capacitance under test and reads the resulting voltage. For this circuit, an added series resistance between the sensing circuit and the test capacitor creates a voltage offset as the capacitor under test is being charged. This appears in the test results as a small increase in bulk capacitance, but it is a constant offset that can be removed during characterization.

Higher levels of external series resistance give better protection. As the current-carrying capacity of the IC’s internal ESD protection circuits tops out, its resistance increases causing an increase in the ESD voltage into the IC. Higher levels of external series resistance will decrease the current an ESD event can drive into the IC. The amount of series resistance can be selected by balancing ESD suppression levels and capacitive sensitivity required.

5. Additional Protection Diodes

ESD susceptible lines are sometimes protected by attaching diodes to shunt the high energy from a discharge event before it can reach an IC's input pin. These diodes may either pass the current to the power supply rails or they may internally dissipate the unwanted power. The diodes that may be added to an ESD-susceptible line are similar to the diodes built into an IC for protection, but they are fabricated differently. External diodes have their own significant advantages: they can switch faster and at a lower excursion voltage than the IC's own diodes; they can have much better connections to the supply rails, and can carry more power. Their effects on circuit operation are different from internal diodes, because the connections used internally cannot be achieved with external devices.

Two styles of diode protection are typically used. Zener diodes or transient voltage suppression (TVS) avalanche diodes can be placed between an input signal and ground. In this configuration, the diode protects the CMOS input by reverse conduction whenever its voltage rises above the specified diode breakdown voltage. Negative ESD excursions are shunted to ground through normal diode action. In another configuration, diode pairs (typically Schottky diodes due to their lower forward voltage drop) are placed between the input line and the power and ground rails. These devices protect the CMOS input by normal diode conduction whenever the input line voltage moves outside of the range of the power supply rails. Although small and inexpensive, an external diode circuit can be two to four times larger and four times more expensive than adding only a series resistance.

Diodes placed on capacitive sensed lines present the same problems to capacitive sensing circuits that they do with any analog circuit input: they can be highly capacitive (over 100 pF) and leaky. Some Schottky pairs leak over 20 µA; some avalanche diodes leak over 1 mA when operated near their reverse-standoff voltage (generating significant noise voltage as well). Although these given numbers are for the least suitable devices, the most commonly-used Schottky and TVS diodes have parasitic parameters that make them unacceptable for use in capacitive sensing circuits. If the diode circuit can be designed to add only a very small amount of additional capacitance, capacitance sensing circuits can be adjusted to match. This is because compensation mechanisms are usually built into these circuits for adaptation to the naturally-occurring changes in capacitance that result from environmental changes. Still, leakage and bulk capacitance can create problems for any sort of capacitive sensing method, some more than others.

The added capacitance of protection diodes adds an offset to the capacitance measurement. As explained in the section on shielding capacitance, an increase in the untouched capacitance can swamp the small effect of a finger touch, resulting in a lower signal-to-noise ratio and lower confidence in the sampled results. Properly designed diode shunts only moderately affect RO and C2D methods of conversion. For conversion methods with a hard upper limit on total capacitance, adding large amounts of bulk capacitance may also raise the untouched capacitance level out of sensing range. To retain maximum sensitivity where protection diodes must be used, it is essential to specify devices with extremely low capacitance.

External diodes with high reverse leakage make the test capacitance look larger because their leakage drains test current from the circuit. This disappearing test current (which should be filling the capacitance under test) has no dV/dt effect on the test load. As diode leakage currents approach the level of the test current, the apparent load capacitance approaches infinity. Also, the amount of current required to detect a 0.1 pF change in capacitance is less than 20 pA, many orders of magnitude less than the leakage current for some protection diodes. For this reason, where external diodes must be used, it is essential to specify devices with extremely low reverse leakage for RO and C2D systems.

A device such as the BAS70-04 diode pair has both low capacitance (2 pF) and low leakage (below 0.1 µA), reducing the problems that come from using Schottky protection diodes in RO and C2D capacitive sensing applications. Using a diode pair such as the BAS70-04 should effect a small increase (3% to 8%) in the base (untouched) level of the measured capacitance, and a modest decrease (–6 dB) in the sensitivity of the detector for C2D measurements.

6. Summary

With appropriate design, the capacitive sensing techniques of Silicon Laboratories' MCU products can be used concurrently with the most common ESD protection methods. The use of series resistance and Schottky clamps is not only possible but encouraged in situations where ESD susceptibility is expected to be high and suppression by other methods is not as practical.

Almost every method of capacitive sensing is affected by the addition of ESD protection circuits. The sensitivity and range of Silicon Laboratories' capacitive sensing solutions makes it possible to use many of these methods as long as the effects of their parasitic circuit elements are properly considered.

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