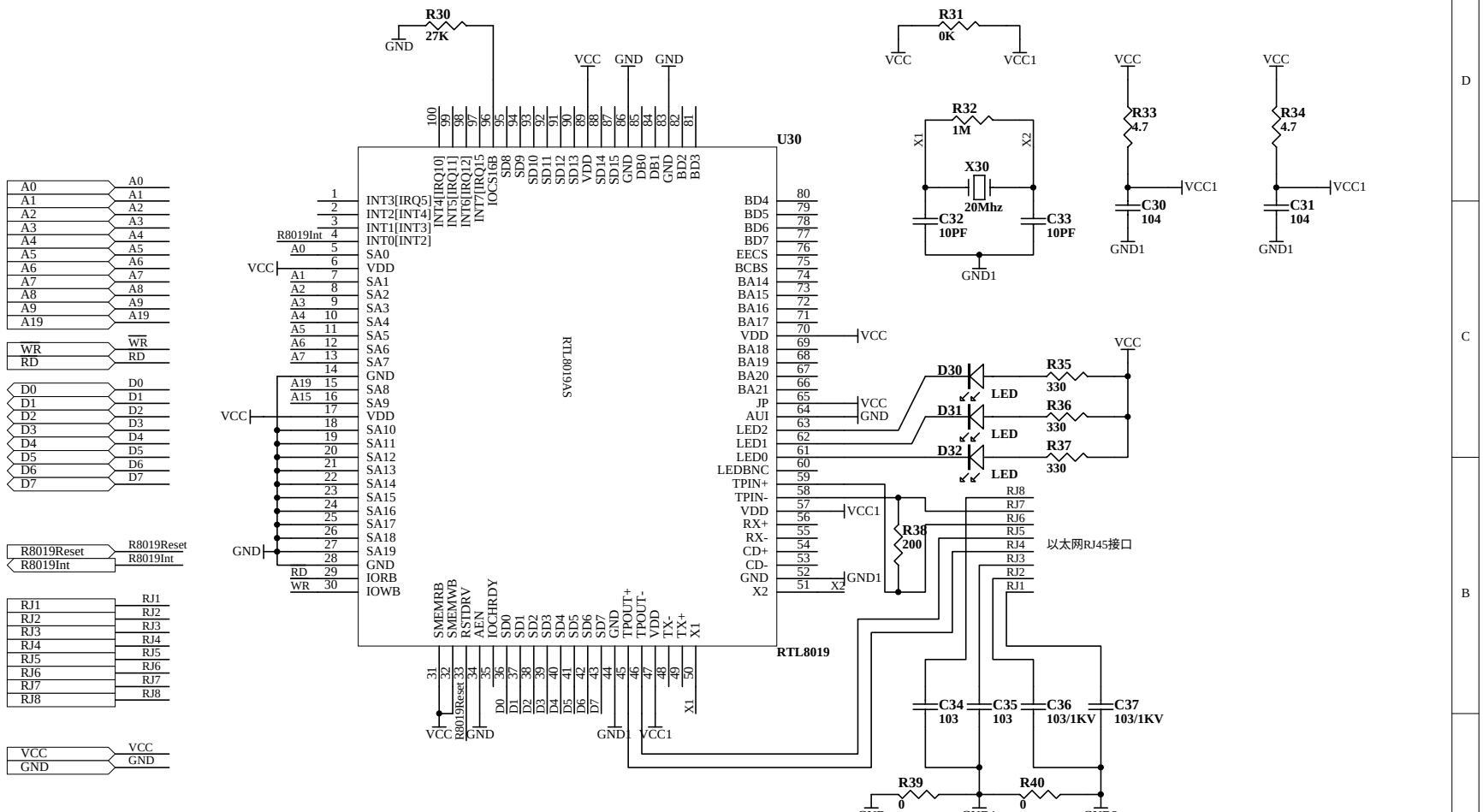

Title	核心模块原理图 4	
Size: A4	Number	Revision
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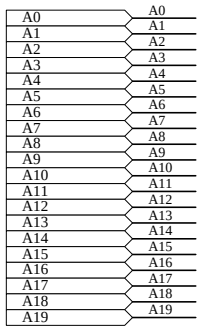
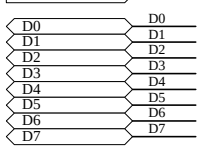
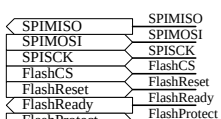
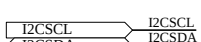
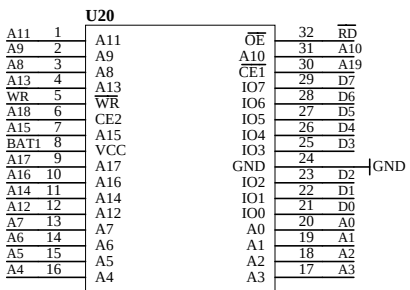
File: C:\Document backup\Tcpip\TCPIP.DDB	Drawn By:	







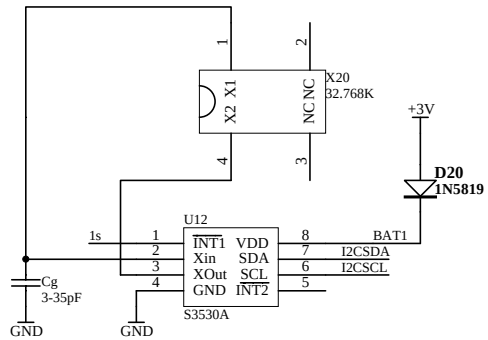


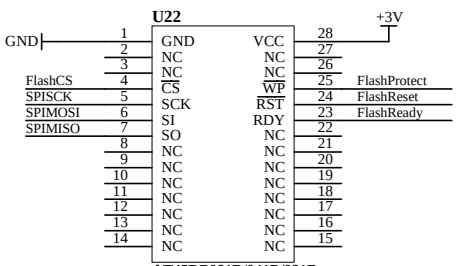


IS62LV2568

IC62LV5128 IC62LV2568 IC62LV1024

SRAM 说明
系统可选择的容量为 128K 256K 512K
对应芯片分别为
128K-->ISSI的IS62LV1024或ICSI的IC62LV1024
256K-->ICSI的IC62LV2568
512K-->ISSI的IS62LV5128或ICSI的IC62LV5128
芯片封装为32-Pin TSOP
地址分配
128K-->分两段:
BANK0 A19A18A17A16=01X0
BANK1 A19A18A17A16=01X1
256K-->分四段:
BANK0 A19A18A17A16=0100
BANK1 A19A18A17A16=0101
BANK2 A19A18A17A16=0110
BANK3 A19A18A17A16=0111
512K-->分八段:
BANK0 A19A18A17A16=0000
BANK1 A19A18A17A16=0001
BANK2 A19A18A17A16=0010
BANK3 A19A18A17A16=0011
BANK4 A19A18A17A16=0100
BANK5 A19A18A17A16=0101





AT45DB081B/041B/021B

8Mbit/4Mbit/2Mbit

1M/512K/256K

Title: 核心模块原理图 3		
Size: A4	Number:	Revision:
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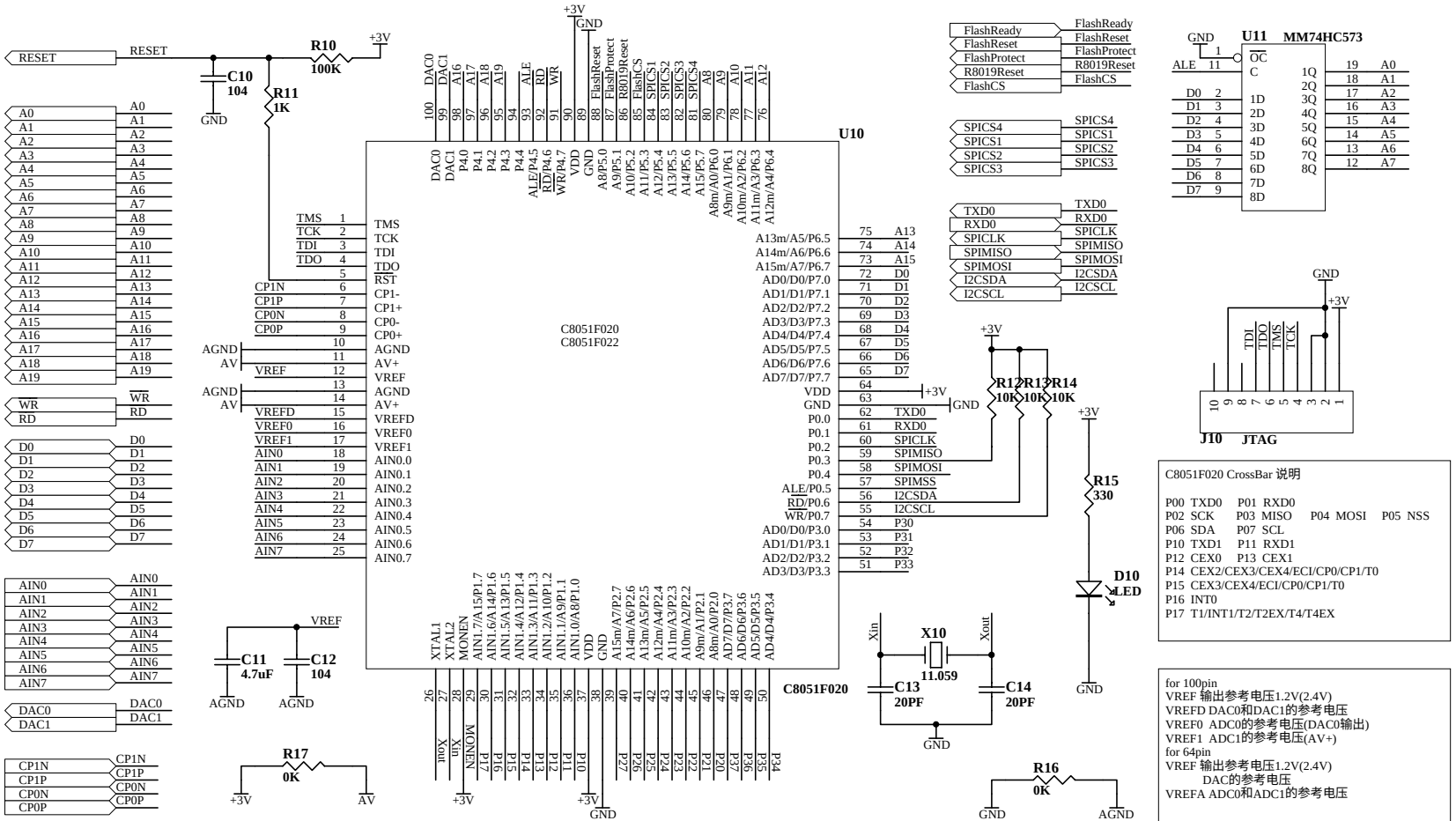
U10
C8051F020
C8051F022
C8051F020
U11 MM74HC573
J10 JTAG
R10 100K
R11 1K
C10 104
C11 4.7uF
C12 104
R12 10K
R13 10K
R14 10K
R15 330
D10 LED
X10 11.059
C13 20PF
C14 20PF
R16 0K
R17 0K
R18 0K
C8051F020 CrossBar 说明
P00 TXD0 P01 RXD0
P02 SCK P03 MISO P04 MOSI P05 NSS
P06 SDA P07 SCL
P10 TXD1 P11 RXD1
P12 CEX0 P13 CEX1
P14 CEX2/CEX3/CEX4/ECI/CP0/CP1/T0
P15 CEX3/CEX4/ECI/CP0/CP1/T0
P16 INT0
P17 T1/INT1/T2/T2EX/T4/T4EX
for 100pin
VREF 输出参考电压1.2V(2.4V)
VREFD DAC0和DAC1的参考电压
VREF0 ADC0的参考电压(DAC0输出)
VREF1 ADC1的参考电压(AV+)
for 64pin
VREF 输出参考电压1.2V(2.4V)
DAC的参考电压
VREFA ADC0和ADC1的参考电压
Title
核心模块原理图 2
Size A4
Number
Revision
Date: 25-Dec-2002
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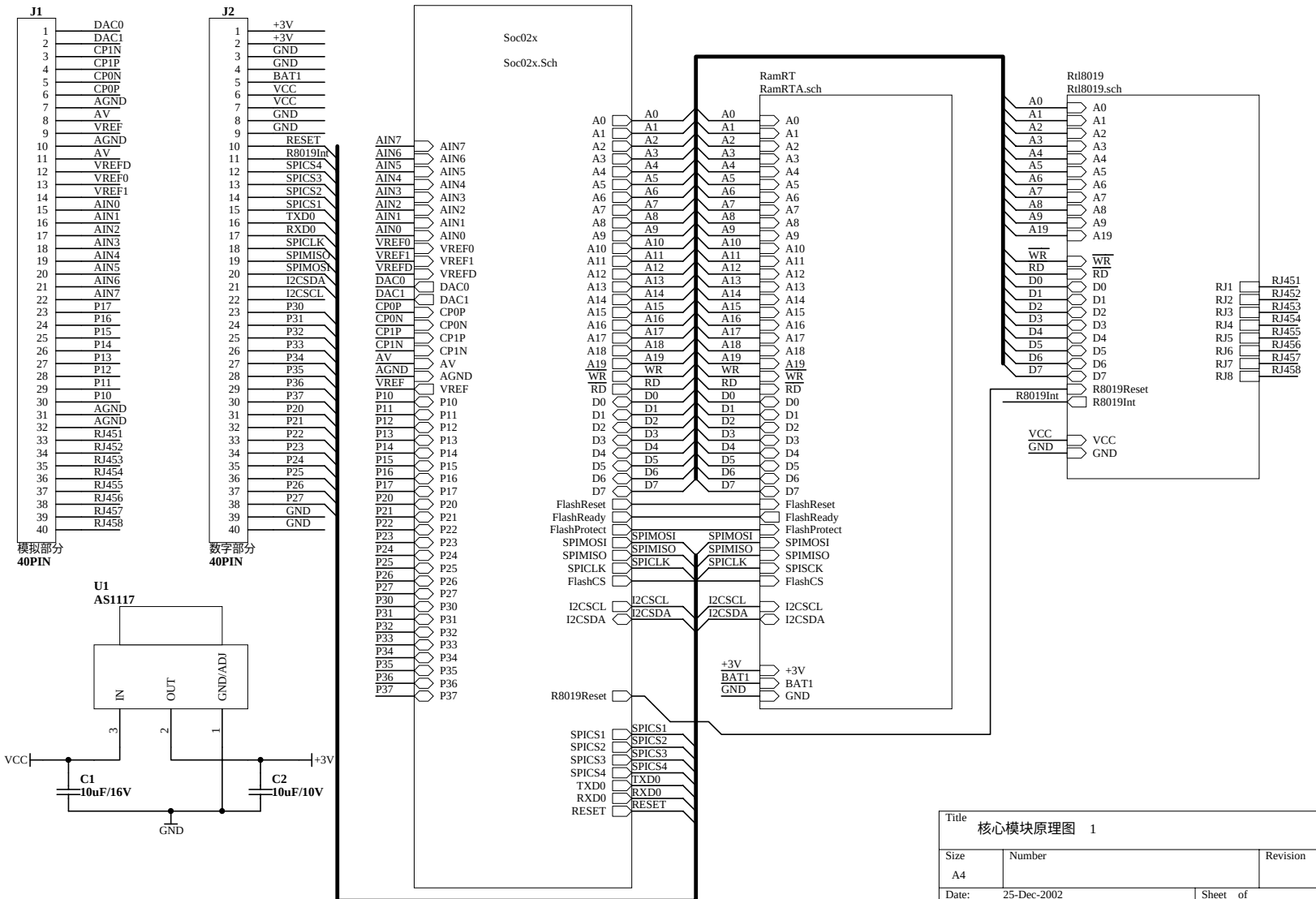
File: C:\Document_backup\Tcpip\TCPIP.DDB
Drawn By:


J1
1 DAC0
2 DAC1
3 CP1N
4 CP1P
5 CP0N
6 CP0P
7 AGND
8 AV
9 VREF
10 AGND
11 AV
12 VREFD
13 VREF0
14 VREF1
15 AIN0
16 AIN1
17 AIN2
18 AIN3
19 AIN4
20 AIN5
21 AIN6
22 AIN7
23 P17
24 P16
25 P15
26 P14
27 P13
28 P12
29 P11
30 P10
31 AGND
32 AGND
33 RJ451
34 RJ452
35 RJ453
36 RJ454
37 RJ455
38 RJ456
39 RJ457
40 RJ458
模拟部分
40PIN
J2
1 +3V
2 +3V
3 GND
4 GND
5 BAT1
6 VCC
7 VCC
8 GND
9 GND
10 RESET
11 R8019Int
12 SPICS4
13 SPICS3
14 SPICS2
15 SPICS1
16 TXD0
17 RXD0
18 SPICLK
19 SPIMISO
20 SPIMOSI
21 I2CSDA
22 I2CSCL
23 P30
24 P31
25 P32
26 P33
27 P34
28 P35
29 P36
30 P37
31 P20
32 P21
33 P22
34 P23
35 P24
36 P25
37 P26
38 P27
39 GND
40 GND
数字部分
40PIN
Soc02x
Soc02x.Sch
RamRT
RamRTA.sch
Rtl8019
Rtl8019.sch
U1
AS1117
IN
OUT
GND/ADJ
VCC
+3V
GND
C1
10uF/16V
C2
10uF/10V
R8019Reset
FlashReset
FlashReady
FlashProtect
SPIMOSI
SPIMISO
SPICLK
FlashCS
I2CSCL
I2CSDA
SPICS1
SPICS2
SPICS3
SPICS4
TXD0
RXD0
RESET
BAT1
Title
核心模块原理图 1
Size
A4
Number
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Drawn By: