METANOIA

MT3302 Preliminary Datasheet

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Revision History

Revision	Description
1.0	First revision of this document.
1.01	Removed less important data from Thermal Characteristics chapter.

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Chapter 1

General Description

1.1 Description of MT3302

The MT3302 is a highly integrated Analog Front End (AFE) for VDSL2 and ADSL1/2/2+ application which provides all analog functions necessary for receiving and transmitting xDSL data according to ITU-T, ETSI and ANSI. The high integrity with low distortion and noise reduces the need for complex and costly external components. A serial control interface allows the software programming of various functional blocks. Power back off combined with power down for some blocks provides the flexible power saving policy. An on-chip clean up PLL provides all the required internal clocks. As single port device it is intended to be used in customer premises equipment (CPE). The full 8MHz/12MHz/17MHz/30MHz bandwidth support in downstream and upstream direction also allows the use in central office (CO).

In transmit path, it includes an interpolation filter, a 14-bit DAC, a smoothing LPF and a high performance line driver. The transmit signal bandwidth can be as wide as 30MHz with high linearity. A programmable attenuation is designed from 0dB down to -14.5dB in 0.5dB steps which is designed for power back off. The internal line driver provides sufficient power settings required by the xDSL standards for PSD masks.

The receive path consists of a Variable Gain Amplifier (VGA), an anti-aliasing LPF, a HPF, a sophisticated 14-bit ADC and a decimation filter. The VGA has a minimum gain setting of -6dB and a maximum of 51dB. The HPF cutoff frequency can be set from 32kHz to 3MHz which do more echo rejection from transmit band.

The AFE interface provides a loopback function which loops the data at the DAC input directly back to the ADC output.

The MT3302 AFE provides highly integrated solution for xDSL. It is available in a space saving 64-pin QFN package and is specified for the industrial (-40C to +85C) temperature range.

Chapter 2

Electrical Characteristics

2.1 Electrical Characteristics for MT3302

2.1.1 Absolute Maximum Ratings and Environmental Limitations

Parameter	Symbol	Min	Max	Unit	Conditions
Analog supply voltage DAC,LD	V_{DD-A1}	-0.3	6	V	Note 1
Analog supply voltage VGA, ADC, PLL	V_{DD-A2}	-0.3	3	V	Note 1
Digital core supply voltage	V_{DD-D}	-0.3	3	V	Note 1
I/O-supply voltage	$V_{DD-I/O}$	-0.3	3.8	V	Note 1
Ambient temperature	T_{AMB}	0	85	$°C$	Note 1
Storage Temperature	T_{STG}	-65	125	$°C$	Note 1
Junction Temperature	T_J	-40	125	$°C$	Note 1
ESD classification	V_{ESD}	-	2	kV	Note 1,2

Table 2.1: Absolute Maximum Ratings and Environmental Limitations.

Notes:
1. Operating conditions outside the min-max ranges specified may cause permanent device failure. Exposure to conditions near the min or max limits for extended periods may impair device reliability.
2. Test method for ESD per JEDEC JESD22-A114-B.

2.1.2 Operating Conditions and Power Requirements

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Analog supply voltage DAC, LD	V_{DD-A1}	4.75	5	5.25	V	
Analog supply voltage VGA,ADC,PLL	V_{DD-A2}	2.375	2.5	2.625	V	
Digital core supply voltage	V_{DD-D}	2.375	2.5	2.625	V	
I/O-supply voltage	$V_{DD-I/O}$	1.1	-	3.5	V	Note 1
Ambient temperature	T_{AMB}	-40	25	85	$°C$	
Power consumption	$P_{SUPPLY1}$	-	1.7	-	W	VDSL2 30a, Note 2
Power consumption	$P_{SUPPLY1}$	-	1.5	-	W	VDSL2 17a, Note 2
Power consumption	$P_{SUPPLY1}$	-	1.4	-	W	ADSL2+, Note 2

Table 2.2: Operating Conditions and Power Requirements

Notes:
1. The supply voltage for the digital I/O's can take any voltage between 1.1V and 3.5V.
2. The exact power consumption is depending on the used loop length.

2.1.3 Transmit Path Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input data rate	DR_{TX}	35.328	-	70.656	MS/s	Different data rate for different profile.
Resolution	Res_{TX}	-	14	-	$bits$	
Max. output voltage	$V_{outmaxTX}$	8	-	-	V_{dpp}	0dBfs, PBO=0dB, at the load impedance derived from the concept of synthesized impedance
Common mode output voltage	$V_{outCMTX}$	-	$V_{DD-A1}/2$	-	V	
Max. output current	$I_{outmaxTX}$	800	-	-	mA	
Output noise in-band	PSD_{IBLTX}	-	-128/-130	-	dBm/Hz	line referred, 138 kHz ... 30 MHz, -128 dBm/Hz for VDSL profile, -130 dBm/Hz for ADSL profile
Output noise out-of-band	PSD_{OBLTX}	-	-128	-	dBm/Hz	line referred, >30MHz
Signal BW lower corner frequency	f_{lowTX}	-	10	-	kHz	
Signal BW upper corner frequency	f_{highTX}	30	-	-	MHz	
Passband ripple	PBR_{TX}	-	0.5	-	dB	
Total harmonic distortion	THD_{TX-3}	-	-	-70	dBc	$f_{in} = 1, 4, 6, 10MHz$ @ -3dBfs harmonic in band
Missing band depth	MBD_{TX}	-	55	-	dB	
Power back off range	GR_{PBO}	-14.5	-	0	dB	
PBO step size	SS_{PBO}	-	0.5	-	dB	
PBO accuracy	SS_{PBOADJ}	-0.5	-	0.5	dB	

Table 2.3: Transmit Path Characteristics.

2.1.4 Receive Path Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Output data rate	DR_{RX}	35.328	-	70.656	MS/s	Different data rate for different profile.
Resolution	Res_{RX}	-	14	-	$bits$	
Max. input voltage	$V_{inmaxRX}$	-	3.6	-	V_{dpp}	VGA gain = 0dB
VGA gain range	GR_{VGA}	-6	-	51	dB	
VGA step size	SS_{VGA}	-	2 1	- -	dB dB	$Gain = -6dB - - + 12dB$ $Gain = +12dB - - + 51dB$
VGA accuracy	SS_{VGAADJ}	-0.5	-	0.5	dB	
Signal BW lower corner frequency	f_{lowRX}	-	32	-	kHz	
Signal BW upper corner frequency	f_{highRX}	30	-	-	MHz	
Passband ripple	PBR_{RX}	-	1	-	dB	
Total harmonic distortion	THD_{RX-3}	-	-	-70	dBc	$f_{in} = 1, 4, 6, 10MHz$ @ -3dBfs harmonic in band
Input noise	PSD_{LRX}	-	-149	-	dBm/Hz	line referred, tested at the VGA gain > 30 dB condition, the attenuation caused by hybrid circuit in RX path is assumed to be 12 dB.
Missing band depth	MBD_{RX}	-	55	-	dB	

Table 2.4: Receive Path Characteristics.

2.1.5 Xtal Oscillator

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Frequency	f_{OSC}	-	35.328	-	MHz	
Capacitor trimming range	$\triangle C_{trim}$	6	-	38	pF	

Table 2.5: Xtal Oscillator

2.1.6 Digital I/O's

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input high	V_{IH}	$V_{DD-I/O} * 0.8$	-	-	V	
Input low	V_{IL}	-	-	$V_{DD-I/O} * 0.2$	V	
Output high	V_{OH}	$V_{DD-I/O} - 0.1$	-	-	V	
Output low	V_{OL}	-	-	0.1	V	
Input capacitance	C_{in}	-	-	5	pF	
Load capacitance	C_{load}	-	-	30	pF	60MHz signal

Table 2.6: Digital I/O's

2.1.7 I/O Timing

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Clock period	t_{CLK30}	-	28.306	-	ns	$CLK30 = 1/f_{OSC}$
Clock duty cycle	DC	-	50	-	%	CLK30
Rise/fall time	t_R/t_F	-	2.5	-	ns	20% to 80%
Invalid time ADC,DOUT	$t_{InvalidADC}$	0	-	6	ns	See Figure 2.1
Setup time DAC	$t_{SetupDAC}$	10	-	-	ns	
Hold time DAC	$t_{HoldDAC}$	0	-	-	ns	

Table 2.7: I/O Timing.

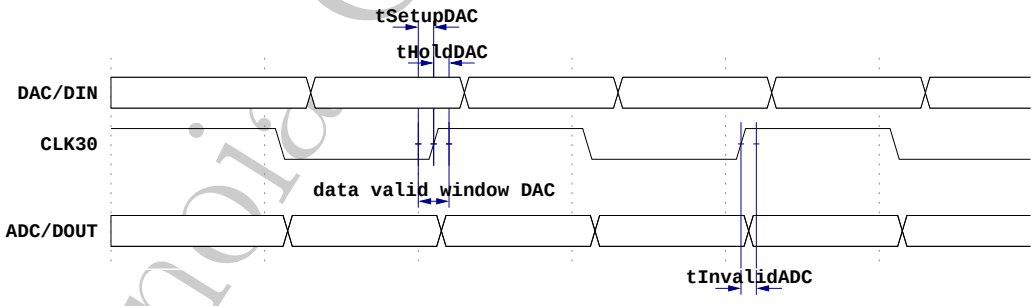

Figure 2.1: I/O Timing Diagram.

Chapter 3

Thermal Characteristics

3.1 Thermal Characteristics for MT3302

3.1.1 Thermal Resistance

Parameter	Symbol	Value	Unit	Conditions
Junction to ambient temperature	θ_{ja}	24.38	$°C/W$	4 layer PCB, 0m/s airflow
Junction to case temperature	θ_{jc}	2.41	$°C/W$	4 layer PCB, 0m/s airflow

Table 3.1: Thermal Resistance

Chapter 4

Pin Configuration

4.1 Pin Description for MT3302

Pin	Symbol	Pad Type	Description
1	LDFBP	AI	Internal LD feedback input P
2	LDFBN	AI	Internal LD feedback input N
3	LDINN	AI	Internal LD input N for external signal
4	LDINP	AI	Internal LD input P for external signal
5	POFIOUTP	AO	TX post-filter output P for external LD
6	POFIOUTN	AO	TX post-filter output N for external LD
7	DAC0	DI	Data 0, interpolator/DAC input
8	DAC1	DI	Data 1, interpolator/DAC input
9	DAC2	DI	Data 2, interpolator/DAC input
10	DAC3	DI	Data 3, interpolator/DAC input
11	DAC4	DI	Data 4, interpolator/DAC input
12	VDD2.5(DIG)	Supply	Digital power supply (2.5V)
13	VDD2.5(DAC)	Supply	Analog power supply, DAC (2.5V)
14	DAC5	DI	Data 5, interpolator/DAC input
15	DAC6	DI	Data 6, interpolator/DAC input
16	DAC7	DI	Data 7, interpolator/DAC input
17	DAC8	DI	Data 8, interpolator/DAC input
18	DAC9	DI	Data 9, interpolator/DAC input
19	DAC10	DI	Data 10, interpolator/DAC input
20	DAC11	DI	Data 11, interpolator/DAC input
21	DAC12	DI	Data 12, interpolator/DAC input
22	DAC13	DI	Data 13, interpolator/DAC input
23	VDD2.5(PLL)	Supply	Analog power supply, bandgap REF/DCXO/PLL (2.5V)
24	XTAL1	AI	Oscillator crystal pin 1
25	XTAL2	AI	Oscillator crystal pin 2
26	VDD5	Supply	Analog power supply, bandgap REF/switches/DAC (5.0V)
27	VDDxIF	Supply	Digital power supply, data interface (3.3V)
28	ADC13	DO	Data 13, ADC/decimator output
29	ADC12	DO	Data 12, ADC/decimator output
30	ADC11	DO	Data 11, ADC/decimator output
31	ADC10	DO	Data 10, ADC/decimator output
32	ADC9	DO	Data 9, ADC/decimator output
33	ADC8	DO	Data 8, ADC/decimator output
34	ADC7	DO	Data 7, ADC/decimator output
35	EXTLDON	DO	External LD power on
36	VDD5IF	Supply	Digital power supply (5.0V)
37	VDD2.5(DIG)	Supply	Digital power supply (2.5V)

Pin	Symbol	Pad Type	Description
38	CLK30	DO	Clock 35MHz out
39	VDDxIF	Supply	Digital power supply, data interface (3.3V)
40	VDD2.5(ADC)	Supply	Analog power supply, ADC (2.5V)
41	ADC6	DO	Data 6, ADC/decimator output
42	ADC5	DO	Data 5, ADC/decimator output
43	ADC4	DO	Data 4, ADC/decimator output
44	ADC3	DO	Data 3, ADC/decimator output
45	ADC2	DO	Data 2, ADC/decimator output
46	ADC1	DO	Data 1, ADC/decimator output
47	ADC0	DO	Data 0, ADC/decimator output
48	VDDxIF	Supply	Digital power supply, data interface (3.3V)
49	SERDATAOUT	DO	Serial control interface data output
50	SERDATAIN	DI	Serial control interface data input
51	RSTB	DI	AFE reset input
52	VDD2.5(VGA)	Supply	Analog power supply, VGA (2.5V)
53	VGAINP	AI	VGA input P
54	VGAINN	AI	VGA input N
55	VGAINPATT	AI	VGA input P for application with attenuation on PCB
56	VGAINNATT	AI	VGA input N for application with attenuation on PCB
57	OUT_P1	AO	Positive line driver output 1
58	VDD_LD	Supply	Analog power supply, line driver (5.0V)
59	VDD_LD	Supply	Analog power supply, line driver (5.0V)
60	OUT_N1	AO	Negative line driver output 1
61	OUT_P2	AO	Positive line driver output 2
62	VDD_LD	Supply	Analog power supply, line driver (5.0V)
63	VDD_LD	Supply	Analog power supply, line driver (5.0V)
64	OUT_N2	AO	Negative line driver output 2

Table 4.1: Pin Description

Note: Package bottom pad is used as the ground pin as well as the heat sink function. Therefore, it must be assigned and soldered carefully to the PCB.

4.1.1 Pinout Diagram

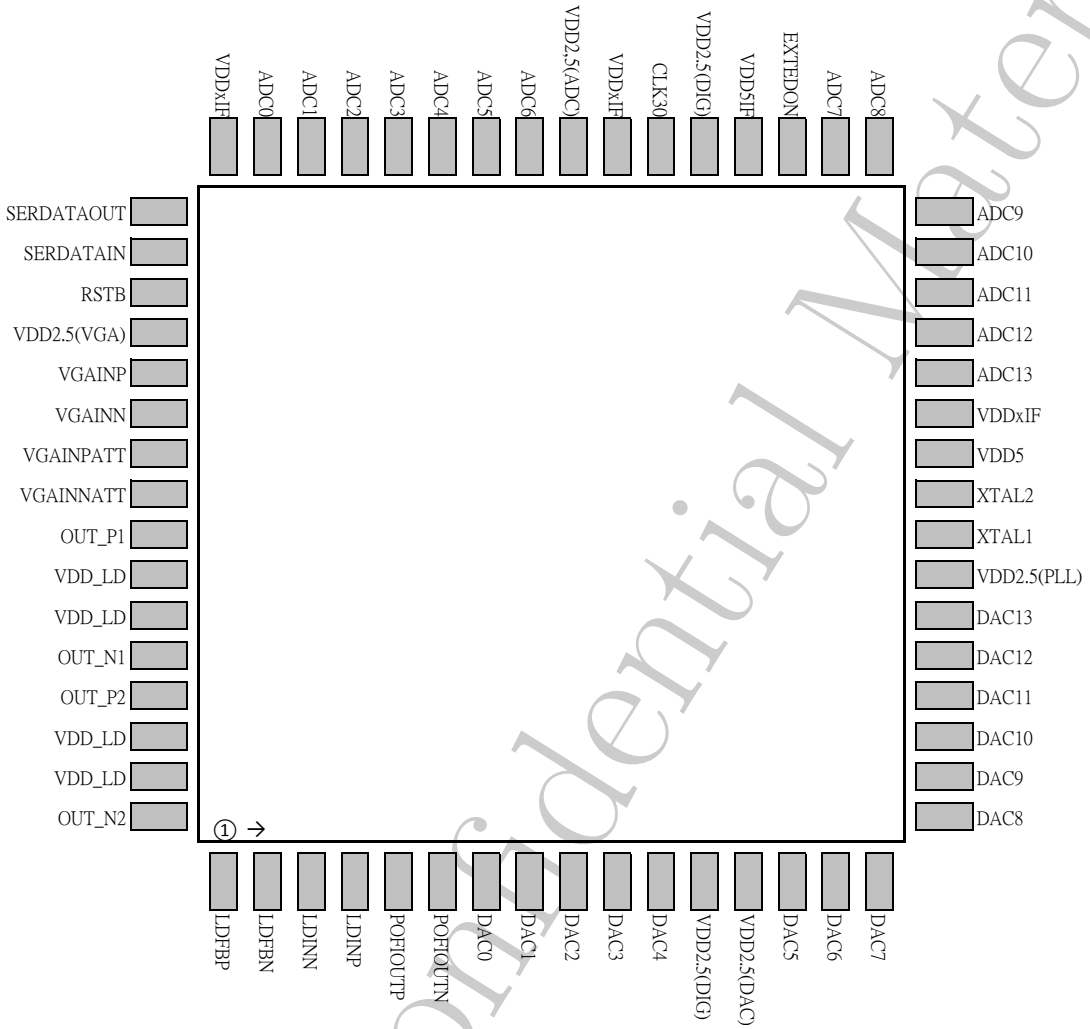

Figure 4.1: Pinout diagram for MT3302

Chapter 5

Package

5.1 Package Information for MT3302

The MT3302 is packaged in a 9mm×9mm, 64-pin Quad Flat No-lead package (QFN) suitable for surface mounting, as shown in figure 5.1.

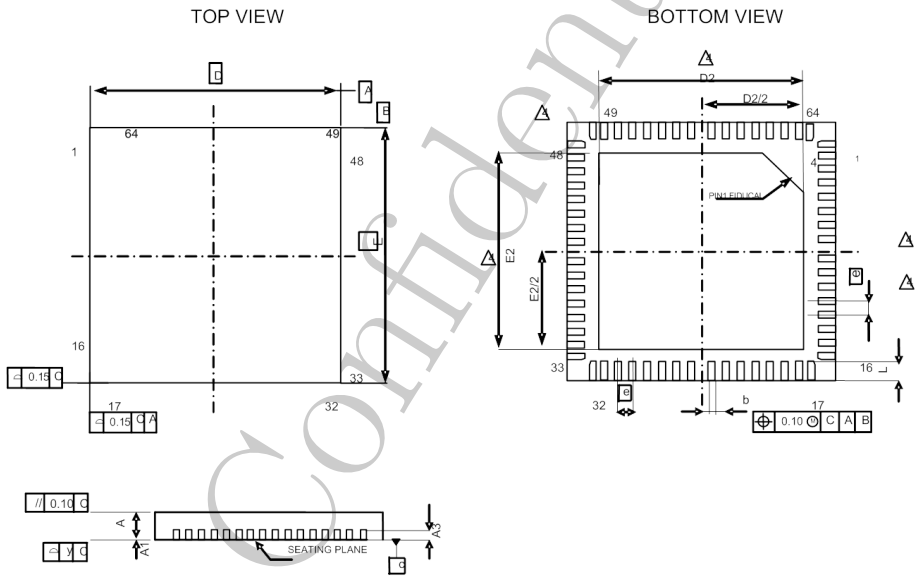

Figure 5.1: Package Diagram

Symbol	Dimension (mm)			Dimension (MIL)		
	MIN	NOM.	MAX	MIN	NOM	MAX
A	0.7	0.75	0.80	27.6	29.5	31.5
A1	0	0.02	0.05	0	0.79	1.97
A3		0.203 REF			8 REF	
b	0.18	0.25	0.28	7.1	9.8	11.0
D		9.00 BSC			354.3 BSC	
D2	7.20	7.30	7.40	283	287	291
E		9.00 BSC			354.3 BSC	
E2	7.20	7.30	7.40	283	287	291
e		0.50 BSC			19.7 BSC	
L	0.35	0.40	0.45	13.8	15.7	17.7
y		0.08			3.15	

Table 5.1: Package Dimentions

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. REFER TO JEDEC STD. MO-220 WMMD.
3. DIMENSION “b” APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL TIP.
4. LEADFRAME MATERIAL IS OLIN194 AND THICKNESS IS 0.203mm (8 MIL).

Chapter 6

Ordering Information

6.1 Ordering Information for MT3302

Part Number:
MT3302GN-xy: 1 port xDSL AFE chip with 64-QFN package.

Prefix	Part No.	RoHS	Package type	Version
MT	3302	G: Green product N: Pb product	N:QFN P:QFP L:LQFP C:CHIP B:BGA	xy

Table 6.1: MT3302 Part Number Explanation