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METANOIA

MT2311 Preliminary Datasheet

2013

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MT2311 Preliminary Datasheet

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Revision History

Revision	Description
1.0	First revision of this document.
1.01	Removed less important values in the Thermal Characteristics chapter.

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Contents

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List of Figures

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List of Tables

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Chapter 1

Introduction

The MT2311 is part of the Metanoia xDSL chipset solutions. MT2311 is a single chip, programmable Discrete Multi-Tone (DMT) Digital Subscriber Loop (DSL) digital modulator/ demodulator processor unit for VDSL2/ADSL2+. The Device supports all committee T1E1.4 and ITU-T G.993.2 VDSL2 and G.992.5 ADSL2+ discrete multi-tone based specifications, as well as IEEE 802.3 10PASS-TS.

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Chapter 2

Applications

Metanoia's PHY module enables a variety of suitable applications, from point-to-point solutions for industrial use to high end residential- or media gateways. Below are a few application examples.

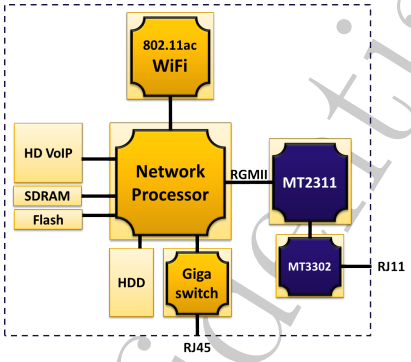

Figure 2.1: High-end gateway for the smart home

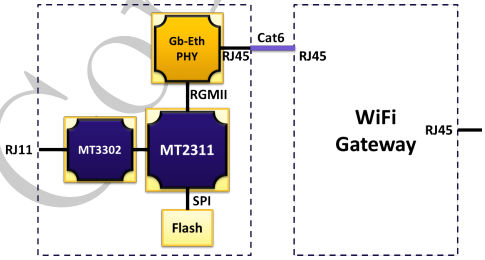

Figure 2.2: VDSL2 bridge to upgrade already deployed ADSL gateways with VDSL2 capabilities

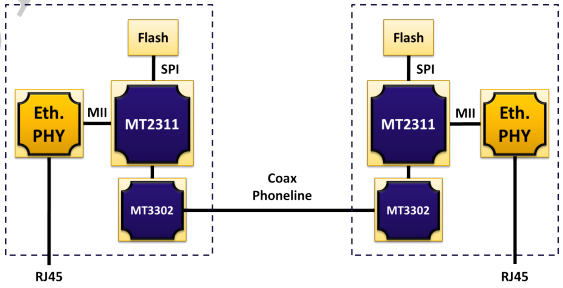

Figure 2.3: Point-to-point (P2P) bridge for a variety of Ethernet extension applications

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Chapter 3

Features

3.1 Features of MT2311

The features of MT2311 are described below. These features can be controlled through a command line interface that is also described in this document.

General Features

- ⋆ Single chip configurable DMT data pump supporting more than 100Mbps/100Mbps DS/US payload data rate.
- ⋆ Conformance to T1E1, ITU-T standards for VDSL2, ADSL2/2+ and current IEEE 802.3ah for 10PASS-TS (EFM).
- ⋆ Supports G.inp PHY layer retransmissions described in ITU-T standard G.998.4.
- ⋆ Supports G.vector for CPE side as described in ITU-T standard G.993.5.
- ⋆ Supports both UPBO and DPBO.
- ⋆ Optimized to support low latency as required for voice and other applications.

Hardware Features

- ⋆ 128-pin Low-profile Quad Flat Package (LQFP).
- ⋆ Two packaging options:
  1. Including MII/RGMII/GMII interfaces.
  2. Including MII/RGMII/SMII interfaces.
- ⋆ No external RAM required. Internal RAM booted from external flash memory or CPU via SPI or HPI interface.
- ⋆ Management available through HPI, proprietary SPI or through Ethernet packets with the Ethernet Boot and Management (EBM) protocol.

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VDSL2 Features

- ⋆ Supports all VDSL2 profiles (8a/b/c/d, 12a/b, 17a, 30a).
- ⋆ Supports Robust Overhead Channel (ROC).
- ⋆ Supports Seamless Rate Adaptation (SRA), bit-swapping and dynamic interleaver depth (D)-change.
- ⋆ Up to 3072 DMT carriers supported in the downstream and upstream directions.
- ⋆ All 4096 DMT carriers can be allocated between US/DS, with four DMT pass-bands per direction.
- ⋆ Trellis coding support for up to 3072 DMT carriers in any VDSL2 mode.
- ⋆ 4 KHz and 8 KHz (@2k carriers) symbol rates allow variable bandwidth per bin.
- ⋆ Configurable band-plan, conforms to NA and EU band-plans subject to the 3072/4096 and 8/4-passband constraints.

ADSL Features

The ADSL features described in this section are only available in CPE mode.

- ⋆ ADSL1/2/2+ fallback.
- ⋆ Conforms to ITU-T G.992.1/3/5 standards for ADSL1/2/2+.

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3.2 Details on Important Features of MT2311

3.2.1 G.inp retransmission procedures

The retransmission function can work in four modes:

- No retransmission.
- Only retransmission in upstream.
- Only retransmission in downstream.
- Retransmission in both directions.

At the transmitter side the channel coded packets are saved and at the receiver side the G.inp function also stores the received packets until error free packets have been assembled and extracted.

3.2.2 G.vector operation

The MT2311 provides all G.vector functions for the CPE side as described in the ITU-T standard G.993.5.

- Provides VTU-R downstream and upstream vectoring functions.
- For downstream vectoring, VTU-R supports sync symbol reception and error sample computing.
- For downstream vectoring, VTU-R can perform error sample reporting through either EOC or Ethernet L2 back channels.
- For upstream vectoring, VTU-R can transmit a modified sync symbol as configured by VTU-O, allowing the VTU-O to estimate channel conditions.

3.2.3 ATM operation

- Supports 0-255 VPs and 0-65535 VCs.
- Supports up to 8 PVCs and dynamic mapping of PVCs.
- Supports ATM UNI cell - AAL5 and OAM cells.
- Supports traffic shaping for upstream/downstream - CBR, UBR, rt-VBR, and nrt-VBR.
- Supports fault Management functions of ATM layer.
- OAM F4/F5 cells for Segment-to-Segment and end-to-end loopbacks.
- Supports LLC/SNAP and VC-MUX Ethernet bridged/routed encapsulation.
- Supports PPPoA encapsulation.
- Supports dynamic reconfiguration.
- Supports each PVC mapping to/from:
  - 802.1Q VLAN tag in Ethernet frame format
  - 802.1p Class of Service in Ethernet frame format
  - Classical IP, i.e. IP over ATM
  - multiple PVCs to one 802.1Q VLAN mapping

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Chapter 4

Interfaces

4.1 Data Interfaces of MT2311

MT2311 supports four widely used data interfaces: MII, SMII, RGMII and GMII (depending on package option). All of these interfaces conform to the official standards and specifications. Timing diagrams for these are shown in section 5.1.

4.2 Control Interfaces of MT2311

4.2.1 Serial Port Interface

The Serial Port Interface (SPI) supports both master and slave mode operations. Master mode is used when booting from a flash memory and slave mode is used when connected to a processor. When operating as master the interface supports all modes but when in slave mode the timing diagrams provided in section 5.1.2 must be carefully followed.

4.2.2 Host Port Interface

The host port interface (HPI) is an eight bit parallel interface. It supports both master and slave mode operation and provides a DMA interface to the internal memory for block transfers of up to 512 bytes. The HPI can interface with many microprocessors and DSPs available on the market with no external components. The HPI can provide a message interface API for a command and response interface with the external host. The command and response message format uses HDLC-like framing, similar to the one used in G.997.1. Each command is followed by an acknowledge response typically within 1 ms. If a command is not acknowledged within 10 ms, the command is assumed to be not understood or not executed due to some other error condition. The commands that are acknowledged are followed by a status frame sent from MT2311 to the host at a later time.

The HPI provides 11 pins to connect to an external memory bus as listed in table 4.1.

No. of Pins	Function
1	Data Strobe
1	Chip Select
1	Write Enable
8	Data Pins

Table 4.1: HPI pins

4.2.3 Ethernet Boot and Management

The Ethernet Boot and Management (EBM) protocol uses ethernet packets over the MII/SMII/RGMII/GMII interfaces for host control. Therefore if EBM is used the HPI/SPI pins are not needed for control of the chipset.

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4.3 Debug Interfaces of MT2311

4.3.1 Eyebox Interface

The MT2311 can be debugged using the *Eyebox* supplied by Metanoia. The *Eyebox* is a USB connected device that connects to the MT2311 through a proprietary 10-pin interface. It enables read and write of MIB parameters by using Metanoia's PC software, *DSLmonitor*.

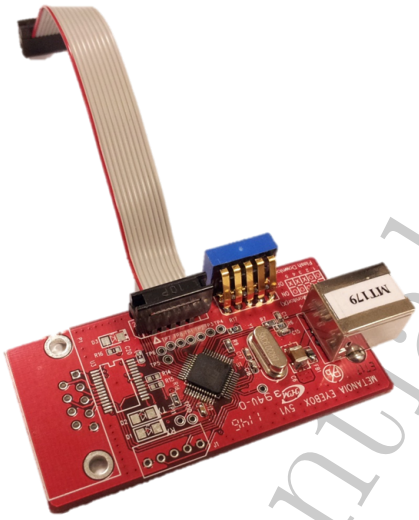

Figure 4.1: Picture of the Eyebox

4.4 Boot Modes of MT2311

SPI Master Boot Mode

Pin Name	Pin Definition	Power-on Strapping Value
IRQ[A,B,C,D]	Master Mode	0000
EX_AA3	BIST	1
EX_A16	Flash Hold*	1
EX_A17	No Use	0

* Flash Hold means that the flash operation is paused without deselecting the flash memory.

Table 4.2: Power-on strapping values for SPI Master Boot Mode

SPI Slave Boot Mode

Pin Name	Pin Definition	Power-on Strapping Value
IRQ[A,B,C,D]	Slave Mode	0010
EX_AA3	BIST	1
EX_A16	No Use	0
EX_A17	SPI Mode	1

Table 4.3: Power-on strapping values for SPI Slave Boot Mode

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HPI Boot Mode (Micro processor enable)

Pin Name	Pin Definition	Power-on Strapping Value
IRQ[A,B,C,D]	HPI Mode	1110
EX_AA3	BIST	1
EX_A16	8-bit Mode	0
EX_A17	Dual Strobe	1

Table 4.4: Power-on strapping values for HPI Boot Mode

Ethernet Boot Mode

Pin Name	Pin Definition	Power-on Strapping Value
IRQ[A,B,C,D]	Ethernet Mode	0101
EX_AA3	BIST	1
Ethernet Interface Selection		
Pin Name	**Interface Mode**	**Power-on Strapping Value**
EX_A[17,16]	SMII	00
EX_A[17,16]	MII	01
EX_A[17,16]	GMII	10
EX_A[17,16]	RGMII	11

Table 4.5: Power-on strapping values for Ethernet Boot Mode

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Chapter 5

Interface Timing

5.1 Timing Characteristics for MT2311

This section presents the detailed timing characteristics for the MT2311. The values of the timing parameters are tabulated below each waveform diagram. All output times are measured with a 25 pF load capacitance for max conditions and 5 pF load capacitance for min conditions, unless noted otherwise. Timing parameters are measured at voltage levels of $(V_{IH} + V_{IL})/2$ and $(V_{OH} + V_{OL})/2$, for input and output signals, respectively. All input transition times, 10/90%, used for timing measurements are 1.0 ns for max conditions and 0.2 ns for min conditions.

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5.1.1 Host Port Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
Setup for CS to Read	$t_{CSSetup}$	10	-	-	ns
Hold for CS to Read	t_{CSHold}	30	-	-	ns
Period of Read Strobe	t_{READ}	100	-	-	ns
Data ready to CS	t_{DSetup}	12	-	-	ns
Data to Hi-Z	t_{DtoZ}	-	-	12	ns

Table 5.1: Host port read cycle characteristic

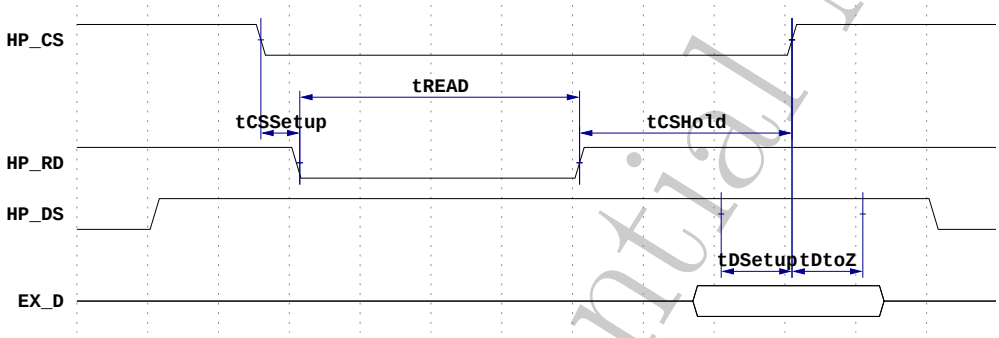

Figure 5.1: Host port read cycle timing diagram

Parameter	Symbol	Min	Typ	Max	Unit
Data Setup time	t_{DSetup}	12	-	-	ns
Setup for CS to strobe	$t_{CSSetup}$	8	-	-	ns
Period of write strobe	t_{WRITE}	100	-	-	ns
Hold for CS to strobe	t_{CSHold}	30	-	-	ns
Data Hold time	t_{DHold}	10	-	-	ns

Table 5.2: Host port write cycle characteristic

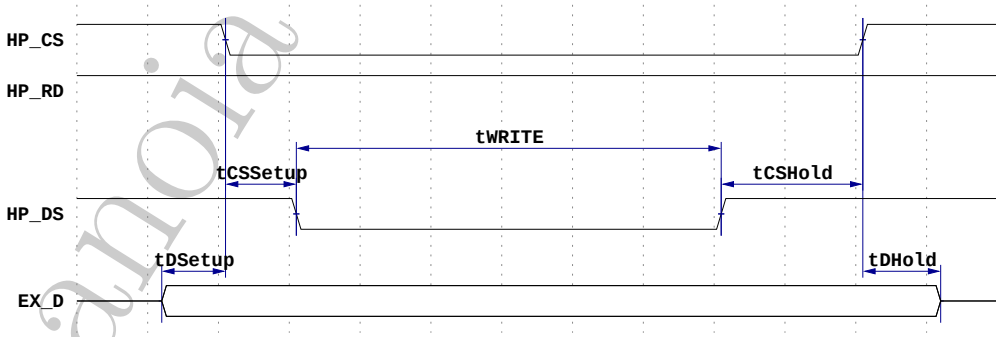

Figure 5.2: Host port write cycle timing diagram

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5.1.2 Serial Port Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
SCK(A-B) frequency	$1/t_P$	0.036	-	37.5	MHz
SRD(A-B)/STD(A-B) delay from SCK↑	t_D	30	-	100	ns
SRD(A-B)/STD(A-B) setup from SCK↑	t_S	15	-	-	ns
SRD(A-B)/STD(A-B) hold from SCK↑	t_H	0.0	-	-	ns
SC2(B) delay from SCK↑	t_D	10	-	100	ns

Table 5.3: Serial port A-B interface characteristic

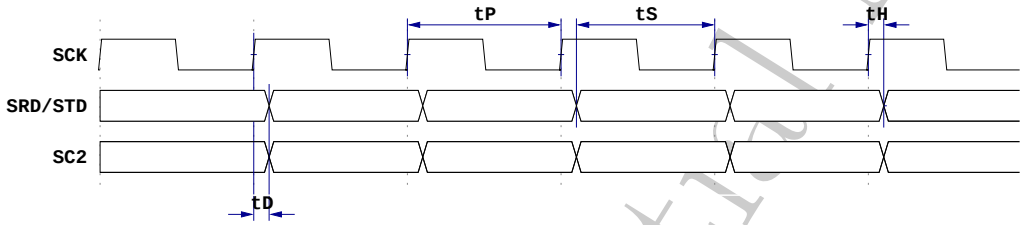

Figure 5.3: Serial port A-B interface timing diagram

Parameter	Symbol	Min	Typ	Max	Unit
SCK frequency	$1/t_{CYCLE}$	-	-	20	MHz
SCK duty cycle	t_P	40	-	60	%
CS setup time	t_{CSS}	10	-	-	ns
CS hold time	t_{CSH}	10	-	-	ns
SO setup time	t_{SOS}	10	-	-	ns
SO hold time	t_{SOH}	10	-	-	ns
SO to Hi-Z time	t_{SOZ}	-	-	10	ns
SI setup time	t_{SIS}	10	-	-	ns
SI hold time	t_{SIH}	20	-	-	ns
Dummy SCK cycle	c_{DUMMY}	1	-	-	cycles

Table 5.4: Serial port slave mode characteristic

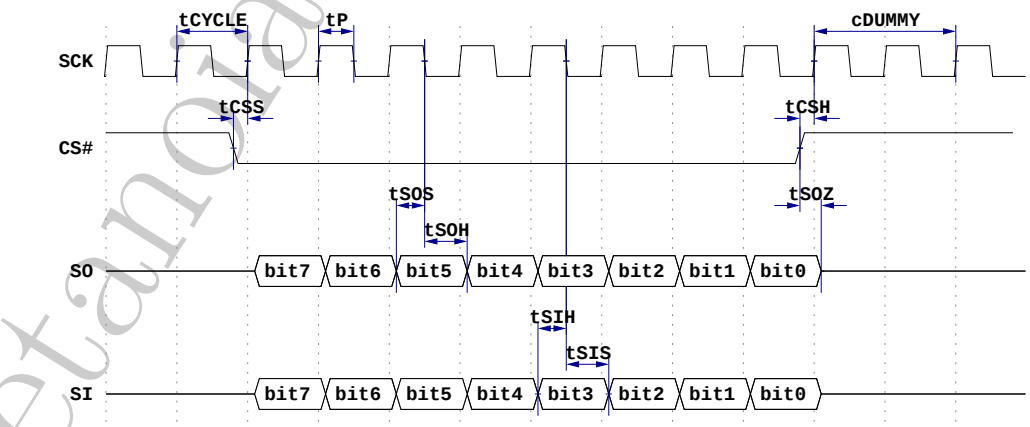

Figure 5.4: Serial port slave mode timing diagram

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5.1.3 MII Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
MII_RXCLK frequency	$1/t_P$	-	25	-	MHz
MII_RXCLK duty cycle	-	40	-	60	%
MII_RXD(0-3) setup to MII_RXCLK↑	t_S	15	-	-	ns
MII_RXD(0-3) hold from MII_RXCLK↑	t_H	5	-	-	ns

Table 5.5: MII output characteristic

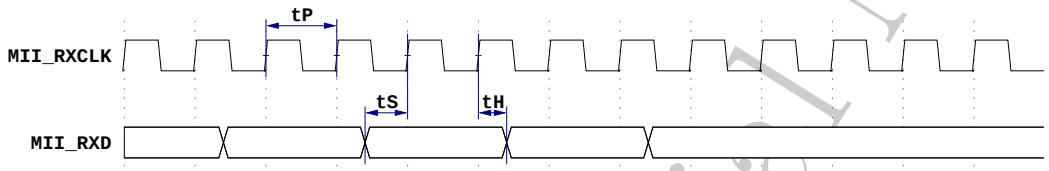

Figure 5.5: MII output timing diagram

Parameter	Symbol	Min	Typ	Max	Unit
MII_TXCLK frequency	$1/t_P$	-	25	-	MHz
MII_TXCLK duty cycle	-	40	-	60	%
MII_TXD(0-3) setup to MII_TXCLK↑	t_S	15	-	-	ns
MII_TXD(0-3) hold from MII_TXCLK↑	t_H	5	-	-	ns

Table 5.6: MII input characteristic

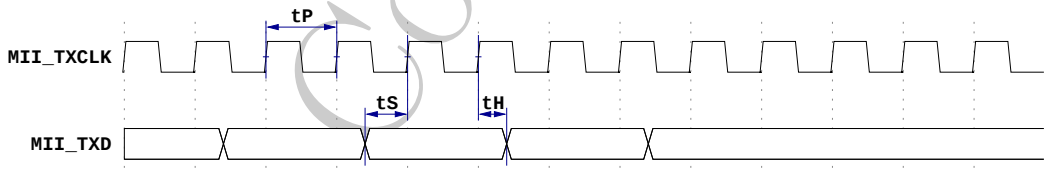

Figure 5.6: MII input timing diagram

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5.1.4 RGMII Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at Tx)	t_{ST}	-500	-	500	ps
Data to clock input skew (at Rx)	t_{SR}	1	-	2.6	ns

Table 5.7: RGMII interface characteristic

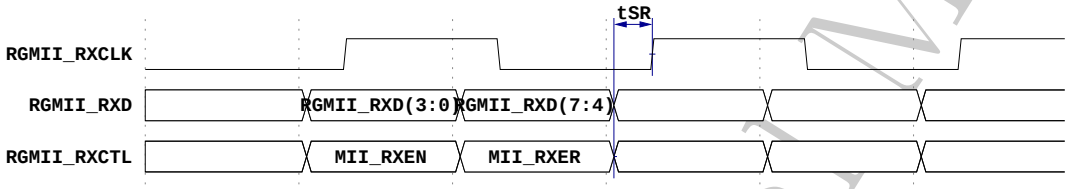

Figure 5.7: RGMII output timing diagram

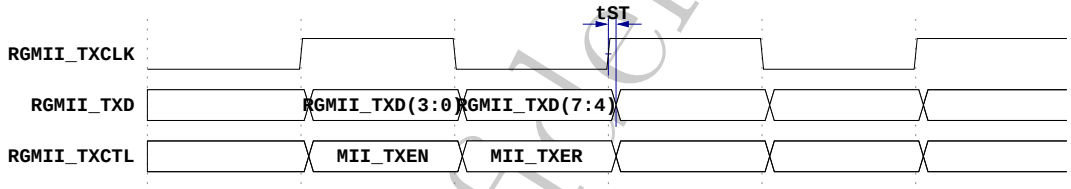

Figure 5.8: RGMII input timing diagram

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5.1.5 GMII Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
GMII_TXEN and GMII_TXD(0-7) to GMII_TXCLK	t_{SU}	2.0	-	-	ns
GMII_TXEN and GMII_TXD(0-7) to GMII_TXCLK rising hold time	t_H	0	-	-	ns
GMII_RXCLK rising to GMII_RXDV and GMII_RXD(0-7) output delay	t_{DLY}	0.5	-	5.5	ns

Table 5.8: GMII interface characteristic

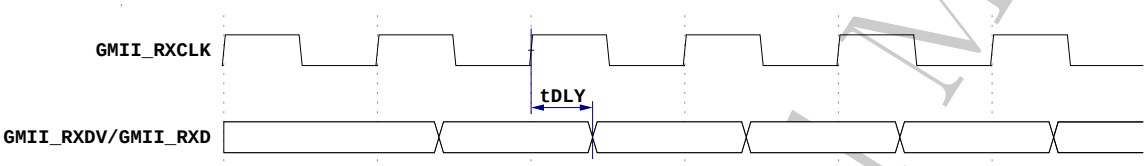

Figure 5.9: GMII output timing diagram

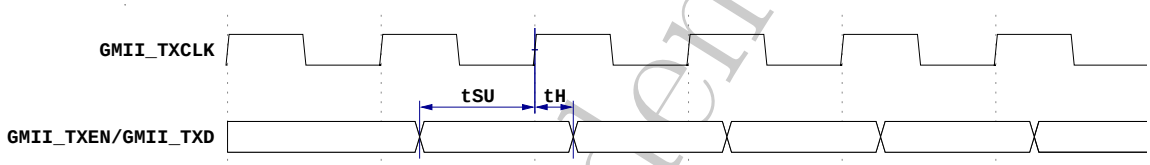

Figure 5.10: GMII input timing diagram

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5.1.6 SMII Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
STXCLK and SRXCLK period	t_P	-	8.0	-	ns
STXCLK and SRXCLK duty cycle	-	40	-	60	%
STXSYNC setup time to STXCLK ↑	t_S	1.5	-	-	ns
STXSYNC hold time from STXCLK ↑	t_H	1.0	-	-	ns
SRXSYNC/SRXCLK delay from STXCLK	t_D	1.5	-	4.5	ns

Table 5.9: SMII interface characteristic

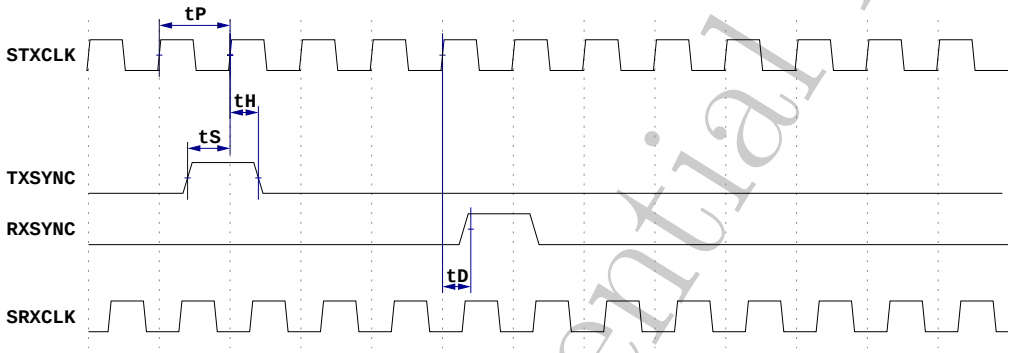

Figure 5.11: SMII Sync In/Out timing diagram

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Parameter	Symbol	Min	Typ	Max	Unit
SRXCLK period	t_P	-	8.0	-	ns
SRXDAT(0-1) delay from SRXCLK↑	t_D	1.5	-	4.5	ns

Table 5.10: SMII receiver characteristic

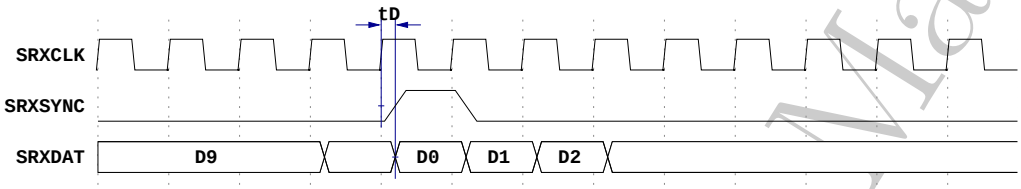

Figure 5.12: SMII receiver timing diagram

Parameter	Symbol	Min	Typ	Max	Unit
STXCLK period	t_P	-	8.0	-	ns
STXDAT(0-1) setup to STXCLK↑	t_S	1.5	-	-	ns
STXDAT(0-1) hold from STXCLK↑	t_H	1.0	-	-	ns

Table 5.11: SMII transmitter characteristic

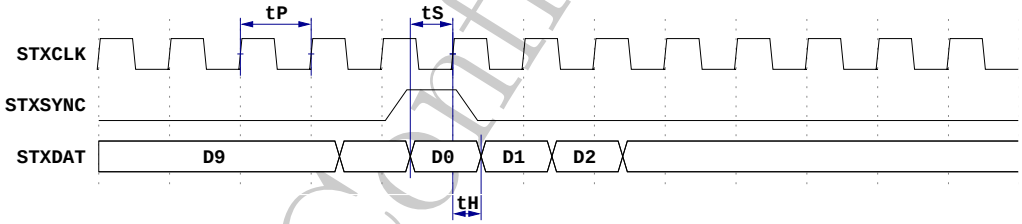

Figure 5.13: SMII transmitter timing diagram

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5.1.7 AFE Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
ACLK frequency	$1/t_P$	-	35.328	-	MHz
ATXD(2-15) setup to ACLK↑	t_S	4	-	-	ns
ATXD(2-15) hold from ACLK↑	t_H	3	-	-	ns
ARXD(2-15) setup to ACLK↑	t_S	4	-	-	ns
ARXD(2-15) hold from ACLK↑	t_H	3	-	-	ns

Table 5.12: AFE interface characteristic

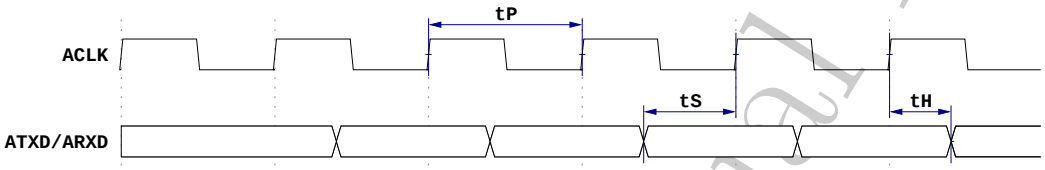

Figure 5.14: AFE interface timing diagram

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Chapter 6

Electrical Characteristics

6.1 Electrical Characteristics for MT2311

6.1.1 Absolute Maximum Ratings and Environmental Limitations

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage (CMOS I/O)	V_{DDIO}	-0.3	3.6	V	Note 1, 4
Supply voltage (Core)	V_{DDCORE}	-0.3	1.1	V	Note 1, 4
Supply Voltage (PLL)	V_{CCPLL}	-0.3	1.1	V	Note 1, 4
DC input voltage	V_{IN}	-0.5	5.5	V	Note 1, 4
Storage temperature range	T_S	-55	+150	$°C$	Note 1
Ambient operating	T_A	0	+85	$°C$	0 ft/min linear
Temperature	ME	5	-	$Level$	Per IPC/JEDEC
Moisture exposure level	RH	30	60	%	Note 2
Relative humidity level	RH	0	100	%	Non-condensing
ESD classification	ESD	-	2	kV	Note 3

Table 6.1: Values for absolute maximum ratings and environmental limitations

Notes:
1. Operating conditions outside the min-max ranges specified may cause permanent device failure. Exposure to conditions near the min or max limits for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per JEDEC JESD22-A114-B.
4. Device core is 1.0V only.

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6.1.2 Power Requirements

Parameter	Min	Typ	Max	Unit	Conditions
V_{DDIO}	3.0	3.3	3.6	V	
I_{DDIO}	20	-	-	mA	See notes 1, 2
P_{DDIO}	60	-	-	mW	See notes 1, 2
V_{CCPLL}	0.9	1.0	1.1	V	
I_{CCPLL}	-	-	10	mA	See notes 1, 2
P_{CCPLL}	-	-	10	mW	See notes 1, 2
V_{DDCORE}	0.9	1.0	1.1	V	
I_{DDCORE}	-	285	315	mA	See notes 1, 2
P_{DDCORE}	-	285	346.5	mW	See notes 1, 2
P_{TOTAL}	313.1	341.5	403.4	mW	See notes 1, 2

Table 6.2: Power requirements

Notes:
1. Typical estimated values with nominal voltages at 25 $°C$.
2. All I_{DD} and P_{DD} values are dependent upon V_{DD}.

6.1.3 Input Parameters for LVTTL

Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	2.0	-	-	V	$3.14 \leq V_{DDIO} \leq 3.46$
V_{IL}	-	-	0.8	V	$3.14 \leq V_{DDIO} \leq 3.46$
Input leakage current	-10		10	μA	$V_{IN} = V_{DDIO} \vee V_{SSIO}$
Input capacitance	-	5	-	pF	

Table 6.3: Input parameters for LVTTL

6.1.4 Input Parameters for LVTTL$_{pull}$

Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	2.0	-	-	V	$3.14 \leq V_{DDIO} \leq 3.46$
V_{IL}	-	-	0.8	V	$3.14 \leq V_{DDIO} \leq 3.46$
Internal Pull High Resistance	-	28k	-	Ω	$V_{IN} = V_{DDIO} \vee V_{SSIO}$
Input capacitance	-	5	-	pF	

Table 6.4: Input parameters for LVTTL$_{pull}$

6.1.5 Output Parameters for CMOS

Parameter	Min	Typ	Max	Unit	Conditions
V_{OH}	V_{DDIO} - 0.4	-	-	V	$I_{OH} = -10mA$
V_{OL}	-	-	0.4	V	$I_{OL} = 10mA$
I_{OL}	-	-	10.0	mA	
I_{OH}	-	-	-10.0	mA	
Leakage tristate	-10	-	10	μA	

Table 6.5: Output parameters for CMOS

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6.1.6 Input/Output Parameters for LVTTL/CMOS

Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	2.0	-	-	V	$3.14 \leq V_{DDIO} \leq 3.46$
V_{IL}	-	-	0.8	V	$3.14 \leq V_{DDIO} \leq 3.46$
Input leakage current	-10	-	10	μA	$V_{DDIO} = 3.46$
Input capacitance	-	5	-	pF	
V_{OH}	V_{DDIO} - 0.4	-	-	V	$I_{OH} = -10mA$
V_{OL}	-	-	0.4	V	$I_{OL} = 10mA$
I_{OL}	-	-	10.0	mA	
I_{OH}	-	-	-10.0	mA	

Table 6.6: Input/Output parameters for LVTTL/CMOS

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Chapter 7

Thermal Characteristics

7.1 Thermal Characteristics for MT2311

7.1.1 Thermal Resistance

Parameter	Symbol	Value	Unit	Conditions
Junction to ambient temperature	θ_{ja}	50.28	$°C/W$	4 layer PCB, 0m/s airflow, 25$°C$
Junction to case temperature	θ_{jc}	9.5	$°C/W$	4 layer PCB, 0m/s airflow, 25$°C$

Table 7.1: Thermal resistance for MT2311

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Chapter 8

Pin Configuration

8.1 Pin Configuration for MT2311

8.1.1 General Pin Description

Pin	Symbol	Type	Description
1	GMII_RXD7	I/O	GMII receive data 7, output / SMII Tx clock, input
2	GMII_RXD6	I/O	GMII receive data 6, output / SMII Tx sync, input
3	GMII_RXD5	I/O	GMII receive data 5, output / SMII Tx data 1, input
4	GMII_RXD4	I/O	GMII receive data 4, output / SMII Tx data 0, input
5	MII_CRS	O	MII/GMII/RGMII carrier sense
6	MII_COL	O	MII/GMII/RGMII collision
7	MII_RXD3	O	MII/RGMII/GMII receive data 3-0, output
8	MII_RXD2	O	
9	MII_RXD1	O	
10	MII_RXD0	O	
11	MII_RXDV	O	MII/RGMII/GMII indicates Rx data valid
12	MII_RXCLK	I/O	MII/RGMII/GMII Rx clock
13	MII_RXER	O	MII/GMII indicates error on Rx
14	MII_TXER	I	MII/GMII indicates error on Tx
15	MII_TXCLK	I/O	MII/RGMII/GMII Tx clock
16	MII_TXEN	I	MII/GMII transmit enable / RGMII transmit control
17	VDDPST	V_{DDIO}	VDD digital I/O supply
18	VSSPST	V_{SSIO}	VSS digital I/O supply
19	MII_TXD0	I	MII/RGMII/GMII transmit data 0-1, input
20	MII_TXD1	I	
21	VDD	V_{DDCORE}	VDD digital core supply
22	VSS	V_{SSCORE}	VSS digital core supply
23	MII_TXD2	I	MII/RGMII/GMII transmit data 2, input
24	VDD	V_{DDCORE}	VDD digital core supply
25	VSS	V_{SSCORE}	VSS digital core supply
26	MII_TXD3	I	MII/RGMII/GMII transmit data 3, input
27	VDDPST	V_{DDIO}	VDD digital I/O supply
28	VSSPST	V_{SSIO}	VSS digital I/O supply
29	GMII_TXD4	I/O	GMII transmit data 4, input / SMII Rx data 0, output
30	GMII_TXD5	I/O	GMII transmit data 5, input / SMII Rx data 1, output
31	GMII_TXD6	I/O	GMII transmit data 6, input / SMII Rx clock, output
32	GMII_TXD7	I/O	GMII transmit data 7, input / SMII Rx sync, output
33	MDC	I	MDC

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Pin	Symbol	Type	Description
34	MDIO	I/O	MDIO
35	VCCOSC(3.3V)	VCC OSC	OSC 3.3V supply
36	XTALI	I	Master crystal oscillator input
37	XTALO	O	Master crystal oscillator output
38	VSSOSC	VSS OSC	OSC supply
39	STDA	O	SPI serial port A transmit data/GPIO(output only)
40	SRDA	I	SPI serial port A receive data/GPIO(input only)
41	SCKA	I/O	SPI serial port A clock/GPIO
42	TESTMODE	I	For internal use only/tie to ground
43	NMI	I	Non-maskable interrupt
44	VDD	V_{DDCORE}	VDD digital core supply
45	VSS	V_{SSCORE}	VSS digital core supply
46	ARXD2	I	AFE interface receive data 2
47	VDDPST	V_{DDIO}	VDD digital I/O supply
48	VSSPST	V_{SSIO}	VSS digital I/O supply
49	ARXD3	I	AFE interface receive data 3-6
50	ARXD4	I	
51	ARXD5	I	
52	ARXD6	I	
53	VDD	V_{DDCORE}	VDD digital core supply
54	VSS	V_{SSCORE}	VSS digital core supply
55	ARXD7	I	AFE interface receive data 7-8
56	ARXD8	I	
57	ACLK	I	AFE interface clock
58	ARXD9	I	AFE interface receive data 9-15
59	ARXD10	I	
60	ARXD11	I	
61	ARXD12	I	
62	ARXD13	I	
63	ARXD14	I	
64	ARXD15	I	
65	ATXD15	O	AFE interface transmit data 15-4
66	ATXD14	O	
67	ATXD13	O	
68	ATXD12	O	
69	ATXD11	O	
70	ATXD10	O	
71	ATXD9	O	
72	ATXD8	O	
73	ATXD7	O	
74	ATXD6	O	
75	ATXD5	O	
76	ATXD4	O	
77	VSS	V_{SSCORE}	VSS digital core supply
78	VDD	V_{DDCORE}	VDD digital core supply
79	ATXD3	O	AFE interface transmit data 3-2
80	ATXD2	O	
81	SCKB	I/O	SPI serial port B clock
82	STDB	O	SPI serial port B transmit data/GPIO(output only)
83	SRDB	I	SPI serial port B receive data/GPIO(input only)
84	SC2B	I/O	SPI serial port B control 2/GPIO
85	VSSPST	V_{SSIO}	VSS I/O supply
86	VDDPST	V_{DDIO}	VDD I/O supply
87	TMS	I	JTAG/OnCE test mode select (internal pull-up)
88	DEN	I	JTAG/OnCE debug enable

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Pin	Symbol	Type	Description
89	TDI	I	JTAG/OnCE test data in (internal pull-up)
90	VSS	V_{SSCORE}	VSS digital core supply
91	VDD	V_{DDCORE}	VDD digital core supply
92	TDO	O	JTAG/OnCE test data out
93	TCK	I	JTAG/OnCE test clock (internal pull-down)
94	TRSTN	I	JTAG/OnCE test reset (internal pull-up)
95	EX_A11/GPIO0	I/O	External memory address 11/GPIO0
96	EX_A16/GPIO1	I/O	External memory address 16/GPIO1
97	VCCPLL1	V_{CCPLL}	VCC supply for PLL1
98	VSSPLL1	V_{SSPLL}	VSS for PLL1
99	EX_A17/GPIO2	I/O	External memory address 17/GPIO2
100	EX_AA0/3	I/O	Ext. memory address attribute 0-3/GPIO3-6
101	EX_AA1/4	I/O	
102	EX_AA2/5	I/O	
103	EX_AA3/6	I/O	
104	RESET	I	System reset signal active low
105	VSS	V_{SSCORE}	VSS digital core supply
106	VDD	V_{DDCORE}	VDD digital core supply
107	HP_DY	I/O	Host port slave ready
108	HP_CS	I/O	Host port chip select
109	HP_RD	I/O	Host port read/write
110	HP_DS	I/O	Host port data strobe
111	SCKC/EX_D0/8	I/O	SPI serial port C clock/External memory data 8/Host port data 0/GPIO8
112	SRDC/EX_D1/9	I/O	SPI serial port C receive data/External memory data 9/Host port data 1/GPIO9
113	STDC/EX_D2/10	I/O	SPI serial port C transmit data/External memory data 10/Host port data 2/GPIO10
114	VSSPST	V_{SSIO}	VSS I/O supply
115	VDDPST	V_{DDIO}	VDD I/O supply
116	SC2C/EX_D3/11	I/O	SPI serial port C control 2/External memory data 11/Host port data 3/GPIO11
117	EX_D4/12	I/O	External memory data 12/Host port data 4/GPIO12
118	EX_D5/13	I/O	External memory data 13/Host port data 5/GPIO13
119	VSS	V_{SSCORE}	VSS digital core supply
120	VDD	V_{DDCORE}	VDD digital core supply
121	EX_D6/14	I/O	External memory data 14/Host port data 6/GPIO14
122	EX_D7/15	I/O	External memory data 15/Host port data 7/GPIO15
123	IRQA	I	External interrupt A/Test mode 0 lead strap
124	IRQB	I	External interrupt B/Test mode 1 lead strap
125	IRQC	I	External interrupt C/Test mode 2 lead strap
126	IRQD	I	External interrupt D/Test mode 3 lead strap
127	VCCPLL2	V_{CCPLL}	VCC supply for PLL2
128	VSSPLL2	V_{SSPLL}	VSS supply for PLL2

Table 8.1: General pin description

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8.1.2 Data Interface Pins for MII/RGMII/GMII Package

Package: MII/RGMII/GMII				
No.	**I/O**	**MII**	**RGMII**	**GMII**
1	I/O	-	-	GMII_RXD7 (O)
2	I/O	-	-	GMII_RXD6 (O)
3	I/O	-	-	GMII_RXD5 (O)
4	I/O	-	-	GMII_RXD4 (O)
5	O	MII_CRS	MII_CRS	MII_CRS
6	O	MII_COL	MII_COL	MII_COL
7	O	MII_RXD3	RGMII_RXD3	GMII_RXD3
8	O	MII_RXD2	RGMII_RXD2	GMII_RXD2
9	O	MII_RXD1	RGMII_RXD1	GMII_RXD1
10	O	MII_RXD0	RGMII_RXD0	GMII_RXD0
11	O	MII_RXDV	RGMII_RXCTL	GMII_RXDV
12	I/O	MII_RXCLK(I)	RGMII_RXCLK(O)	GMII_RXCLK(O)
13	O	MII_RXER	MII_RXER	MII_RXER
14	I	MII_TXER	MII_TXER	MII_TXER
15	I/O	MII_TXCLK(IO)	RGMII_TXCLK(I)	GMII_TXCLK (I)
16	I	MII_TXEN	RGMII_TXCTL	GMII_TXEN
19	I	MII_TXD0	RGMII_TXD0	GMII_TXD0
20	I	MII_TXD1	RGMII_TXD1	GMII_TXD1
23	I	MII_TXD2	RGMII_TXD2	GMII_TXD2
26	I	MII_TXD3	RGMII_TXD3	GMII_TXD3
29	I/O	-	-	GMII_TXD4 (I)
30	I/O	-	-	GMII_TXD5 (I)
31	I/O	-	-	GMII_TXD6 (I)
32	I/O	-	-	GMII_TXD7 (I)

Table 8.2: Interface pin description of MII/RGMII/GMII package

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8.1.3 Data Interface Pins for MII/SMII/RGMII Package

Package: MII/SMII/RGMII				
No.	**I/O**	**MII**	**SMII**	**RGMII**
1	I/O	-	STXCLK (I)	-
2	I/O	-	STXSYNC (I)	-
3	I/O	-	STXDAT1 (I)	-
4	I/O	-	STXDAT0 (I)	-
5	O	MII_CRS	-	MII_CRS
6	O	MII_COL	-	MII_COL
7	O	MII_RXD3	-	RGMII_RXD3
8	O	MII_RXD2	-	RGMII_RXD2
9	O	MII_RXD1	-	RGMII_RXD1
10	O	MII_RXD0	-	RGMII_RXD0
11	O	MII_RXDV	-	RGMII_RXCTL
12	I/O	MII_RXCLK(I)	-	RGMII_RXCLK(O)
13	O	MII_RXER	-	MII_RXER
14	I	MII_TXER	-	MII_TXER
15	I/O	MII_TXCLK(IO)	-	RGMII_TXCLK(I)
16	I	MII_TXEN	-	RGMII_TXCTL
19	I	MII_TXD0	-	RGMII_TXD0
20	I	MII_TXD1	-	RGMII_TXD1
23	I	MII_TXD2	-	RGMII_TXD2
26	I	MII_TXD3	-	RGMII_TXD3
29	I/O	-	SRXDAT0 (O)	-
30	I/O	-	SRXDAT1 (O)	-
31	I/O	-	SRXCLK (O)	-
32	I/O	-	SRXSYNC (O)	-

Table 8.3: Interface pin description of MII/SMII/RGMII package

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8.1.4 Pinout Diagram

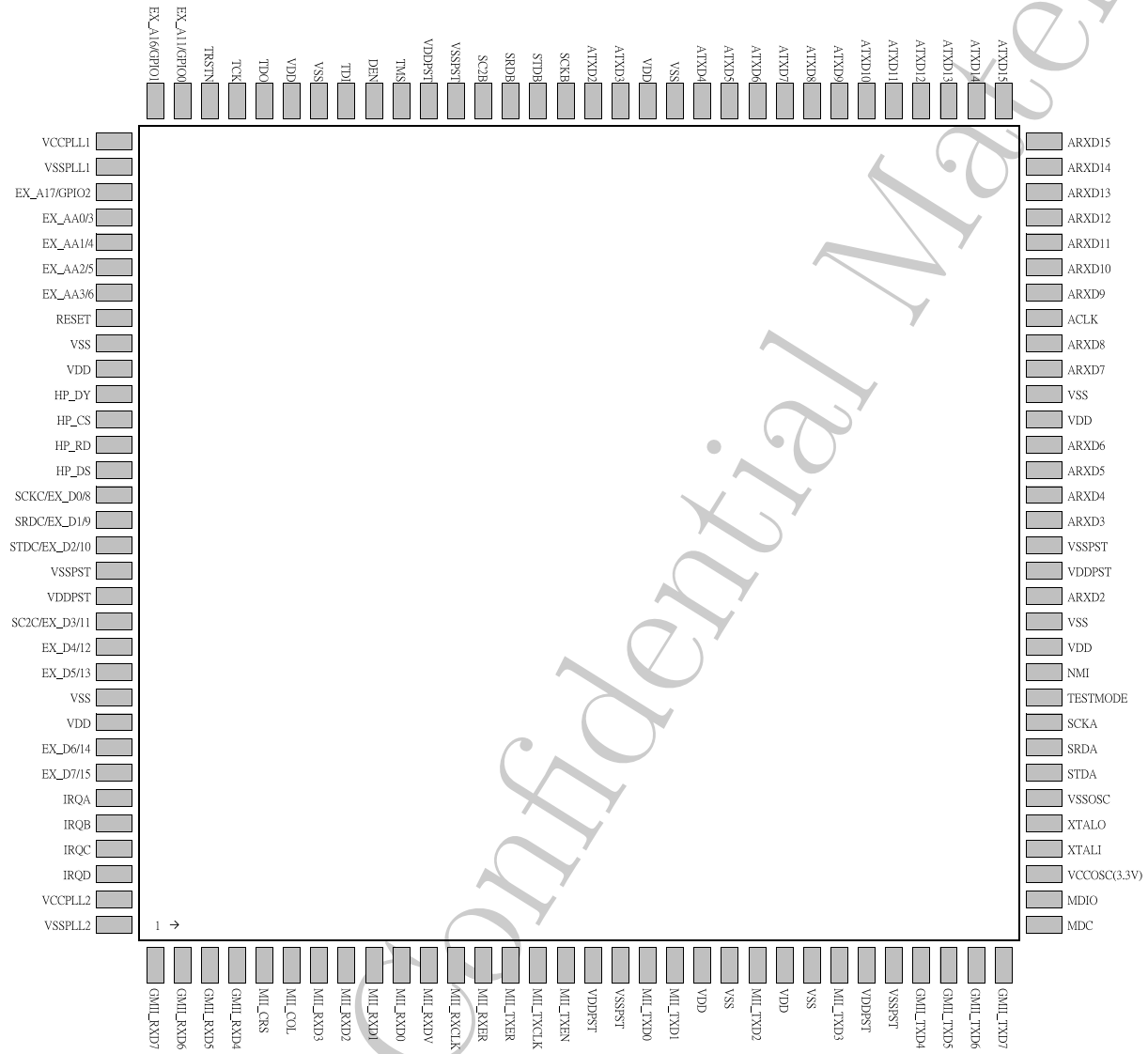

Figure 8.1: Pinout diagram for MT2311.

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Chapter 9

Package

9.1 Package Information for MT2311

The MT2311 device is packaged in a 14mm×14mm, 128-pin Low-profile Quad Flat Package (LQFP) suitable for surface mounting, as shown in Figure 9.1.

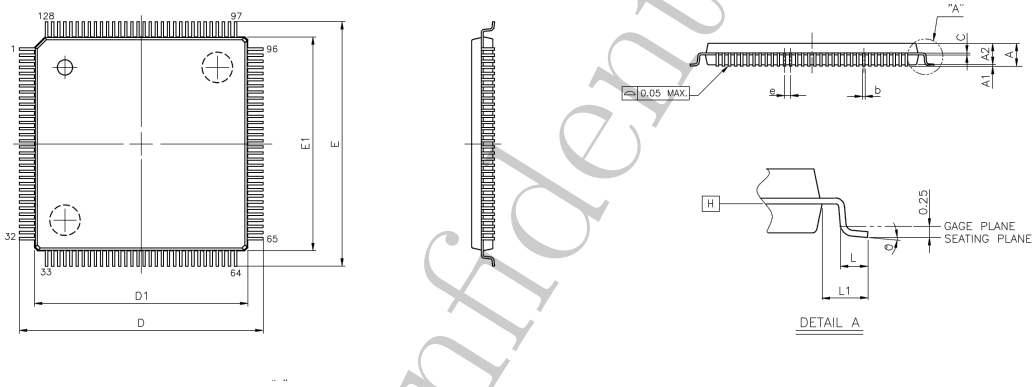

Figure 9.1: Package diagram

Symbol	Dimension (mm)			Dimension (MIL)		
	MIN	NOM.	MAX	MIN	NOM	MAX
A	-	-	1.60	-	-	62.99
A1	0.05	-	0.15	1.97	-	5.91
A2	1.35	1.40	1.45	53.15	55.12	57.09
b	0.13	0.16	0.23	5.12	6.30	9.06
c	0.09	-	0.20	3.54	-	7.87
D	16.00 BSC			629.9 BSC		
D1	14.00 BSC			551.2 BSC		
E	16.00 BSC			629.9 BSC		
E1	14.00 BSC			551.2 BSC		
e	0.40 BSC			15.7 BSC		
L	0.45	0.60	0.75	17.72	23.62	29.53
L1	1.00 REF			39.37 REF		
∘	0°	3.5°	7°	-	-	-

Table 9.1: Package dimensions

1. DATUM PLANE IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

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Chapter 10

Description of Provided Software

10.1 Overview of the Components

10.1.1 Introduction

This chapter describes the basic components of the software layer that Metanoia provides in order to control the functionality of the MT2311. The role of each component and the relationship of each component is also described in this chapter.

10.1.2 Software Components

Figure 10.1 shows software components and relationship between them. Below the components are described further.

1. **dslcli**
   The *dslcli* is a user space command line interface (CLI) program. It communicates with the driver via *ioctl()*. The user can use *dslcli* to access xDSL data or execute xDSL commands for functions like disconnecting the line or changing xDSL profile. It is also a shell-like program which supports many commands, so the user can easily send commands to the chip via *dslcli*.

2. **driver**
   The *driver* is a lower level software component which handles hardware dependency flow. Since different hardware may have different control access requirements, the *driver* handles hardware access to make the upper layer interface hardware independent. In other words, the user only needs to know the interface, and does not need to care about the details of hardware.

3. **board.conf** and **cfgmgr**
   The *board.conf* is a configuration file containing global settings that remains persistent after device reset. It restores settings such as the profile setting, PVC settings, etc. after a device reset. *cfgmgr* is a utility for easily accessing the *board.conf* configuration file. With the -r option, the operator can read a setting in *board.conf*, and with the -w option, the operator can write a setting into *board.conf*.

4. **system.conf** and ***.scr**
   The *dslcli* can read a list of commands in a script and automatically execute those commands in a sequence. This allows the user to perform initial flow as necessary or setup a sequence of settings. The *system.conf* is the first script run by *dslcli*. It includes the necessary initial setup commands for CPE and CO modes.

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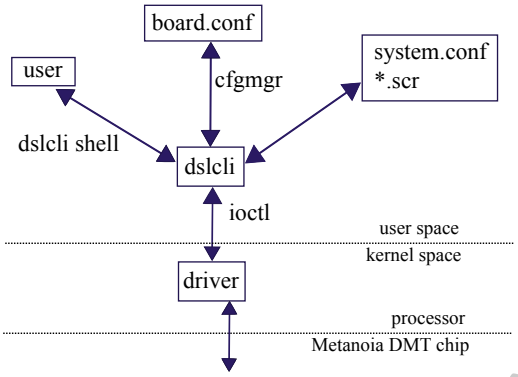

Figure 10.1: Software components

The *dslcli* needs *board.conf* to save global settings and scripts to do automatic setup. *dslcli* is also an interface for the user. It passes each user command to the driver layer. The *driver* handles hardware dependent access and sends commands to hardware. When hardware returns a response, the *driver* passes the result back to *dslcli*. Finally *dslcli* returns the result to the user.

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Chapter 11

Ordering Information

11.1 Ordering Information for MT2311

Part Number:
MT2311GL-xy: 1 port xDSL DMT chip with 128-LQFP package.

Prefix	Part No.	RoHS	Package type	Version
MT	2311	G: Green product N: Pb product	N:QFN P:QFP L:LQFP C:CHIP B:BGA	xy

Table 11.1: MT2311 part number explanation

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