METANOIA

MT2301 Datasheet

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MT2301 Datasheet

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Revision History

Revision	Description
1.6	Last revision of this document in previous format.
1.7	First revision of this document in new format.
1.71	Removed less import values in Thermal Characteristics chapter.

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Chapter 1

Introduction

The MT2301 is part of the Metanoia VDSL2 chipset solutions. MT2301 is a single chip, programmable Discrete Multi-Tone (DMT) Digital Subscriber Loop (DSL) digital modulator/ demodulator processor unit for VDSL2. The Device supports all committee T1E1.4 and ITU-T G.993.2 VDSL2 discrete multi-tone based specifications, as well as IEEE 802.3 10PASS-TS.

Chapter 2

Applications

Metanoia's PHY module enables a variety of suitable applications, from point-to-point solutions for industrial use to high end residential- or media gateways. Below are a few application examples.

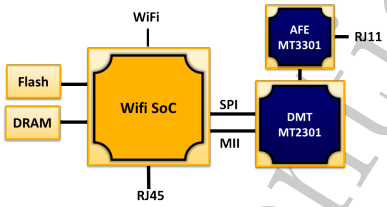

Figure 2.1: Home gateway including all needs of todays' users

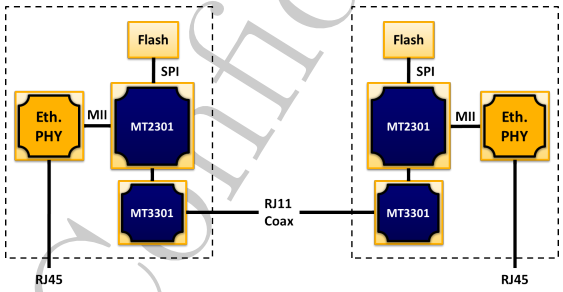

Figure 2.2: Point-to-point (P2P) bridge for a number of Ethernet extension applications

Chapter 3

Features

The features of MT2301 are described below. These features can be controlled through a command line interface that is also described in this document.

General Features

- ⋆ Single chip configurable DMT data pump supporting more than 100Mbps/100Mbps DS/US payload data rate.
- ⋆ Conformance to T1E1, ITU-T standards for VDSL2, ADSL2/2+ and current IEEE 802.3ah for 10PASS-TS (EFM).
- ⋆ Supports both UPBO and DPBO.
- ⋆ Optimized to support low latency as required for voice and other applications.

Hardware Features

- ⋆ 128-pin Low-profile Quad Flat Package (LQFP)
- ⋆ Support MII and SMII data interfaces in same package
- ⋆ No external RAM required. Internal RAM booted from external flash memory or CPU via SPI or HPI interface.

VDSL2 Features

- ⋆ Supports all VDSL2 profiles (8a/b/c/d, 12a/b, 17a, 30a).
- ⋆ Supports Seamless Rate Adaptation (SRA), bit-swapping and dynamic interleaver depth (D)-change.
- ⋆ Up to 3072 DMT carriers supported in the downstream and upstream directions.
- ⋆ All 4096 DMT carriers can be allocated between US/DS, with four DMT pass-bands per direction.
- ⋆ Trellis coding support for up to 3072 DMT carriers in any VDSL2 mode.
- ⋆ 4 KHz and 8 KHz (@2k carriers) symbol rates allow variable bandwidth per bin.
- ⋆ Configurable band-plan, conforms to NA and EU band-plans subject to the 3072/4096 and 8/4-passband constraints.

Chapter 4

Interfaces

4.1 Data Interfaces of MT2301

MT2301 supports four widely used data interfaces: MII and SMII. Both of these interfaces conform to the official standards and specifications. Timing diagrams for these are shown in section 5.1.

4.2 Control Interfaces of MT2301

4.2.1 Serial Port Interface

The Serial Port Interface (SPI) supports both master and slave mode operations. Master mode is used when booting from a flash memory and slave mode is used when connected to a processor. When operating as master the interface supports all modes but when in slave mode the timing diagrams provided in section 5.1.2 must be carefully followed.

4.2.2 Host Port Interface

The host port interface (HPI) is an eight bit parallel interface. It supports both master and slave mode operation and provides a DMA interface to the internal memory for block transfers of up to 512 bytes. The HPI can interface with many microprocessors and DSPs available on the market with no external components. The HPI can provide a message interface API for a command and response interface with the external host. The command and response message format uses HDLC-like framing, similar to the one used in G.997.1. Each command is followed by an acknowledge response typically within 1 ms. If a command is not acknowledged within 10 ms, the command is assumed to be not understood or not executed due to some other error condition. The commands that are acknowledged are followed by a status frame sent from MT2301 to the host at a later time.

The HPI provides 11 pins to connect to an external memory bus as listed in table 4.1.

No. of Pins	Function
1	Data Strobe
1	Chip Select
1	Write Enable
8	Data Pins

Table 4.1: HPI pins

4.3 Debug Interfaces of MT2301

4.3.1 Eyebox Interface

The MT2301 can be debugged using the *Eyebox* supplied by Metanoia. The *Eyebox* is a USB connected device that connects to the MT2301 through a proprietary 10-pin interface. It enables read and write of MIB parameters by using Metanoia's PC software, *DSLmonitor*.

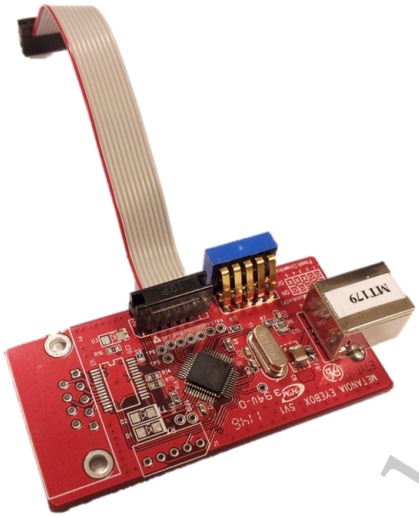

Figure 4.1: Picture of the Eyebox

Chapter 5

Interface Timing

5.1 Timing Characteristics for MT2301

This section presents the detailed timing characteristics for the MT2301. The values of the timing parameters are tabulated below each waveform diagram. All output times are measured with a 25 pF load capacitance for max conditions and 5 pF load capacitance for min conditions, unless noted otherwise. Timing parameters are measured at voltage levels of $(V_{IH} + V_{IL})/2$ and $(V_{OH} + V_{OL})/2$, for input and output signals, respectively. All input transition times, 10/90%, used for timing measurements are 1.0 ns for max conditions and 0.2 ns for min conditions.

5.1.1 Host Port Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
Setup for CS to Read	$t_{CSSetup}$	10	-	-	ns
Hold for Read to CS	t_{CSHold}	30	-	-	ns
Period of Read Strobe	t_{READ}	100	-	-	ns
Data ready to CS	t_{DSetup}	12	-	-	ns
Data to Hi-Z	t_{DtoZ}	-	-	12	ns

Table 5.1: Host port read cycle characteristic

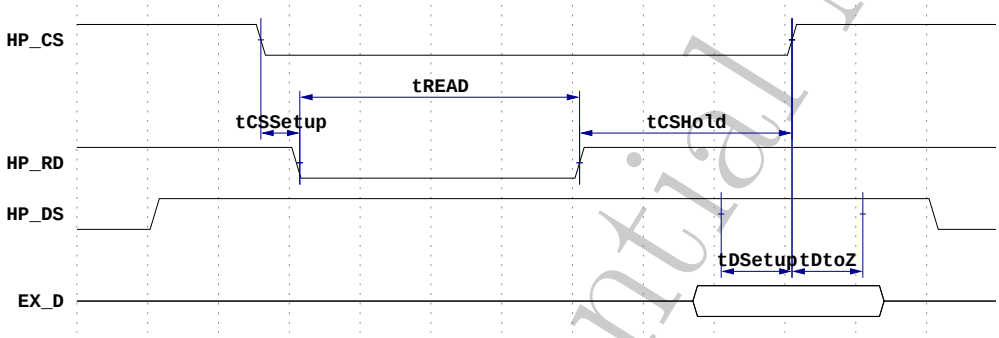

Figure 5.1: Host port read cycle timing diagram

Parameter	Symbol	Min	Typ	Max	Unit
Data Setup time	t_{DSetup}	12	-	-	ns
Setup for CS to strobe	$t_{CSSetup}$	8	-	-	ns
Period of write	t_{WRITE}	100	-	-	ns
Hold for CS to strobe	t_{CSHold}	30	-	-	ns
Data Hold time	t_{DHold}	10	-	-	ns

Table 5.2: Host port write cycle characteristic

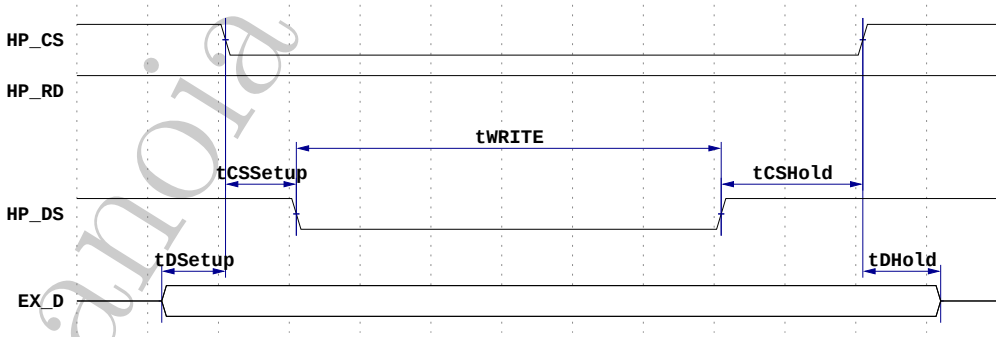

Figure 5.2: Host port write cycle timing diagram

5.1.2 Serial Port Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
SCK(A-B) frequency	$1/t_P$	0.036	-	37.5	MHz
SRD(A-B)/STD(A-B) delay from SCK↑	t_D	30	-	100	ns
SRD(A-B)/STD(A-B) setup from SCK↑	t_S	15	-	-	ns
SRD(A-B)/STD(A-B) hold from SCK↑	t_H	0.0	-	-	ns
SC2(B) delay from SCK↑	t_D	10	-	100	ns

Table 5.3: Serial port A-B interface characteristic

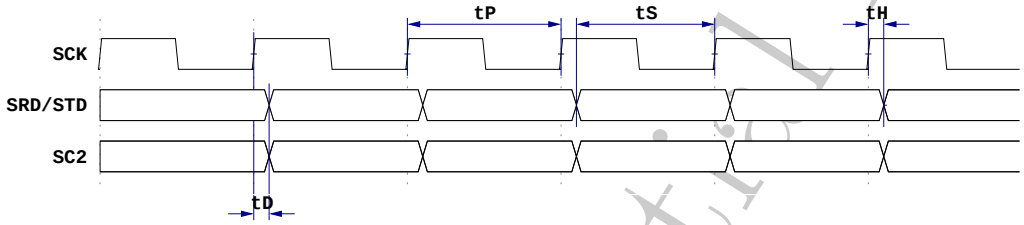

Figure 5.3: Serial port A-B interface timing diagram

5.1.3 SMII Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
STXCLK and SRXCLK period	t_P	-	8.0	-	ns
STXCLK and SRXCLK duty cycle	-	40	-	60	%
STXSYNC setup time to STXCLK ↑	t_S	1.5	-	-	ns
STXSYNC hold time from STXCLK ↑	t_H	1.0	-	-	ns
SRXSYNC/SRXCLK delay from STXCLK	t_D	1.5	-	4.5	ns

Table 5.4: SMII interface characteristic

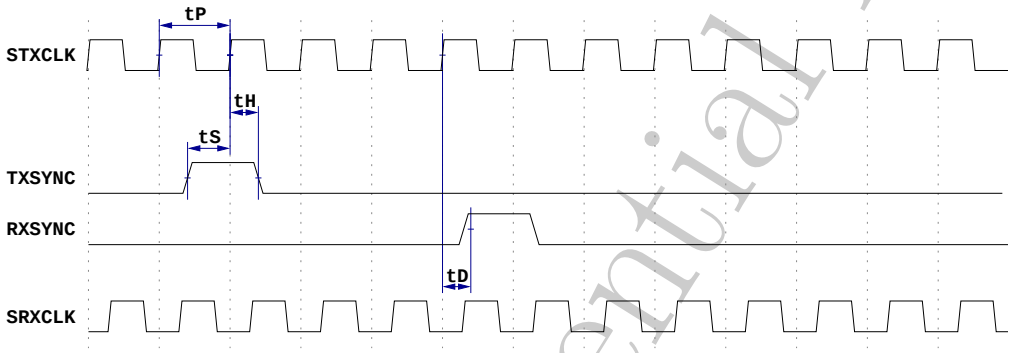

Figure 5.4: SMII Sync In/Out timing diagram

Parameter	Symbol	Min	Typ	Max	Unit
SRXCLK period	t_P	-	8.0	-	ns
SRXDAT(0-1) delay from SRXCLK↑	t_D	1.5	-	4.5	ns

Table 5.5: SMII receiver characteristic

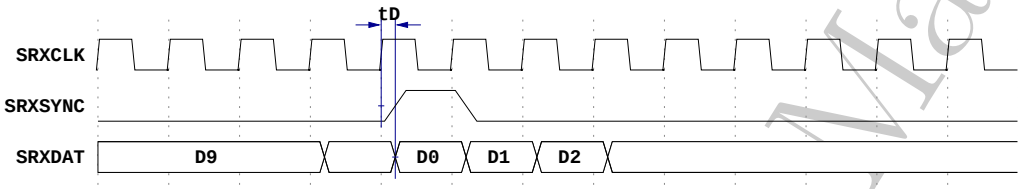

Figure 5.5: SMII receiver timing diagram

Parameter	Symbol	Min	Typ	Max	Unit
STXCLK period	t_P	-	8.0	-	ns
STXDAT(0-1) setup to STXCLK↑	t_S	1.5	-	-	ns
STXDAT(0-1) hold from STXCLK↑	t_H	1.0	-	-	ns

Table 5.6: SMII transmitter characteristic

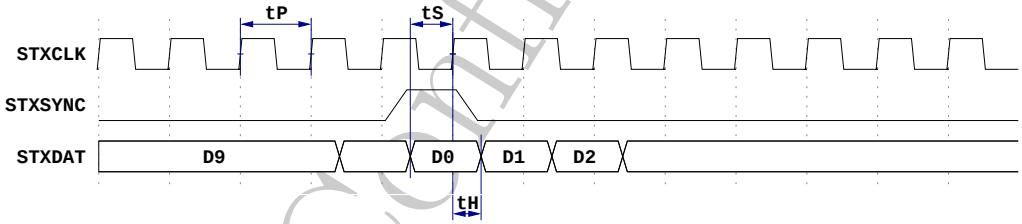

Figure 5.6: SMII transmitter timing diagram

5.1.4 MII Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
MII_RXCLK frequency	$1/t_P$	-	25	-	MHz
MII_RXCLK duty cycle	-	40	-	60	%
MII_RXD(0-3) setup to MII_RXCLK↑	t_S	15	-	-	ns
MII_RXD(0-3) hold from MII_RXCLK↑	t_H	5	-	-	ns

Table 5.7: MII output characteristic

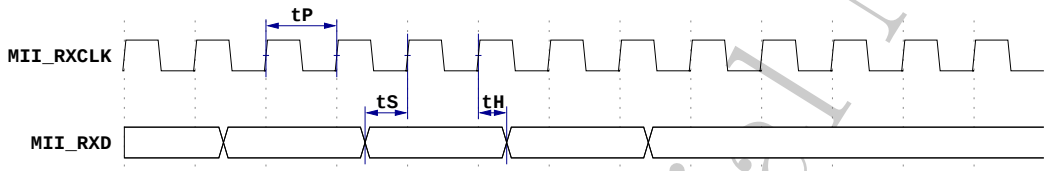

Figure 5.7: MII output timing diagram

Parameter	Symbol	Min	Typ	Max	Unit
MII_TXCLK frequency	$1/t_P$	-	25	-	MHz
MII_TXCLK duty cycle	-	40	-	60	%
MII_TXD(0-3) setup to MII_TXCLK↑	t_S	15	-	-	ns
MII_TXD(0-3) hold from MII_TXCLK↑	t_H	5	-	-	ns

Table 5.8: MII input characteristic

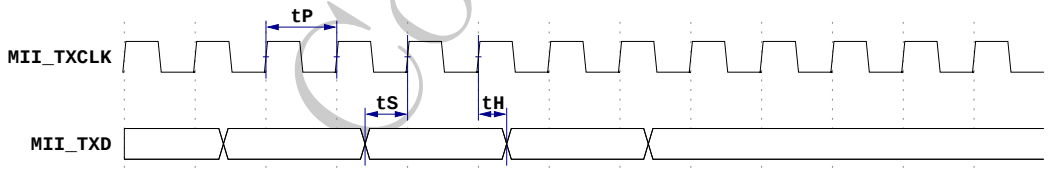

Figure 5.8: MII input timing diagram

5.1.5 AFE Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
ACLK frequency	$1/t_P$	-	35.328	-	MHz
ATXD(2-15) setup to ACLK↑	t_S	4	-	-	ns
ATXD(2-15) hold from ACLK↑	t_H	3	-	-	ns
ARXD(2-15) setup to ACLK↑	t_S	4	-	-	ns
ARXD(2-15) hold from ACLK↑	t_H	3	-	-	ns

Table 5.9: AFE interface characteristic

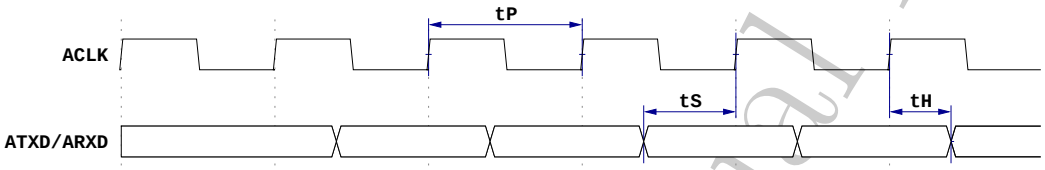

Figure 5.9: AFE interface timing diagram

Chapter 6

Electrical Characteristics

6.1 Electrical Characteristics for MT2301

6.1.1 Absolute Maximum Ratings and Environmental Limitations

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage (CMOS I/O)	V_{DDIO}	-0.3	3.96	V	Note 1, 4
Supply voltage (Core)	V_{DDCORE}	-0.3	1.32	V	Note 1, 4
DC input voltage	V_{IN}	-0.5	5.5	V	Note 1, 4, 5
Storage temperature range	T_S	-55	+150	$°C$	Note 1
Ambient operating	T_A	0	+85	$°C$	0 ft/min linear
Temperature	ME	5	-	$Level$	Per IPC/JEDEC
Moisture exposure level	RH	30	60	%	Note 2
Relative humidity level	RH	0	100	%	Non-condensing
ESD classification	ESD	-	2	kV	Note 3

Table 6.1: Values for absolute maximum ratings and environmental limitations

Notes:

1. Operating conditions outside the min-max ranges specified may cause permanent device failure. Exposure to conditions near the min or max limits for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per JEDEC JESD22-A114-B.
4. Device core is 1.2V only.
5. MT2301 is 5 V compatible in the sense that the output logic 1 (V_{OH}) and output logic 0 (V_{OL}) levels of the MT2301 outputs have been specified at the same voltage levels that have been commonly recognized as logic 1 and logic 0 for the 5 V environment. MT2301 can generally be expected to drive 5 V TTL compatible components. However, while MT2301 outputs are able to meet the minimum input logic switching levels (V_{IH} and V_{IL}) of 5 V TTL compatible components, the output logic 1 output voltage of some 5 V components may exceed the maximum input voltage of MT2301. Depending on the technology and circuit implementation, the 5 V TTL compatible components may drive their outputs anywhere from 3 V to their V_{DD} supply level. CAUTION: Before connecting a 5 V component to the MT2301, always check to be sure that the Maximum V_{OH} of the 5 V device does not exceed the specified Maximum V_{IN} listed in the table above.

6.1.2 Power Requirements

Parameter	Min	Typ	Max	Unit	Conditions
V_{DDIO}	2.667	3.3	3.96	V	
I_{DDIO}	20	-	-	mA	See notes 1, 2
P_{DDIO}	53.34	-	-	mW	See notes 1, 2
V_{CCPLL}	1.12	1.2	1.32	V	
I_{CCPLL}	-	-	10	mA	See notes 1, 2
P_{CCPLL}	-	-	13.2	mW	See notes 1, 2
V_{DDCORE}	1.12	1.2	1.32	V	
I_{DDCORE}	-	320	335	mA	See notes 1, 2
P_{DDCORE}	358.4	384.0	442.2	mW	See notes 1, 2
P_{TOTAL}	415	450	550	mW	See notes 1, 2

Table 6.2: Power requirements

Notes:
1. Typical estimated values with nominal voltages at 25 $°C$.
2. All I_{DD} and P_{DD} values are dependent upon V_{DD}.

6.1.3 Input Parameters for LVTTL

Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	2.0	-	-	V	$3.14 \leq V_{DDIO} \leq 3.46$
V_{IL}	-	-	0.8	V	$3.14 \leq V_{DDIO} \leq 3.46$
Input leakage current	-10		10	μA	$V_{IN} = V_{DDIO} \vee V_{SSIO}$
Input capacitance	-	5	-	pF	

Table 6.3: Input parameters for LVTTL

6.1.4 Input Parameters for LVTTL$_{pull}$

Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	2.0	-	-	V	$3.14 \leq V_{DDIO} \leq 3.46$
V_{IL}	-	-	0.8	V	$3.14 \leq V_{DDIO} \leq 3.46$
Internal Pull High Resistance	-	28k	-	Ω	$V_{IN} = V_{DDIO} \vee V_{SSIO}$
Input capacitance	-	5	-	pF	

Table 6.4: Input parameters for LVTTL$_{pull}$

6.1.5 Output Parameters for CMOS

Parameter	Min	Typ	Max	Unit	Conditions
V_{OH}	2.4	-	-	V	$I_{OH} = -16mA$
V_{OL}	-	0.2	0.4	V	$I_{OL} = 16mA$
I_{OL}	-	-	16.0	mA	
I_{OH}	-	-	-16.0	mA	
Leakage tristate	-10	-	10	μA	

Table 6.5: Output parameters for CMOS

6.1.6 Input/Output Parameters for LVTTL/CMOS

Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	2.0	-	-	V	$3.14 \leq V_{DDIO} \leq 3.46$
V_{IL}	-	-	0.8	V	$3.14 \leq V_{DDIO} \leq 3.46$
Input leakage current	-10	-	10	μA	$V_{DDIO} = 3.46$
Input capacitance	-	5	-	pF	
V_{OH}	2.4	-	-	V	$I_{OH} = -16mA$
V_{OL}	-	0.2	0.4	V	$I_{OL} = 16mA$
I_{OL}	-	-	16.0	mA	
I_{OH}	-	-	-16.0	mA	

Table 6.6: Input/Output parameters for LVTTL/CMOS

Chapter 7

Thermal Characteristics

7.1 Thermal Characteristics for MT2301

7.1.1 Thermal Resistance

Parameter	Symbol	Value	Unit	Conditions
Junction to ambient temperature	θ_{ja}	50.28	$°C/W$	4 layer PCB, 0m/s airflow, 25$°C$
Junction to case temperature	θ_{jc}	9.5	$°C/W$	4 layer PCB, 0m/s airflow, 25$°C$

Table 7.1: Thermal resistance

Chapter 8

Pin Configuration

8.1 Pins Configuration for MT2301

8.1.1 General Pin Description

Pin	Symbol	Type	Description
1	STXCLK	I	SMII Tx clock
2	STXSYNC	I	SMII Tx sync
3	STXDAT1	I	SMII Tx data 1
4	STXDAT0	I	SMII Tx data 0
5	MII_CRS	O	MII carrier sense
6	MII_COL	O	MII collision
7	MII_RXD3	O	MII receive data 3-0
8	MII_RXD2	O	
9	MII_RXD1	O	
10	MII_RXD0	O	
11	MII_RXDV	O	MII indicates Rx data valid
12	MII_RXCLK	I/O	MII Rx clock
13	MII_RXER	O	MII indicates error on Rx
14	MII_TXER	I	MII indicates error on Tx
15	MII_TXCLK	I/O	MII Tx clock
16	MII_TXEN	I	MII transmit enable
17	VDDPST	V_{DDIO}	VDD digital I/O supply
18	VSSPST	V_{SSIO}	VSS digital I/O supply
19	MII_TXD0	I	MII transmit data 0-1
20	MII_TXD1	I	
21	VDD	V_{DDCORE}	VDD digital core supply
22	VSS	V_{SSCORE}	VSS digital core supply
23	MII_TXD2	I	MII transmit data 2
24	VDD	V_{DDCORE}	VDD digital core supply
25	VSS	V_{SSCORE}	VSS digital core supply
26	MII_TXD3	I	MII transmit data 3
27	VDDPST	V_{DDIO}	VDD digital I/O supply
28	VSSPST	V_{SSIO}	VSS digital I/O supply
29	SRXDAT0	O	SMII Rx data 0-1
30	SRXDAT1	O	
31	SRXCLK	O	SMII Rx clock
32	SRXSYNC	O	SMII Rx sync
33	MDC	I	MDC
34	MDIO	I/O	MDIO
35	VCCOSC(3.3V)	VCC OSC	OSC 3.3V supply
36	XTALI	I	Master crystal oscillator input

Pin	Symbol	Type	Description
37	XTALO	O	Master crystal oscillator output
38	VSSOSC	VSS OSC	OSC supply
39	STDA	O	SPI serial port A transmit data/GPIO(output only)
40	SRDA	I	SPI serial port A receive data/GPIO(input only)
41	SCKA	I/O	SPI serial port A clock/GPIO
42	TESTMODE	I	For internal use only/tie to ground
43	NMI	I	Non-maskable interrupt/PLL bypass lead strap
44	VDD	V_{DDCORE}	VDD digital core supply
45	VSS	V_{SSCORE}	VSS digital core supply
46	ARXD2	I	AFE interface receive data 2
47	VDDPST	V_{DDIO}	VDD digital I/O supply
48	VSSPST	V_{SSIO}	VSS digital I/O supply
49	ARXD3	I	AFE interface receive data 3-6
50	ARXD4	I	
51	ARXD5	I	
52	ARXD6	I	
53	VDD	V_{DDCORE}	VDD digital core supply
54	VSS	V_{SSCORE}	VSS digital core supply
55	ARXD7	I	AFE interface receive data 7-8
56	ARXD8	I	
57	ACLK	I	AFE interface clock
58	ARXD9	I	AFE interface receive data 9-15
59	ARXD10	I	
60	ARXD11	I	
61	ARXD12	I	
62	ARXD13	I	
63	ARXD14	I	
64	ARXD15	I	
65	ATXD15	O	AFE interface transmit data 4-15
66	ATXD14	O	
67	ATXD13	O	
68	ATXD12	O	
69	ATXD11	O	
70	ATXD10	O	
71	ATXD9	O	
72	ATXD8	O	
73	ATXD7	O	
74	ATXD6	O	
75	ATXD5	O	
76	ATXD4	O	
77	VSS	V_{SSCORE}	VSS digital core supply
78	VDD	V_{DDCORE}	VDD digital core supply
79	ATXD3	O	AFE interface transmit data 3-2
80	ATXD2	O	
81	SCKB	I/O	SPI serial port B clock
82	STDB	O	SPI serial port B transmit data/GPIO(output only)
83	SRDB	I	SPI serial port B receive data/GPIO(input only)
84	SC2B	I/O	SPI serial port B control 2/GPIO
85	VSSPST	V_{SSIO}	VSS I/O supply
86	VDDPST	V_{DDIO}	VDD I/O supply
87	TMS	I	JTAG/OnCE test mode select (internal pull-up)
88	DEN	I	JTAG/OnCE debug enable
89	TDI	I	JTAG/OnCE test data in (internal pull-up)
90	VSS	V_{SSCORE}	VSS digital core supply
91	VDD	V_{DDCORE}	VDD digital core supply

Pin	Symbol	Type	Description
92	TDO	O	JTAG/OnCE test data out
93	TCK	I	JTAG/OnCE test clock (internal pull-down)
94	TRSTN	I	JTAG/OnCE test reset (internal pull-up)
95	EX_A11/GPIO0	I/O	External memory address 11/GPIO0
96	EX_A16/GPIO1	I/O	External memory address 16/GPIO1
97	VCCPLL1	V_{CCPLL}	VCC supply for PLL1
98	VSSPLL1	V_{SSPLL}	VSS for PLL1
99	EX_A17/GPIO2	I/O	External memory address 17/GPIO2
100	EX_AA0	I/O	External memory address attribute 0-3/GPIO3-6
101	EX_AA1	I/O	
102	EX_AA2	I/O	
103	EX_AA3	I/O	
104	RESET	I	System reset signal active low
105	VSS	V_{SSCORE}	VSS digital core supply
106	VDD	V_{DDCORE}	VDD digital core supply
107	HP_DY	I/O	Host port slave ready
108	HP_CS	I/O	Host port chip select
109	HP_RD	I/O	Host port read/write
110	HP_DS	I/O	Host port data strobe
111	EX_D0/8	I/O	External memory data 8/Host port data 0/GPIO8
112	EX_D1/9	I/O	External memory data 9/Host port data 1/GPIO9
113	EX_D2/10	I/O	External memory data 10/Host port data 2/GPIO10
114	VSSPST	V_{SSIO}	VSS I/O supply
115	VDDPST	V_{DDIO}	VDD I/O supply
116	EX_D3/11	I/O	External memory data 11/Host port data 3/GPIO11
117	EX_D4/12	I/O	External memory data 12/Host port data 4/GPIO12
118	EX_D5/13	I/O	External memory data 13/Host port data 5/GPIO13
119	VSS	V_{SSCORE}	VSS digital core supply
120	VDD	V_{DDCORE}	VDD digital core supply
121	EX_D6/14	I/O	External memory data 14/Host port data 6/GPIO14
122	EX_D7/15	I/O	External memory data 15/Host port data 7/GPIO15
123	IRQA	I	External interrupt A/Test mode 0 lead strap
124	IRQB	I	External interrupt B/Test mode 1 lead strap
125	IRQC	I	External interrupt C/Test mode 2 lead strap
126	IRQD	I	External interrupt D/Test mode 3 lead strap
127	VCCPLL2	V_{CCPLL}	VCC supply for PLL2
128	VSSPLL2	V_{SSPLL}	VSS supply for PLL2

Table 8.1: General pin description

8.1.2 Pinout Diagram

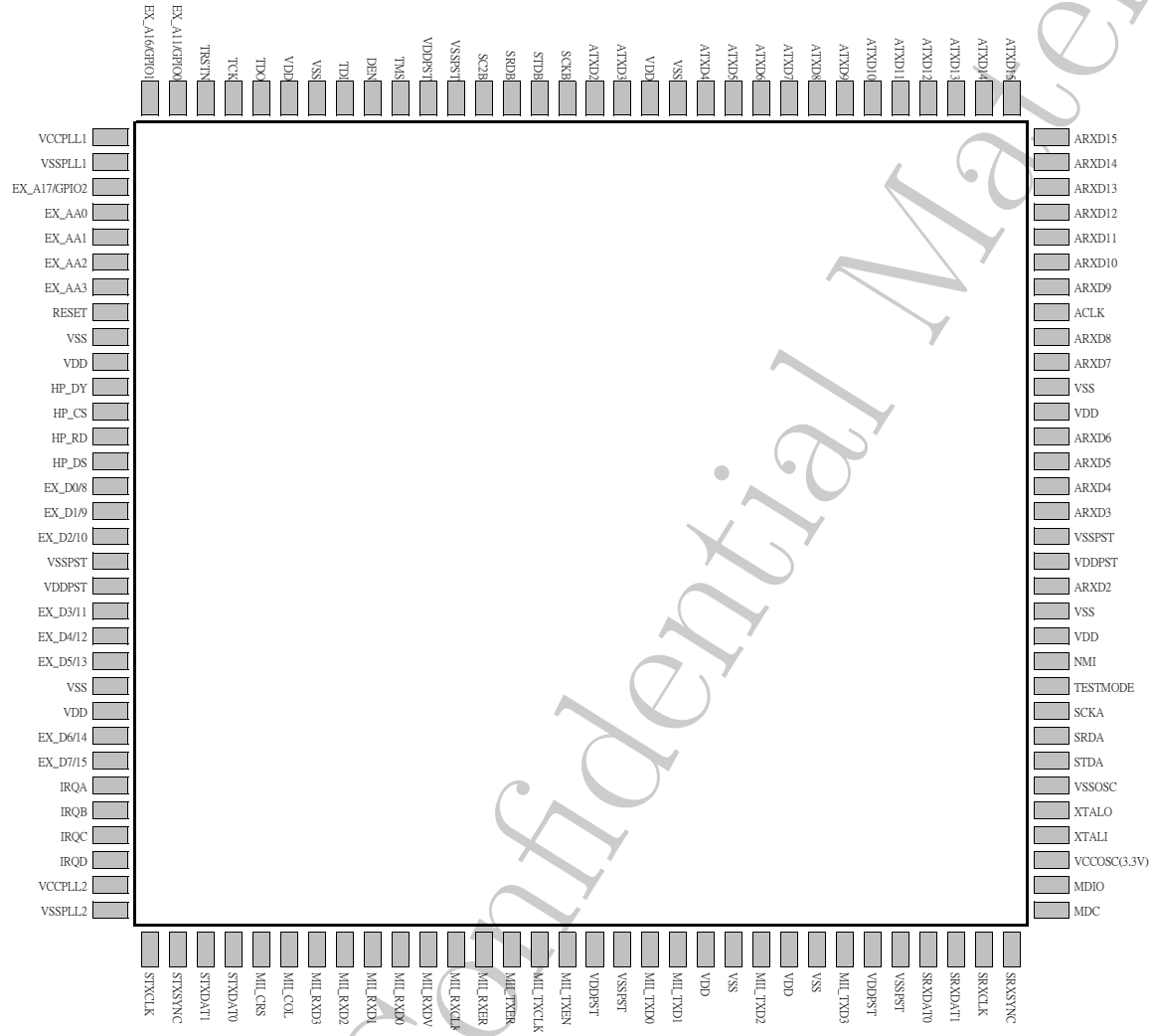

Figure 8.1: Pinout diagram

Chapter 9

Package

9.1 Package Information for MT2301

The MT2301 device is packaged in a 14mm×14mm, 128-pin Low-profile Quad Flat Package (LQFP) suitable for surface mounting, as shown in Figure 9.1.

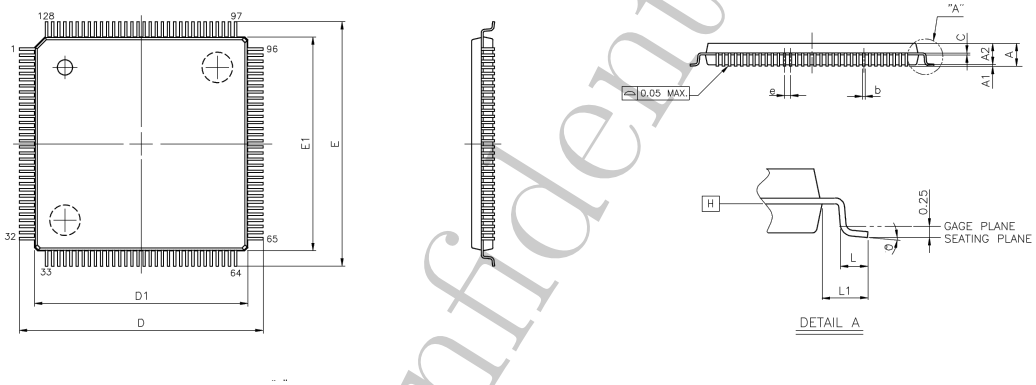

Figure 9.1: Package diagram

Symbol	Dimension (mm)			Dimension (MIL)		
	MIN	NOM.	MAX	MIN	NOM	MAX
A	-	-	1.60	-	-	62.99
A1	0.05	-	0.15	1.97	-	5.91
A2	1.35	1.40	1.45	53.15	55.12	57.09
b	0.13	0.16	0.23	5.12	6.30	9.06
c	0.09	-	0.20	3.54	-	7.87
D	16.00 BSC			629.9 BSC		
D1	14.00 BSC			551.2 BSC		
E	16.00 BSC			629.9 BSC		
E1	14.00 BSC			551.2 BSC		
e	0.40 BSC			15.7 BSC		
L	0.45	0.60	0.75	17.72	23.62	29.53
L1	1.00 REF			39.37 REF		
∘	0°	3.5°	7°	-	-	-

Table 9.1: Package dimensions

1. DATUM PLANE IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

Chapter 10

Ordering information

10.1 Ordering Information for MT2301

Part Number:
MT2301GL-xy: 1 port VDSL2 DMT chip with 128-LQFP package.

Prefix	Part No.	RoHS	Package type	Version
MT	2301	G: Green product N: Pb product	N:QFN P:QFP L:LQFP C:CHIP B:BGA	xy

Table 10.1: MT2301 part number explanation