November 2010

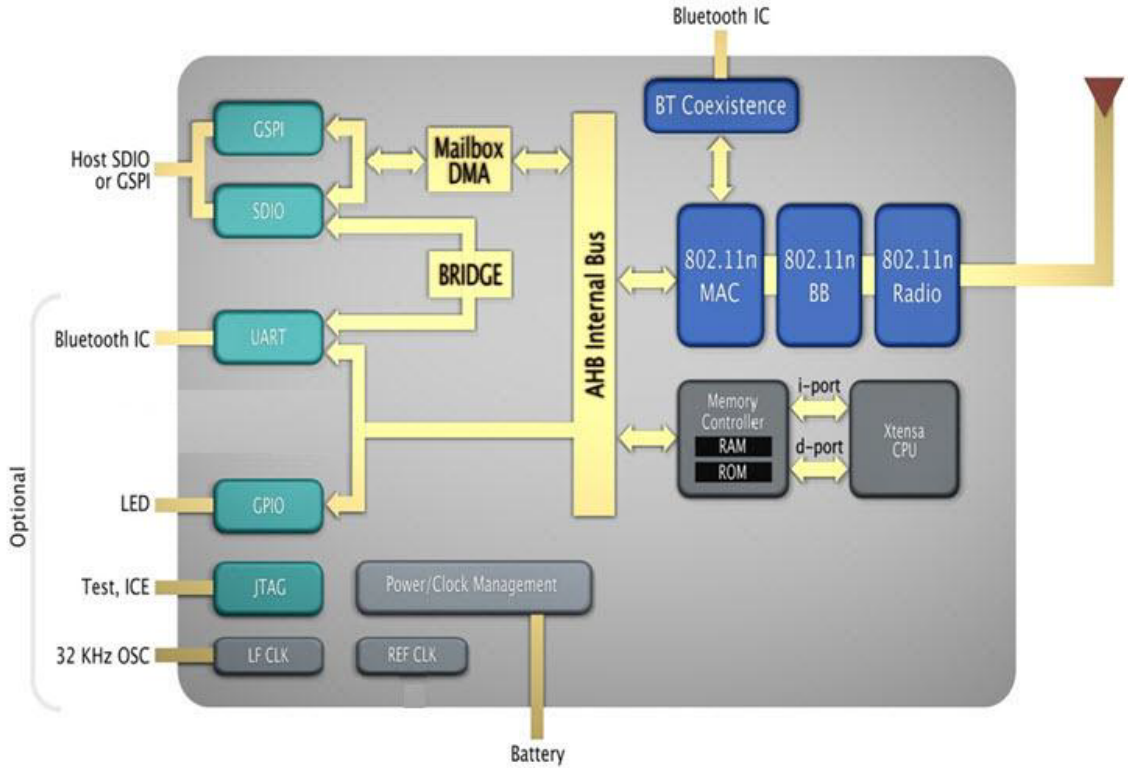
AR6103 ROCm™ Integrated 802.11n

General Description

The AR6103 is a complete, small form factor 802.11 b/g/n Wi-Fi solution optimized for low-power, low-cost, and highly integrated mobile and portable consumer electronic devices. The device integrates all Wi-Fi functionality in a package friendly to low-cost PCB design, requiring only a few external bypass capacitors and connection to an antenna.

The AR6103 is part of the 3rd generation ROCm™ family of mobile 11n devices, employing the world's lowest power consumption embedded architecture.

The AR6103 can support numerous external Bluetooth devices, and includes advanced PTA coexistence support. A flexible architecture enables optional customization to meet customer specific profiles and use cases.



AR6103 Block Diagram

On-chip high-efficiency high-output EPA™ power amplifier with zero calibration, integrated LNAs, integrated receive and transmit RF matching circuits, integrated reference crystal, and integrated T/R switch eliminate the need for external RF components and enable direct antenna connection.

Ultra low power consumption radio architecture and proprietary power save technologies extend battery life. On-chip high-efficiency PMU (power management unit) enables direct-connect to battery, eliminating the need for external regulators. An on-chip embedded CPU handles complete 11n processing to minimize host processor loading.

The AR6103 is available in a low profile 8.3mm x 9.2mm LGA package with 500um pitch pads for robust low-cost PCB design.

The AR6103 can be treated as a single -row QFN for direct on-board designs.

The AR6103 is halogen-free, Pb-free and fully ROHS compliant.

AR6103 Features

AR6103 High performance, ultra-low power, single stream (1x1) IEEE 802.11n featuring:

- Support for standard interfaces including SDIO 2.0 (50MHz, 4-bit and 1-bit)
- Integrated Sleep Clock eliminates the need for expensive bulky 32kHz real-time clock
- Integrated conformal RF shielding and near-zero RBOM for lowest cost
- Atheros proprietary AP Mode for mobile devices, and DirectConnect™ Peer-to-Peer connectivity.
- Half Guard Interval for high max throughput;
- Frame Aggregation for high max throughput;
- Space Time Block Coding (STBC) for improved downlink robustness over range; and
- Low Density Parity Check (LDPC) encoding for improved uplink robustness over range
- Near zero power consumption in idle and stand-by enables users to leave Wi-Fi always on"
- Integrated high-power, high efficiency linearized Power Amplifier
- Best in class Rx sensitivity for superior throughput rate-over-range performance
- Integrated reference crystal reduces BOM cost and foot-print.
- Completely integrated transmit/receive RF paths including balun, matching, and T/R switch for direct antenna connection.

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1. Features Summary

1.1 Overview

The AR6103 is a single package combination IEEE 802.11 (b, g, n) based on cutting edge technology from the AR6003 ROCm™ family of mobile 11n. The AR6103 contains 802.11 including full digital MAC and baseband engines handling all 802.11b (CCK), 11g/n (OFDM). An embedded low-power CPU cores minimize host loading and maximize flexibility to support customer specific profiles and use cases.

The AR6103 is architected for ultra-low power consumption, with near zero power consumption in idle and stand-by modes, enabling users to leave Wi-Fi "always on".

A pin-compatible standalone 802.11n plus advanced Bluetooth device (AR6133) is also available.

1.2 Radio Front End

The AR6103 features a high-power high-efficiency on-chip power amplifier that features the following:

- Atheros proprietary EPA™ linearization technology for Wi-Fi.
- Highly integrated LNAs .
- Integrated receive and transmit RF matching and switching enable direct antenna connection with high performance, low power consumption, and near-zero RBOM for lowest solution cost.

1.3 Power Management

The AR6103 features direct connection to battery, eliminating the need for external regulators and/or PMU. The AR6103 supports operating voltage from 4.2V down to 3.1V and is tolerant of momentary overvoltage up to 5.5V. An on-chip switching regulator supports PWM mode and burst mode to optimize power efficiency under both peak operation and low load conditions. An internal PMU with separate analog and digital LDO regulation provides superior noise isolation for analog and digital supplies.

An optional PMU bypass mode, disables the on-chip switching regulator to allow an external 1.8V regulated supply to directly power the device, if so desired.

The AR6103 power management engine utilizes advanced power save techniques such as: gating clocks to idle or inactive blocks, voltage scaling to specific blocks in certain states, fast start and settling circuits to reduce Tx and active duty cycles, CPU frequency scaling, and other techniques to optimize power consumption across all operation states.

1.4 Manufacturing Calibration

The AR6103 utilizes internal self-calibration and BIST (built-in self test) circuits to maintain optimal performance over temperature, time and process variation. The AR6103 is delivered fully tested and does not require any customer manufacturing line calibration.

1.5 Internal One-Time Programmable Memory

The AR6103 includes internal one-time programmable memory which may be used to store the device MAC address, eliminating the need for external EEPROM.

1.6 Reference Frequency

The AR6103 incorporates an on-chip 26MHz (20ppm) reference frequency source. Internally, the system reference frequency is sleep regulated and gated to enable the internal crystal to be powered down when the device is in sleep mode. Manufacturing calibration of the crystal is not required, but is supported as an option.

1.7 Internal Sleep Clock

The AR6103 incorporates integrated on-chip low power sleep clocks to regulate internal timing, eliminating the need for any external 32kHz real time clocks or crystal oscillators.

1.8 Interfaces

The AR6103 supports SDIO 1.x and the latest 2.0 standard.

1.8.1 Standard Host Interface

The AR6103 supports industry standard SDIO 2.0 (50MHz, 4-bit and 1-bit) and GSPI (Generic SPI) for Wi-Fi.

1.9 Mobile 802.11n

The AR6103 incorporates the latest generation of mobile 802.11n technology from Atheros. The AR6103 is draft 802.11n compliant and features Frame aggregation, reduced inter-frame spacing (RIFS) and half guard intervals for improved throughput and space time block codes (STBC) on downlink receptions and Low Density Parity Check (LDPC) codes on uplink transmissions for improved robustness over range. Table 1-1 shows the 1 802.11n (PHY layer) throughput at different modulations.

Table 1-1. **802.11n (PHY layer) Throughput at Different Modulations**

Mode	MCS	Modulation	Data Rate (Mbps)	
			20MHz Channel Bandwidth	
			Full Guard Interval	Half Guard Interval
IEEE 802.11n	0	BPSK	6.5	7.2
	1	QPSK	13.0	14.4
	2	QPSK	19.5	21.7
	3	16-QAM	26.0	29.9
	4	16-QAM	39.0	43.3
	5	64-QAM	52.0	57.8
	6	64-QAM	58.5	65.0
	7	64-QAM	65.0	72.2

Host interface design optimized for high throughput, low latency, and very low host loading enable high effective throughput. See Table 1-2.

Table 1-2. **Effective 802.11n Throughput**

MCS	Modulation	TCP Data Rate (Mbps)	
		20MHz Channel Bandwidth	
		Full Guard Interval	Half Guard Interval
0	BPSK	5.6	6.1
1	QPSK	10.9	12.0
2	QPSK	16.1	17.7
3	16-QAM	21.1	23.3
4	16-QAM	30.5	33.5
5	64-QAM	39.2	40.8
6	64-QAM	43.4	47.4
7	64-QAM	47.4	51.8
MCS	**Modulation**	**UDP Data Rate (Mbps)**	
0	BPSK	6.1	6.7
1	QPSK	12.0	13.3
2	QPSK	17.8	19.8
3	16-QAM	23.5	26.0
4	16-QAM	34.5	38.0
5	64-QAM	44.8	49.3
6	64-QAM	49.9	54.7
7	64-QAM	54.7	60.1

Host CPU running 88MHz, SDIO 2.0, 8-subframe per A-MPDU and host assisted re-ordering

The AR6103 is fully compliant with IEEE 802.11e QoS, Wi-Fi Alliance WMM® Power Save and 802.11n power saving, ensuring the lowest possible power consumption.

The AR6103 features hardware-based AES, AES-CCMP, and TKIP engines for faster data encryption, and supports industry leading security features including Cisco CCXv4 ASD, WAPI (for China), Wi-Fi Protected Setup (WPS), along with standard WEP/WPA/WPA2 for personal and enterprise environments.

1.10 Advanced Wi-Fi Features

Advanced features such as Host wake-on-wireless and ARP (address resolution protocol) off-loading enable the Wi-Fi link to remain associated for extended periods with host processor asleep for additional deep system power savings.

Other standard Wi-Fi features include:

- WWR, 802.11d, 802.11h
- Wi-Fi Protected Setup (WPS)

- Device based scanning & roaming, tunable parameters optimized for seamless handover
- Statistics and events for monitoring
- Self-managed power state handling
- Self-contained beacon processing
- Shared authentication
- Adhoc power save
- Multiple PMK Id support
- Simulated UAPSD
- T-Spec support
- Production flow diagnostics
- Dynamic PS-Polling for enhanced coexistence performance with Bluetooth
- QoS support for VoIP applications

1.10.1 AP Mode (Mobile Hot Spot)

Atheros industry leading AP Mode feature allows the AR6103 device to operate as both a station and an Access Point, enabling seamless station-to-station interconnection with all the benefits of standard infrastructure-level simplicity (no special client software or settings required), security, and power save functionality. AP Mode enables the deployment of unique and powerful applications such as mobile 3G gateway and mobile range extension.

1.10.2 DirectConnect™ (Peer-to-Peer)

Atheros industry leading DirectConnect™ implementation of advanced peer-to-peer connectivity enables faster device-to-device data & media transfer, improved network efficiency eliminating the 'hop' through the access point, simultaneous connection to device and the internet, and simple PAN setup (with Wi-Fi Protected Setup), all with reduced power consumption to extend battery life.

1.11 Host Offloading (Wi-Fi)

The AR6103 integrates extensive hardware signal processing and an embedded on-chip CPU to offload complete 11n MAC/BB/PHY processing to minimize host processor loading and support application specific customization for gaming and mobile phones.

The AR6103 offloads the complete 802.11 a/b/g/n baseband and MAC functions as standard feature, including:

- Link Maintenance
- 802.11 frame transmission sequence to initiate the connection with an Acces Point;
- Background scanning, including transmission of Probe Request;
- Signal quality detection and automated maintenance of current Access Point list;
- Roaming to a new Access Point
- Rate Adaptation, including automatic retry
- Encapsulation of 802.3 frames from the host to 802.11 frames. This includes adding the security headers for 802.11
- Decapsulation of the 802.11 frame to 802.3 frame
- Encryption & decryption (hardware ciphers) for WEP/TKIP/AES-CCMP, and WAPI
- IEEE PowerSave. Periodic wakeup when in sleep mode to check for buffered traffic
- Packet Filtering and Host Wakeup, including ARP (Address Resolution Protocol) Response. Automated filtering of received data in the sleep mode to transfer only data packets of interest to the host.
- Frame Aggregation (A-MPDU) processing
- LDPC encode and STBC processing

Additionally, the AR6103 also provides host offloading of the following advanced features:

- TCP Checksum
- Security Negotiation

1.11.1 TCP Checksum

The AR6103 can compute the complete TCP checksum.

1.11.2 Security Negotiation

The AR6103 can perform initial and subsequent 4-way handshake offload, and initial Group Key exchange and Re-Keying.

2. Wi-Fi Functional Description

2.1 Overview

The AR6103 is a single chip 802.11 b/g/n device based on cutting edge technology, optimized for low power embedded applications. The typical data path consists of the host interface, mailbox DMA, AHB, memory controller, MAC, BB, and radio. The CPU drives the control path via register and memory accesses. External interfaces include SDIO or GSPI, reference clock, and front-end components as well as optional connections such as UART, GPIO, JTAG, 32 kHz source. See the AR6103 block diagram.

2.2 XTENSA CPU

At the heart of the chip is the XTENSA CPU. This CPU has four interfaces:

- The Code RAM/ROM interface (iBus), going to the Virtual Memory Controller (VMC).
- The Data RAM Interface (dBus), going to the VMC
- The AHB interface, used mainly for register accesses.
- JTAG interface for debugging

2.3 Virtual Memory Controller (VMC)

The VMC contains 256 kBytes of ROM and 256 kBytes of RAM. It has three interfaces:

- iBus,
- dBus, and
- AHB interface.

Any one of these interfaces can request access to the ROM or RAM modules within the VMC. The VMC contains arbiters to serve these three interfaces on a first-come-first-serve basis.

2.4 AHB and APB Blocks

The AHB block acts as an arbiter. It has AHB interfaces from three Masters:

- MAC,
- MBOX (from the Host), and
- CPU.

See below for more on the MBOX and MAC. Depending upon the address, the AHB data request can go into one of the two slaves: APB block or the VMC. Data requests to the VMC are generally high-speed memory requests, while requests to the APB block are primarily meant for register access.

The APB block acts as a decoder. It is meant only for access to programmable registers within the AR6103's main blocks. Depending on the address, the APB request can go to one of the places listed below:

- Radio
- VMC
- MBOX
- GPIO
- UART
- Real Time Clock (RTC), or
- MAC/BB

2.5 GPIO

The AR6103 has 14 configurable GPIO pins configured by software. Some are simple GPIO pins like host mode and wake-on-wireless; others are multiplexed with hardware functions such as the host interface, UART, Bluetooth coexistence, 32KHz sleep clock, and debugging. Though most GPIOs have predetermined functions, a few of them such as TCK and TDI, are typically free for custom application such as LED control.

Each GPIO supports the following configurations via software programming:

- Internal pull-up/down options
- Input available for sampling by a software register
- Input triggering an edge or level CPU interrupt
- Input triggering a level chip wakeup interrupt
- Open-drain or push-pull output driver
- Output source from a software register or the Sigma Delta Pulse-width Modulation (PWM) DAC

The AR6103 has one Sigma Delta PWM DAC that is shared by all of the GPIO pins. It allows the GPIO pins to approximate intermediate output voltage levels. The DAC has a period of 256 samples with a software controllable duty cycle. In applications where the AR6103 is driving LEDs using GPIO pins, the Sigma

Delta PWM DAC can provide a continuous dimmer function.

2.6 MBOX

The MBOX is a service module to handle one of two possible external hosts: SDIO or GSPI. The AR6103 can handle only one of these hosts at any given time. The type of host the AR6103 uses depends upon the polarity of some package pins upon system power-up. The MBOX has two interfaces: an APB interface for access to the MBOX registers and an AHB interface which is used by the external host to access the VMC memory or other registers within the AR6103.

2.7 Debug UART

The AR6103 includes a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface that is fully compatible with the 16550 UART industry standard. This UART is a general purpose UART although it is primarily used for debug.

2.8 Reset Control

The AR6103 CHIP_PWD_L pin can be used to completely reset the entire chip. After this signal has been de-asserted, the AR6103 waits for host communication. Until then, the MAC, BB, and SOC blocks are powered off and all modules except the host interface are held in reset.

Once the host has initiated communication, the AR6103 turns on its crystal and later on its PLL. After all clocks are stable and running, the resets to all blocks are automatically de-asserted. The only resets that stay asserted are given below:

- Warm and cold resets to the MAC
- Warm reset to the radio (The cold reset gets automatically de-asserted)

The above resets are deasserted by software. All AR6103 reset control logic resides in the RTC block to ensure stable reset generation.

2.8.1 CPU Reset

CPU reset is different from the other resets mentioned above. There are four scenarios where the CPU reset can be asserted:

1. The AR6103 CHIP_PWD_L pin is asserted or the host has not initiated communication.
2. The polarity of certain package pins are set to enable JTAG debugging via an In-Circuit Emulator (ICE). In this case, the external ICE can assert CPU reset through a package pin.
3. The polarity of a package pin is set to hold the CPU in reset until the host clears an internal AR6103 register.
4. An internal AR6103 register is set by the host to force the CPU out of an unknown state.

2.9 Reset Sequence

After a COLD_RESET event (e.g., the host toggles CHIP_PWD_L) the AR6103 will enter the HOST_OFF state and await communication from the host. From that point, the typical AR6103 COLD_RESET sequence is shown below:

1. When the host is ready to use the AR6103, it initiates communication via SDIO or GSPI.
2. The AR6103 enters the WAKEUP state then the ON state and enables the XTENSA CPU to begin executing ROM code. Software configures the AR6103 functions and interfaces. When the AR6103 is ready to receive commands from the host, it will set an internal function ready bit.
3. The host reads the ready bit and can now send function commands to the AR6103.
4. The CPU may continue to be held in reset under some circumstances until its reset is cleared by an external pin or when the host clears a register.
5. The MAC cold reset and the MAC/BB warm reset will continue to stay asserted until their respective reset registers are cleared by software.

2.10 Power Management Unit

The AR6103 has a an integrated Power Management Unit (PMU) which generates all the power supplies required by its internal circuitry from an external battery connection. The only supplies needed by the AR6103 are the battery input (4.2V - 3.1V) and the host and SOC I/O supplies (1.8V - 3.3V).

The main components of the PMU are as follows:

- A switching regulator (SWREG) which produces a 1.8V supply from the battery input.

- A small linear regulator (SREG) which converts the host IO supply to a 1.2V supply for some small control blocks which are turned on when CHIP_PWD_L is de-asserted.
- A larger linear regulator (DREG) which converts the 1.8V input to 1.2V for the bulk of AR6103 core digital circuitry. The input is typically connected to the SWREG output.
- A linear regulator (PAREG) which converts the battery input to a 3.3V supply that can be used for the antenna switch controls as well as the internal AR6103 EPA.

In applications where external supplies are already present, the AR6103 supports bypassing all supplies generated by the PMU.

2.11 Power Transition Diagram

The AR6103 provides integrated power management and control functions and extremely low power operation for maximum battery life across all operational states by:

- Gating clocks for logic when not needed
- Shutting down unneeded high speed clock sources
- Reducing voltage levels to specific blocks in some states

When the AR6103 is in a low power state, the switching power supply (SWREG) as well as the main 1.2V regulator for digital circuits (DREG) are both turned off. All digital circuits that normally rely upon 1.2V power from DREG are switched to use power from the smaller SREG regulator using a "Make-and-Break" mechanism.

2.11.1 Hardware Power States

AR6103 hardware has five top level hardware power states managed by the RTC block. Table 2-1 describes the input from the MAC, CPU, SDIO/MBOX, interrupt logic, and timers that affect the power states.

2.11.2 Sleep State Management

Sleep state minimizes power consumption while saving system states. In SLEEP state, all high speed clocks are gated off and the external reference clock source is powered off. The SWREG, DREG, and PAREG supplies are also turned off during SLEEP. For the AR6103 to enter SLEEP state, the MAC, MBOX, and CPU systems must not be active.

The system remains in sleep state until a WAKEUP event causes the system to enter WAKEUP state, wait for the reference clock source to stabilize, and then ungate all enabled clock trees. The CPU wakes up only when an interrupt arrives, which may have also generated the system WAKEUP event.

Figure 2-1 depicts the state transition diagram.

Table 2-1. **Power Management States**

State	Description
OFF	CHIP_PWD_L pin assertion immediately brings the chip to this state.
	Sleep clock is disabled.
	No state is preserved.
	Host power LDO and PMU regulators turned OFF.
HOST_OFF	WLAN is turned OFF.
	Only the host interface is powered on - the rest of the chip is power gated OFF.
	The host instructs the AR6103 to transition to WAKEUP by writing a register in the host interface domain.
	Embedded CPU and WLAN do not retain state (separate entry).
	This state can be bypassed by asserting FORCE_HOST_ON_L during CHIP_PWD_L deassertion.
SLEEP	Only the sleep clock is operating.
	The reference clock is disabled.
	Any wakeup events (MAC, host, LF-Timer, GPIO-interrupt) will force a transition from this state to the WAKEUP state.
	All internal states are maintained.
WAKEUP	The system transitions from sleep states to ON. WAKEUP duration is programmable.
ON	The high speed clock is operational and sent to each block enabled by the clock control register.
	Lower level clock gating is implemented at the block level, including the CPU, which can be gated OFF using the WAITI instruction while the system is ON. No CPU, host, and WLAN activities will transition to sleep states.

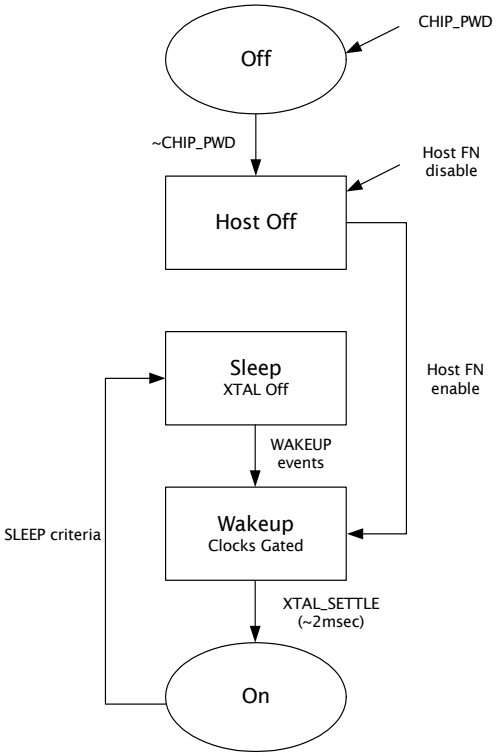


Figure 2-1. **AR6103 Power State**

2.12 System Clocking (RTC Block)

The AR6103 has an RTC block which controls the clocks and power going to other internal modules. Its inputs consist of sleep requests from these modules and its outputs consists of clock enable and power signals which are used to gate the clocks going to these modules. The RTC block also manages resets going to other modules with the device. The AR6103's clocking is grouped into two types: high-speed and low-speed.

2.12.1 High Speed Clocking

The reference clock source drives the PLL and RF synthesizer within the AR6103. It can be either an external crystal or oscillator. To minimize power consumption, the reference clock source is powered off in SLEEP, HOST_OFF, and OFF states. For an external crystal, the AR6103 disables the on-chip oscillator driver. For an external oscillator, the AR6103 de-asserts its CLK_REQ_OUT signal to indicate that a reference clock is not needed.

When exiting SLEEP state, the AR6103 waits in WAKEUP state for a programmable duration. During this time, the CLK_REQ_OUT signal is asserted to allow for the reference clock source to settle. The CLK_REQ_OUT signal remains asserted in ON state.

2.12.2 Low-Speed Clocking

The AR6103 has eliminated the need for an external sleep clock source thereby reducing system cost. Instead, an internal ring oscillator is used to generate a low frequency sleep clock. It is also used to run the state machines and counters inside the AR6103's Power Control Module (PCM). The PCM controls all power and isolation control signals for the entire chip.

The AR6103 has an internal calibration module which produces a 32.768 KHz output with minimal variation. For this, it uses the reference clock source as the golden clock. As a result, the calibration module adjusts for process and temperature variations in the ring oscillator when the system is in ON state.

The AR6103 also supports using an external low frequency sleep clock source in applications where one is already available.

2.12.3 Sleep Clock Option

The AR6103 features on internal low frequency sleep clock and therefore, does not require an external sleep clock source. Designs which use the internal sleep clock, must ground the LF_CLKIN pin. The ideal frequency of the sleep clock is 32768 Hz.

2.12.4 Interface Clock

The host interface clock represents another clock domain for the AR6103. This clock comes from the SDIO or GSPI host and is completely independent from the other internal clocks. It drives the host interface logic as well as certain registers which can be accessed by the host in HOST_OFF and SLEEP states.

2.13 Front End Control

For applications that use external front-end components, the AR6103 provides the ability to control them with three antenna switch control outputs named as follows:

- ANTE
- ANTD
- ANTC

A programmable switch table indexed by transceiver state offers flexibility for various front-end configurations. The AR6103 supports antenna sharing with another wireless chip in all power states by using ANTE to control the shared antenna switch.

2.14 MAC/BB/RF Block

The AR6103 Wireless MAC consists of five major blocks:

- Host interface unit (HIU) for bridging to the AHB for VMC data accesses and APB for register accesses
- Ten queue control units (QCU) for transferring TX data
- Ten DCF control units (DCU) for managing channel access
- Protocol control unit (PCU) for interfacing to baseband
- DMA receive unit (DRU) for transferring RX data

2.15 Baseband Block

The AR6103 baseband module (BB) is the physical layer controller for the 802.11a/b/g/n air interface. It is responsible for modulating data packets in the transmit direction, and detecting and demodulating data packets in the receive direction. It has a direct control interface to the radio to enable hardware to adjust analog gains and modes dynamically.

2.16 Design for Test

The AR6103 has a built in JTAG boundary scan of its pins. It also has features which enable testing of digital blocks via ATPG scan, memories via MBIST, analog components, and the radio.

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 summarizes the absolute maximum ratings and Table 3-2 lists the recommended operating conditions for the AR6103. Absolute maximum ratings are those values beyond which damage to the device can occur.

Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

NOTE: Maximum rating for signals follows the supply domain of the signals.

Table 3-1. **Absolute Maximum Ratings**

Symbol (Domain)	Parameter	Max Rating	Unit
AVDD18	Analog 1.8V supply	-0.3 to 2.5	V
VDDIO	GPIO I/O supply	-0.3 to 4.0	V
HOST_POWER	Host interface I/O supply	-0.3 to 4.0	V
VDD33	Antenna and PA 3.3V supply	-0.3 to 4.0	V
PAREG_BASE	External 3.3V supply	-0.3 to 4.0	V
VAT_42	External 3.3V supply	-0.3 to 4.8	V
RF_{in}	Maximum RF input (reference to 50-ohm input)	+12 (including switch and balun loss)	dBm
T_{store}	Storage temperature	-45 to 135	°C
ESD	Electrostatic discharge tolerance	2000	V

3.2 Recommended Operating Conditions

Table 3-2. **Recommended Operating Conditions**

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
AVDD18	Analog 1.8V supply	1.71	1.8	1.89	V
VDDIO	GPIO I/O supply	1.71		3.46	V
HOST_POWER	Host interface I/O supply	1.71		3.46	V
VDD33_PA	Antenna and PA 3.3V supply	3.14		3.46	V
PAREG_BASE	External 3.3V supply	3.14	3.3	3.46	V
VAT_42 (with PMU)	External 3.3V supply	3.2	3.7	4.2	V
VAT_42 (without PMU)	External 3.3V supply	3.2	3.7	4.2	V
$T_{ambient}$	Ambient temperature	-40		85	°C

3.3 DC Electrical Characteristics

Table 3-3 and Table 3-4 list the general DC electrical characteristics over recommended operating conditions (unless otherwise specified).

Table 3-3. **General DC Electrical Characteristics (For 3.3 V I/O Operation)**

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage			0.7 x V_{DD}			V
V_{IL}	Low Level Input Voltage					0.3 x V_{DD}	V
I_{IL}	Input Leakage Current	Without Pull-up or Pull-down	0 V < V_{IN} < V_{DD} 0 V < V_{OUT} < V_{DD}	0		-3	nA
		With Pull-up	0 V < V_{IN} < V_{DD} 0 V < V_{OUT} < V_{DD}	16		48	µA
		With Pull-down	0 V < V_{IN} < V_{DD} 0 V < V_{OUT} < V_{DD}	-14		-47	µA
V_{OH}	High Level Output Voltage		I_{OH} = -4mA	0.9 x V_{DD}			V
			I_{OH} = -12mA	0.9 x V_{DD}			V
V_{OL}	Low Level Output Voltage		I_{OH} = 4mA			0.1 x V_{DD}	V
			I_{OH} = 12mA			0.1 x V_{DD}	V

Table 3-4. **General DC Electrical Characteristics (For 1.8 V I/O Operation)**

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage			0.7 x V_{DD}			V
V_{IL}	Low Level Input Voltage					0.3 x V_{DD}	V
I_{IL}	Input Leakage Current	Without Pull-up or Pull-down	0 V < V_{IN} < V_{DD} 0 V < V_{OUT} < V_{DD}	0		-3	nA
		With Pull-up	0 V < V_{IN} < V_{DD} 0 V < V_{OUT} < V_{DD}	3.5		13	µA
		With Pull-down	0 V < V_{IN} < V_{DD} 0 V < V_{OUT} < V_{DD}	-6.2		-23	µA
V_{OH}	High Level Output Voltage		I_{OH} = -4mA	0.9 x V_{DD}			V
			I_{OH} = -12mA	0.9 x V_{DD}			V
V_{OL}	Low Level Output Voltage		I_{OH} = 4mA			0.1 x V_{DD}	V
			I_{OH} = 12mA			0.1 x V_{DD}	V

The following two figures show the recommended power up/down and reset sequences for the AR6103 using external 3.3V and 1.8V supplies. We suggest that you add Host_Power and VDDIO in the power on/off timing.

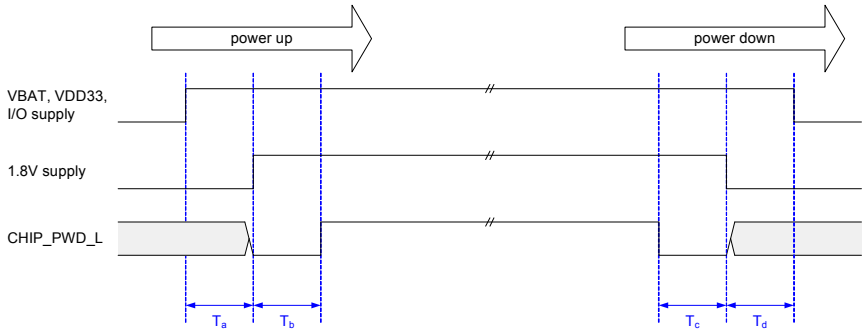


Figure 3-1. **Power Up/Power Down Timing**

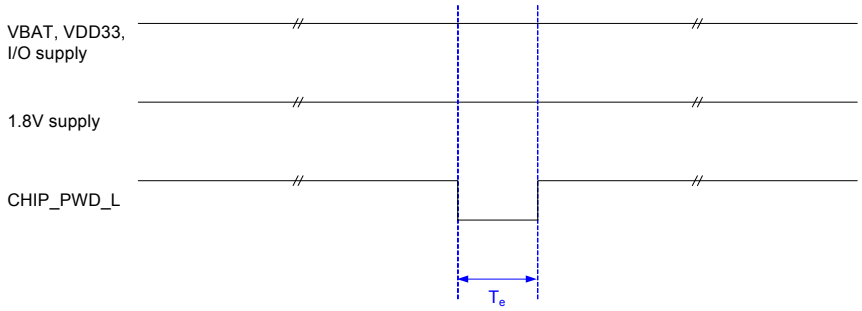


Figure 3-2. **Reset and Power Cycle Timing**

VBAT = VBATTERY_42

VDD33 = VDD33_ANT, VDD33_PA, PAREG_BASE

I/O = DVDD_SDIO, DVDD_SOC1, DVDD_SOC2, VDD18_XTAL

1.8V supply = VREG, AVDD18

Table 3-5. **Timing Diagram Definitions**

	Description	**Min (**μsec)
T_a	Time between VBAT, VDD33, and I/O supplies valid and 1.8V supply valid[1]	0
T_b	Time between 1.8V supply valid and CHIP_PWD_L deassertion	5
T_c	Time between CHIP_PWD_L assertion and 1.8V supply invalid	0
T_d	Time between 1.8V supply invalid and VBAT, VDD33, and I/O supplies invalid	N/A[2]
T_e	Length of CHIP_PWDP_L pulse	5

[1]Supply valid represents the voltage level has reached 90% level.
[2]No strict requirements. This parameter can also be negative.

3.4 Radio Receiver Characteristics

Table 3-6 summarize the AR6103 receiver characteristics.

Table 3-6. **Receiver Characteristics for 2.4 GHz Operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{rx}	Receive input frequency range		2.412		2.484	GHz
NF	Receive chain noise figure (max gain)					dB
S_{rf}	Sensitivity					
	CCK, 1 Mbps	[1]		-97		dBm
	CCK, 2 Mbps			-93		
	CCK, 5.5 Mbps			-91		
	CCK, 11 Mbps			-89		
	OFDM, 6 Mbps			-93		
	OFDM, 9 Mbps			-92		
	OFDM, 12 Mbps			-91		
	OFDM, 18 Mbps			-88		
	OFDM, 24 Mbps			-85		
	OFDM, 36 Mbps			-82		
	OFDM, 48 Mbps			-77		
	OFDM, 54 Mbps			-76		
	HT20, MCS0			-93		
	HT20, MCS1			-90		
	HT20, MCS2			-88		
	HT20, MCS3			-83		
	HT20, MCS4			-81		
	HT20, MCS5			-76		
	HT20, MCS6			-74		
	HT20, MCS7			-73		
IP1dB	Input 1 dB compression (min. gain)					dBm
IIP3	Input third intercept point (min. gain)					dBm
ER_{phase}	I, Q phase error					degree
ER_{amp}	I, Q amplitude error					dB
R_{adj}	Adjacent channel rejection					
	OFDM, 6 Mbps	[1]		37		dB
	OFDM, 54 Mbps			21		
	HT20, MCS0			37		
	HT20, MCS7			20		
TR_{powup}	Time for power up					µs

[1]Performance based on the AR5BSD-00031A with balun, Tx/Rx switch (~1dB loss). Excludes cellular coexistence filter.

3.5 Radio Transmitter Characteristics

Table 3-7 summarize the transmitter characteristics for AR6103.

Table 3-7. **Transmitter Characteristics for 2.4 GHz operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range		2.412		2.484	GHz
P_{out}	Output power	[1]				
	11b mask compliant	1Mbps		18.5		dBm
	11g mask compliant	6Mbps		19		
	11n HT20 mask compliant	MCS0		18.5		
	11g EVM compliant	54Mbps		16.5		
	11n HT20 EVM compliant	MCS7		13		
SP_{gain}	PA gain step					dB
A_{pl}	Accuracy of power leveling loop	[2]		±1.5		dB
OP1dB	Output P1dB (max. gain)					dBm
OIP3	Output third order intercept point (max. gain)					dBm
SS	Sideband suppression					dBc
TT_{powup}	Time for power up					µs

[1]Performance based on the AR5BSD-00031A with balun, Tx/Rx switch (~1dB loss), excludes cellular coexistence filter.
[2]Performance based on the AR5BSD-00031A after calibration.

NOTE: All transmitter characteristics are preliminary and to subject to change without notice.

3.6 AR6103 Synthesizer Characteristics

Table 3-8 summarize the synthesizer characteristics for the AR6103.

Table 3-8. **Synthesizer Composite Characteristics for 2.4 GHz Operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pn	Phase noise (at Tx_Out) At 30 KHz offset At 100 KHz offset At 500 KHz offset At 1 MHz offset					dBc/Hz
F_c	Center channel frequency	Center frequency at 5MHz spacing[1]	2.412		2.484	GHz
F_{ref}	Reference oscillator frequency	±20ppm		26		MHz
F_{step}	Frequency step size (at RF)			1		MHz
TS_{powup}	Time for power up (from sleep)			0.2		ms

[1]Frequency is measured at the Tx output.

3.7 Typical Power Consumption Performance

Table 3-9. **AR6103 Typical Current Consumption – Low Power States (Individual Voltage Rails)**

Mode		Typical Current Consumption [mA]	
		1.8V[1]	3.3V[2]
Standby	OFF	0.000	0.004
	HOST_OFF	0.043	0.005
	SLEEP	0.210	0.005
IEEE PS[3] (2.4GHz)	DTIM=1	2.011	0.005
	DTIM=3	0.868	0.005
	DTIM=10	0.467	0.005
IEEE PS[4] (5GHz)	DTIM=1	2.159	0.173
	DTIM=3	0.921	0.066
	DTIM=10	0.488	0.029

[1]AVDD18, VDDIO
[2]PAREG_BASE, VBAT_42, VDD33
[3]Calculated assuming Rx time of 2ms + 0.1* DTIM
[4]Calculated assuming Rx time of 2ms + 0.1* DTIM

3.7.1 Measurement Conditions for Low Power States

- T_ambient = 25C
- All I/O pins except CHIP_PWD_L are maintained at their default polarities (I/Os without default internal pulls are pulled low).

.

Table 3-10. **AR6103 Typical Current Consumption [2.4 GHz operation] – Continuous Receive (Individual Voltage Rails)**

Mode/Rate [Mbps]	Typical Current Consumption [mA]		
	1.8V[1]	3.3V[2]	I/O[3]
CCK, 1 Mbps	81	0	5
CCK, 11 Mbps	82	0	5
OFDM, 6 Mbps	83	0	5
OFDM, 54 Mbps	85	0	5
HT20, MCS0	84	0	5
HT20, MCS7	86	0	5

[1]AVDD18
[2]PAREG_BASE, VBAT_42, VDD33
[3]VDDIO

3.7.2 Measurement Conditions for Continuous Receive [2.4 GHz Operation]

- T_ambient = 25C
- Measured using AR5BSD-00031A with AR6103 Atheros Radio Test software running in broadcast throughput receive mode

Table 3-11. **AR6103 Typical Current Consumption [2.4 GHz operation] – Continuous Transmit (Individual Voltage Rails)**

Mode/Rate [Mbps]	Target Output Power [dBm]	Typical Current Consumption [mA]		
		1.8V[1]	3.3V[2]	I/O[3]
CCK, 1 Mbps	18.5	58	177	5
CCK, 11 Mbps	18.5	58	175	5
OFDM, 6 Mbps	19.0	64	168	5
OFDM, 54 Mbps	16.5	65	123	5
HT20, MCS0	18.5	64	163	5
HT20, MCS7	13.0	65	99	5

[1]AVDD18
[2]PAREG_BASE, VBAT_42, VDD33
[3]VDDIO

3.7.3 Measurement Conditions for Continuous Transmit [2.4 GHz Operation]

- T_ambient = 25C
- Measured using AR5BSD-00031A with AR6103 Atheros Radio Test software running in continuous transmit mode.
- Output power is targeted on AR5BSD-00031A with balun, Tx/Rx switch (~1dB loss). Excludes cellular coexistence filter.

4. Pin Assignments and Descriptions

This chapter describes the pin assignment of the AR6103.

The following nomenclature is used for signal description described in this chapter.

NC	No Connection should be made to this pin
_L	Suffix at the end of the signal name indicating active low signal
A_I/O	Analog signal
I	Digital input signal
PU	Weak internal pull-up, input can be left floating (not connected)
PD	Weak internal pull-down, input can be left floating (not connected)
I/O	A digital bidirectional signal
O	A digital output signal
P	A power or ground pin
N/A	Not applicable
X	Indeterminate, floating inputs must be externally driven high or low

Figure 4-1 shows the PCB footprint and pin assignments (bottom view of the chip) of the AR6103.

Table 4-1 and Table 4-2 show pin assignments and pin definitions.

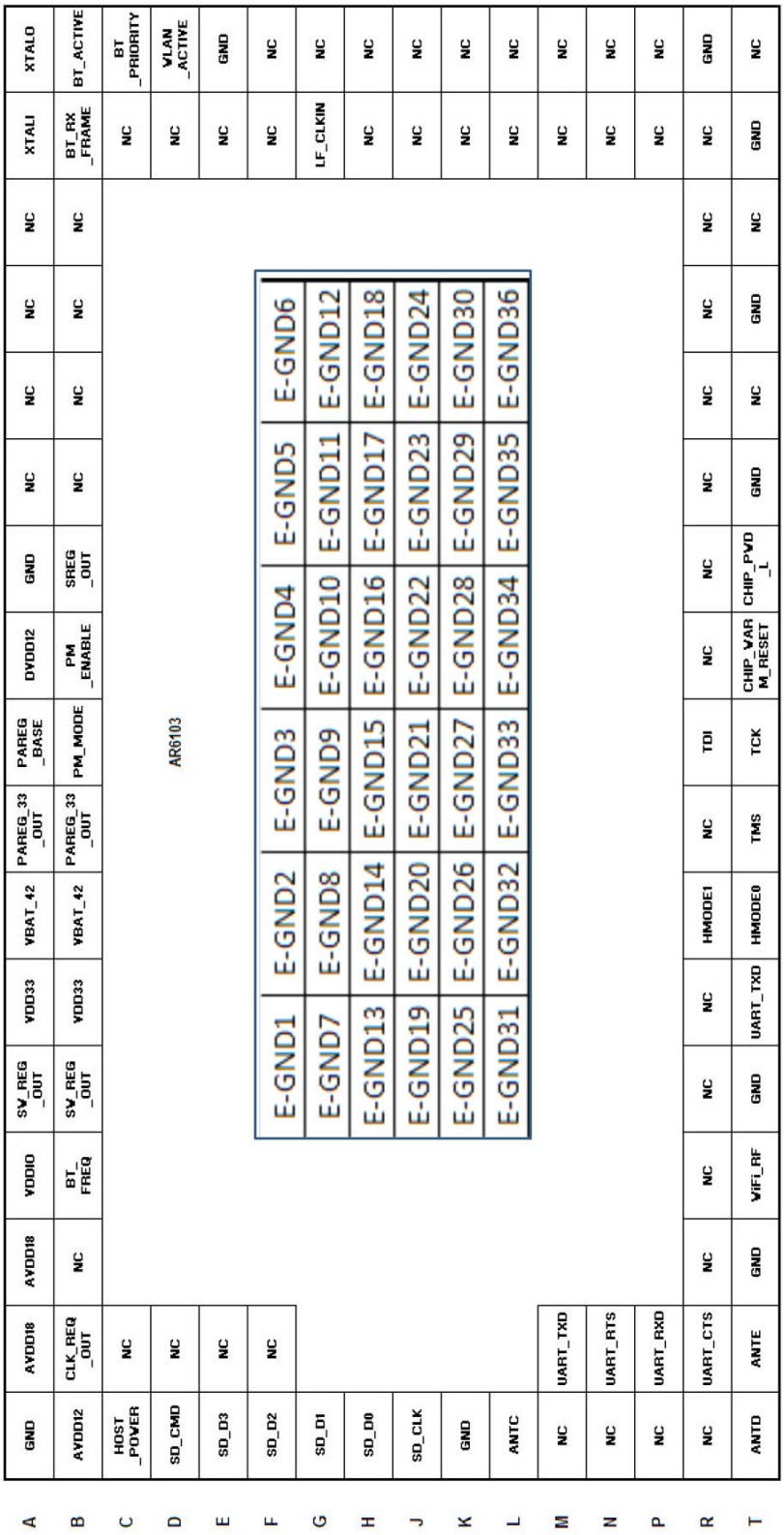


Figure 4-1. **AR6103 Pin Assignment & Ball-out Drawing**

Table 4-1. AR6103 Pin Assignments and Descriptions

Pin No.	Pin Name	Pin No.	Pin Name
A1	GND	J1	SD_CLK
A2	AVDD18	J16	NC
A3	AVDD18	J17	NC
A4	VDDIO	K1	GND
A5	SW_REG_OUT	K16	NC
A6	VDD33	K17	NC
A7	VBAT_42	L1	ANTC
A8	PAREG_33_OUT	L16	NC
A9	PAREG_BASE	L17	NC
A10	DVDD12	M1	NC
A11	GND	M2	UART_TXD
A12	NC	M16	NC
A13	NC	M17	NC
A14	NC	N1	NC
A15	NC	N2	UART_RTS
A16	XTALI	N16	NC
A17	XTALO	N17	NC
B1	AVDD12	P1	NC
B2	CLK_REQ_OUT	P2	UART_RXD
B3	NC	P16	NC
B4	BT_FREQ	P17	NC
B5	SW_REG_OUT	R1	NC
B6	VDD33	R2	UART_CTS
B7	VBAT_42	R3	NC
B8	PAREG_33_OUT	R4	NC
B9	PM_MODE	R5	NC
B10	PM_ENABLE	R6	NC
B11	SREG_OUT	R7	HMODE1
B12	NC	R8	NC
B13	NC	R9	TDI
B14	NC	R10	NC
B15	NC	R11	NC
B16	BT_REG_FRAME	R12	NC
B17	BT_ACTIVE	R13	NC
C1	HOST_POWER	R14	NC
C2	NC	R15	NC

Table 4-1. AR6103 Pin Assignments and Descriptions

Pin No.	Pin Name	Pin No.	Pin Name
C16	NC	R16	NC
C17	BT_PRIORITY	R17	GND
D1	SD_CMD	T1	ANTD
D2	NC	T2	ANTE
D16	NC	T3	GND
D17	WLAN_ACTIVE	T4	WiFi_RF
E1	SD_D3	T5	GND
E2	NC	T6	TDO (DEBUG_UART_TXD)
E16	NC	T7	HMODE0
E17	GND	T8	TMS
F1	SD_D2	T9	TCK
F2	NC	T10	CHIP_WARM_RESET
F16	NC	T11	CHIP_PWD_L
F17	NC	T12	GND
G1	SD_D1	T13	NC
G16	LF_CLKIN	T14	GND
G17	NC	T15	NC
H1	SD_D0	T16	GND
H16	NC	T17	NC
H17	NC	E-GND 1..36	GND

Table 4-2. AR6103 Pin Definitions

Pin No.	Pin Name	Type	Description	Reset State	I/O Pad Supply Domain
			Power Supply		
A1,A11,K1, R17,T3,E17, T5,T12,T14, T16	GND	P	All ground pins must be grounded, follow design note recommendations.	N/A	N/A
E-GND 1..36	GND	P	Ground pads at center of package, all 36 must be connected to the ground plane with sufficient vias, follow design note recommendations.	N/A	N/A
A2,A3	AVDD18	P	Power supply input; Wi-Fi 1.8V digital, RF, baseband, and synthesizer supplies.	N/A	N/A
A4	VDDIO	P	Power supply input; Wi-Fi digital IO supply for GPIOs and XTAL oscillator.	N/A	N/A
A5,B5	SW_REG_OUT	P	Power supply; PMU switching regulator output, see design guide for details.	N/A	N/A
A6,B6	VDD33	P	Power supply input; Wi-Fi antenna and Wi-Fi PA 3.3V supplies.	N/A	N/A
A7,B7	VBAT_42	P	Power supply input; PMU VBAT supply input, see design guide for details.	N/A	N/A
A8,B8	PAREG_33_OUT	P	Power supply; PMU pass transistor collector, see design guide for details.	N/A	N/A
A9	PAREG_BASE	P	Power supply; PMU pass transistor base, see design guide for details.	N/A	N/A
A10	DVDD12	P	Power supply bypass; Wi-Fi digital 1.2V supply from internal LDO, connect to external bypass capacitor.	N/A	N/A
B1	AVDD12	P	Power supply bypass; Wi-Fi analog 1.2V supply from internal LDO, connect to external bypass capacitor.	N/A	N/A
B11	SREG_OUT	P	Power supply bypass; internal SDIO regulator output, option to connect to external bypass capacitor, see design guide.	N/A	N/A
C1	HOST_POWER	P	Power supply input; 1.8V or 3.3V Host IO (SDIO) power supply input.	N/A	N/A

Table 4-2. AR6103 Pin Definitions

Pin No.	Pin Name	Type	Description	Reset State	I/O Pad Supply Domain
			Digital Control		
B9	PM_MODE	I, PD	PMU mode, see design guide for details	Low	VDDIO
B10	PM_ENABLE	I, PD	PMU enable, see design guide for details.	Low	VDDIO
T7	HMODE0	I	Wi-Fi host mode select, see design guide for configuration details, floating input must be tied high or low.	X	VDDIO
R7	HMODE1	I	Wi-Fi host mode select, see design guide for configuration details, floating input must be tied high or low.	X	VDDIO
T11	CHIP_PWD_L	I, PD	WLAN Power Down (0=power down, 1=WLAN awake).	Low	HOST_POWER
T10	CHIP_WARM_RESET	I, PD	Wake-on-Wireless (Active High), UART-Over-SDIO: External BT reset.	Low	VDDIO
			Clocks and Timing		
A16	XTALI	A_I/O	Crystal oscillator input and must be NC.	N/A	VDDIO
A17	XTALO	A_I/O	Crystal oscillator output and must be NC.	N/A	VDDIO
B2	CLK_REQ_OUT	O	Output - asserted when reference clock is enabled.	Low	VDDIO
G16	LF_CLKIN	I	Input – optional Wi-Fi 32KHz low frequency sleep clock, must be tied to ground if not used, see design guide for details.	X	VDDIO
			Host Interface (SDIO Mode)		
D1	SD_CMD	I/O	SDIO Command	PU	HOST_POWER
J1	SD_CLK	I	SDIO Clock, must be driven.	X	HOST_POWER
H1	SD_D0	I/O	SDIO Data 0	PU	HOST_POWER
G1	SD_D1	I/O	SDIO Data 1	PU	HOST_POWER
F1	SD_D2	I/O	SDIO Data 2	PU	HOST_POWER
E1	SD_D3	I/O	SDIO Data 3	PU	HOST_POWER
			RF Port		
T4	WiFi_RF	A_I/O	RF Antenna Port	N/A	N/A

Table 4-2. AR6103 Pin Definitions

Pin No.	Pin Name	Type	Description	Reset State	I/O Pad Supply Domain
			Bluetooth Coexistence Interface		
B4	BT_FREQ	I	BT coexistence, grounded for 3-wire Packet Traffic Arbitration (PTA) protocol; must be driven by external device or tied to 0.	X	VDDIO
B16	BT_REG_FRAME	I	BT coexistence, must be driven by external device or tied to 0.	X	VDDIO
B17	BT_ACTIVE	I	BT coexistence, 3-wire PTA; must be driven by external device or tied to 0.	X	VDDIO
C17	BT_PRIORITY	I	BT coexistence, 3-wire PTA; must be driven by external device or tied to ground.	X	VDDIO
D17	WLAN_ACTIVE	O	Coexistence, 3-wire PTA	Low	VDDIO
M2	UART_TXD	I/O, PU	GPIO pin intended for Wi-Fi HCI UART TXD output used with SDIO-HCI interface.	N/A	VDDIO
N2	UART_RTS	I/O, PU	GPIO pin, intended for Wi-Fi HCI UART RTS output used with SDIO-HCI interface	N/A	VDDIO
P2	UART_RXD	I	GPIO pin intended for Wi-Fi HCI UART RXD input used with SDIO-HCI interface; must be driven by external device or tied to ground.	X	VDDIO
R2	UART_CTS	I	GPIO pin intended for Wi-Fi HCI UART CTS output used with SDIO-HCI interface; must be driven by external device or tied to ground.	X	VDDIO
			Radio Control		
L1	ANTC	O	Antenna switch control C.	Low	VDD33
T1	ANTD	O	Antenna switch control D.	Low	VDD33
T2	ANTE	O	Antenna switch control E.	Low	VDD33
			System Test		
T6	TDO (DEBUG_UART_TXD)	O	Wi-Fi JTAG TDO used with debugging Wi-Fi; reconfigured after software download as debugging UART TXD.	High	VDDIO
T8	TMS	I, PU	Wi-Fi JTAG TMS used with debugging only; for UART-over-SDIO mode, reconfigured after software download as Wake-On-Wireless (WOW), active low.	High	VDDIO

Table 4-2. AR6103 Pin Definitions

Pin No.	Pin Name	Type	Description	Reset State	I/O Pad Supply Domain
T9	TCK	I, PU	Wi-Fi JTAG TCK used with debugging only	High	VDDIO
R9	TDI	I, PU	Wi-Fi JTAG TDI used with debugging only.	High	VDDIO

5. Package Dimensions

Figure 5-1 and Figure 5-2 show the AR6103 package dimensions.

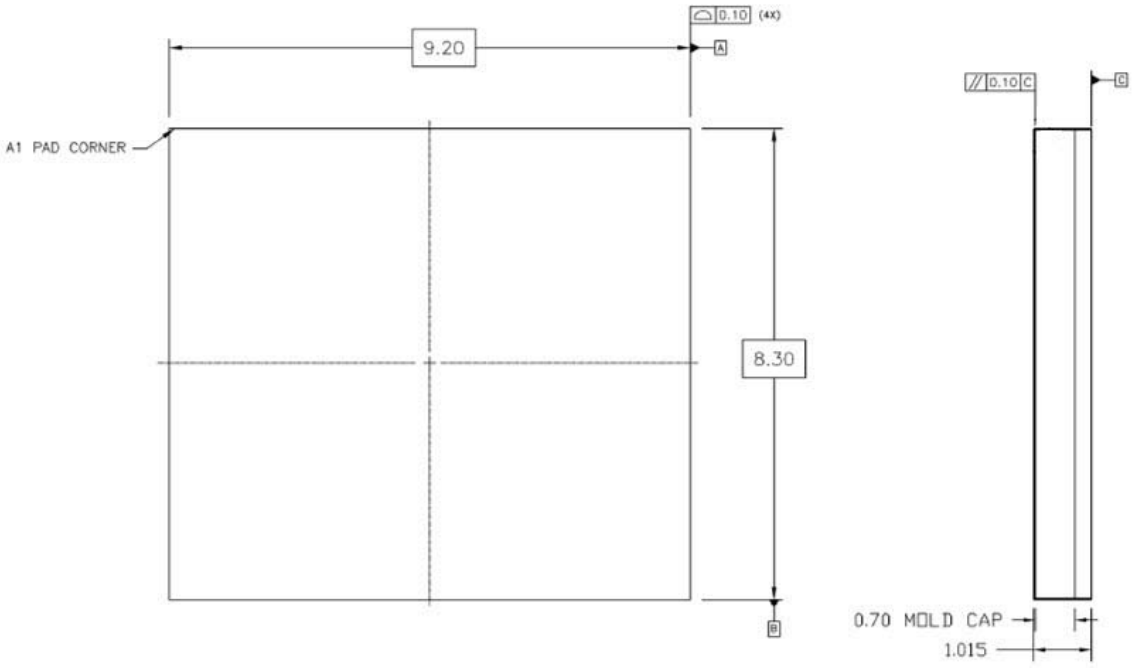


Figure 5-1. AR6103 Package Dimensions Top and Side Views

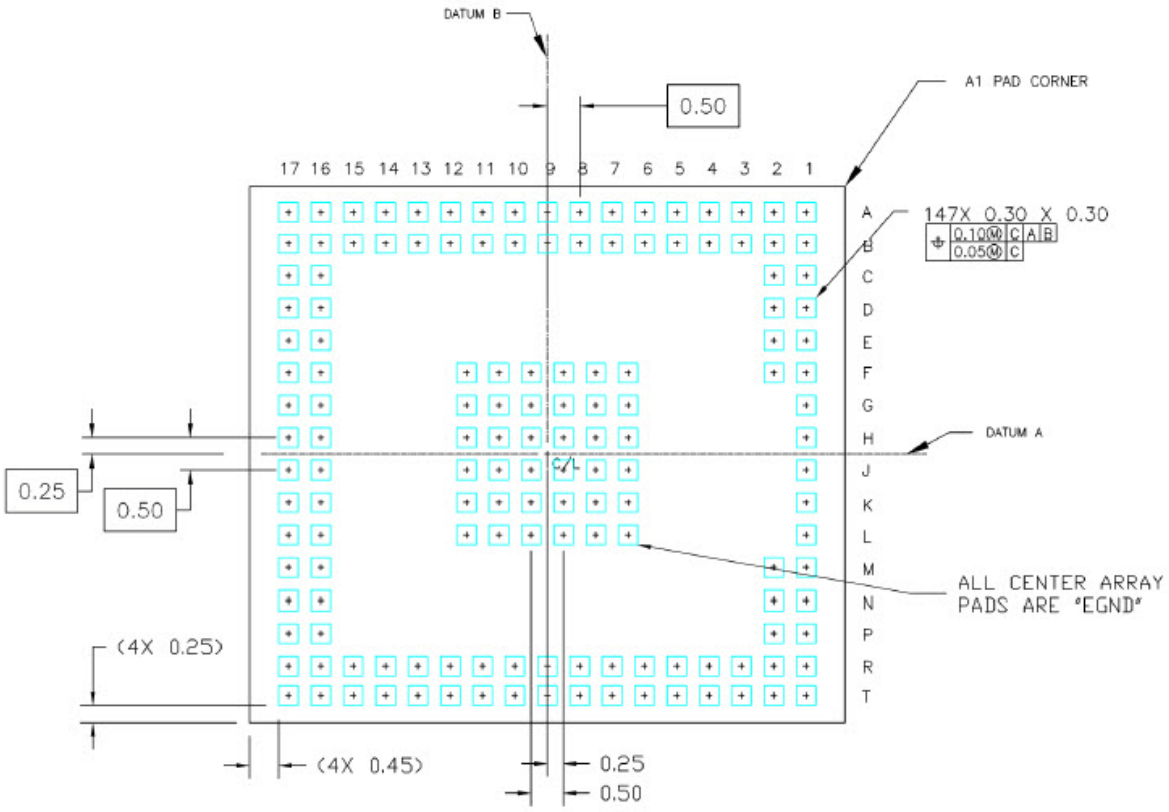


Figure 5-2. AR6103 Pin Assignments

6. Assembly Guidelines

This section describes the assembly guidelines and solder material information.

6.1 Solder Material Information

Manufacturer name: Kester

Solder past part number: EM808-Sn96.5% Ag3.0% Cu0.5% SAC305 alloy with Type 3 powder, water soluble solder paste

7. Design Guidelines

This section provides design information including application schematic, configuration options, design requirements, and recommendations for applying the AR6103 in Wi-Fi applications.

7.1 Application Schematic

Figure 7-1 below illustrates the implementation of the AR6103 in a Wi-Fi only application featuring antenna diversity. Figure 7-2 shows the AR6103 Application Schematic with on-chip PMU.

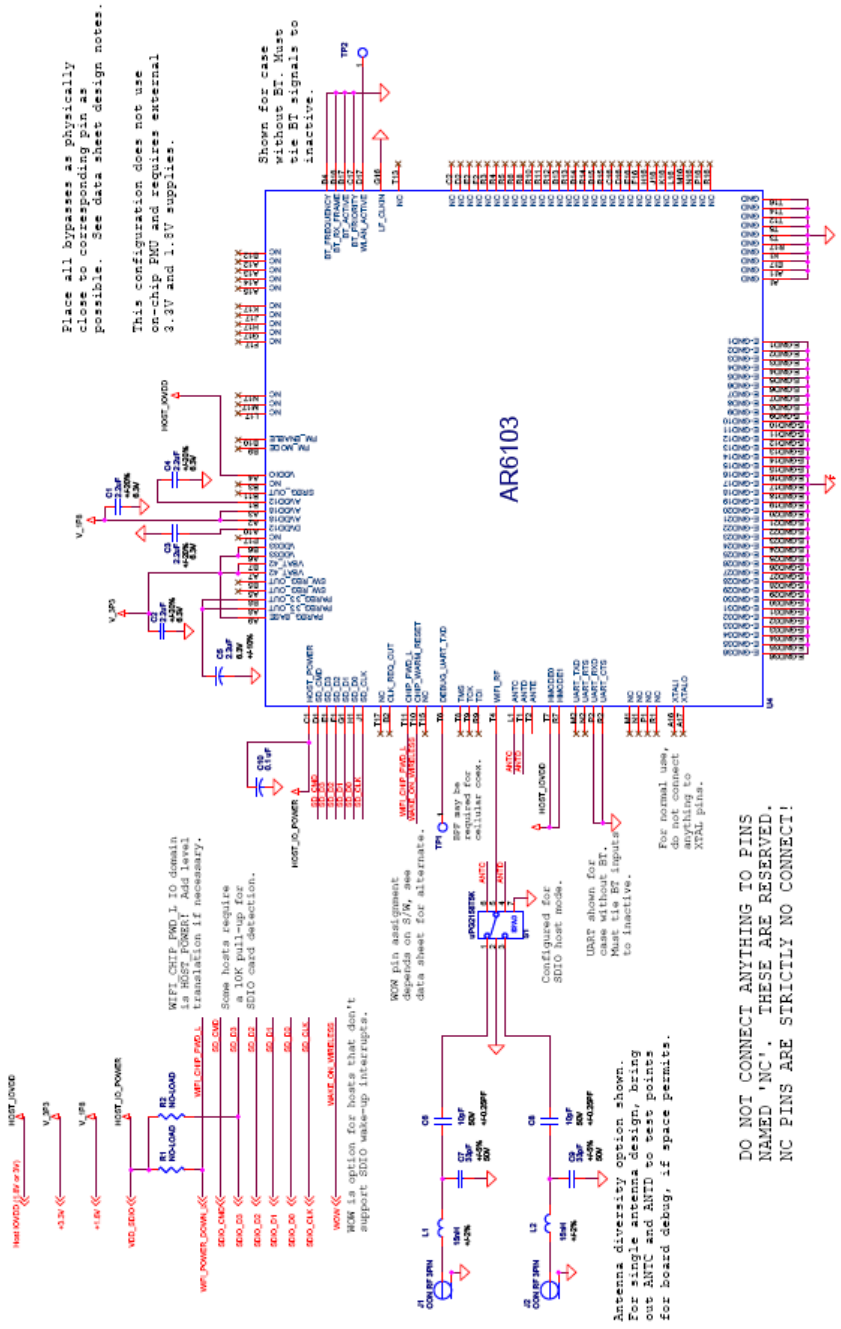


Figure 7-1. **AR6103 Reference Schematic**

7.2 Bluetooth Coexistence

Bluetooth coexistence protocol and options for shared WLAN-Bluetooth single antenna are fully supported in the AR6103.

The AR6103 supports 3 and 4-wire Packet Traffic Arbitration (PTA) protocol through signals BT_ACTIVE, BT_PRIORITY, WLAN_ACTIVE, and BT_FREQ. In 3-wire protocol, BT_FREQ must be grounded. Note that in configurations without Bluetooth, the coexistence protocol input pins (BT_FREQ, BT_RX_FRAME, BT_ACTIVE, and BT_PRIORITY) must be tied to ground as shown in the Application Schematic, Figure 7-1.

Though the AR6103 internally manages WLAN transmit and receive switching, there are three available antenna control pins ANTC to ANTE which can be configured arbitrarily. These ANTC to ANTE pins are capable of sourcing significant current, but should remain fast, with no large decoupling capacitors used. ANTE is a reserved control signal intended for WLAN-Bluetooth single antenna applications that use an antenna switch with ANTE selecting BT traffic. ANTE can also be driven high in low power states (SLEEP, HOST_OFF, and CHIP_PWD) in order to provide the antenna to the Bluetooth device while WLAN is not in use. WLAN traffic could be selected by either ANTC or ANTD. Antenna control pin assignment and use is described in the support bulletin titled AR6003 OTP and EEPROM File Structure; specifically in the section titled Antenna Configuration Supplement which allows configuration of ANTA. ANTD for all WLAN operating modes.

7.3 Antenna Diversity Option

Figure 7-1 shows the AR6103 Application Schematic featuring antenna diversity implemented with two antennas. Antenna selection outputs ANTC and ANTD steer the SPDT RF switch S1 to select the antenna in use for WLAN traffic.

Designs not implementing antenna diversity do not require the RF switch and use only a single antenna. Connect the antenna and appropriate matching network directly to WiFi_RF. Note that WiFi_RF has an internal DC blocking capacitor so an external one is not necessary.

7.4 Power Supply and the PMU

The AR6103 features an on-chip PMU supporting direct battery connection up to 4.2V, by generating 3.3V with an external pass transistor regulator and 1.8V from an internal switching regulator. Use of the PMU regulators is optional allowing for externally sourced 1.8V and 3.3V supplies. For pre-production samples of the AR6103, Atheros recommends designs interested in using the PMU should include external 1.8V and 3.3V LDOs with stuff options allowing PMU use with the production version of the AR6103.

7.4.1 On-chip PMU Configuration

The figure below shows the AR6103 configuration using the on-chip PMU. PMU configuration is implemented with:

- P-channel MOSFET transistor Q1, operated as linear regulator with 3.3V output.
- On-chip switching regulator using inductor L3, supplying 1.8V output.
- 10uFd bypass capacitor recommended for 3.3V regulated supply.

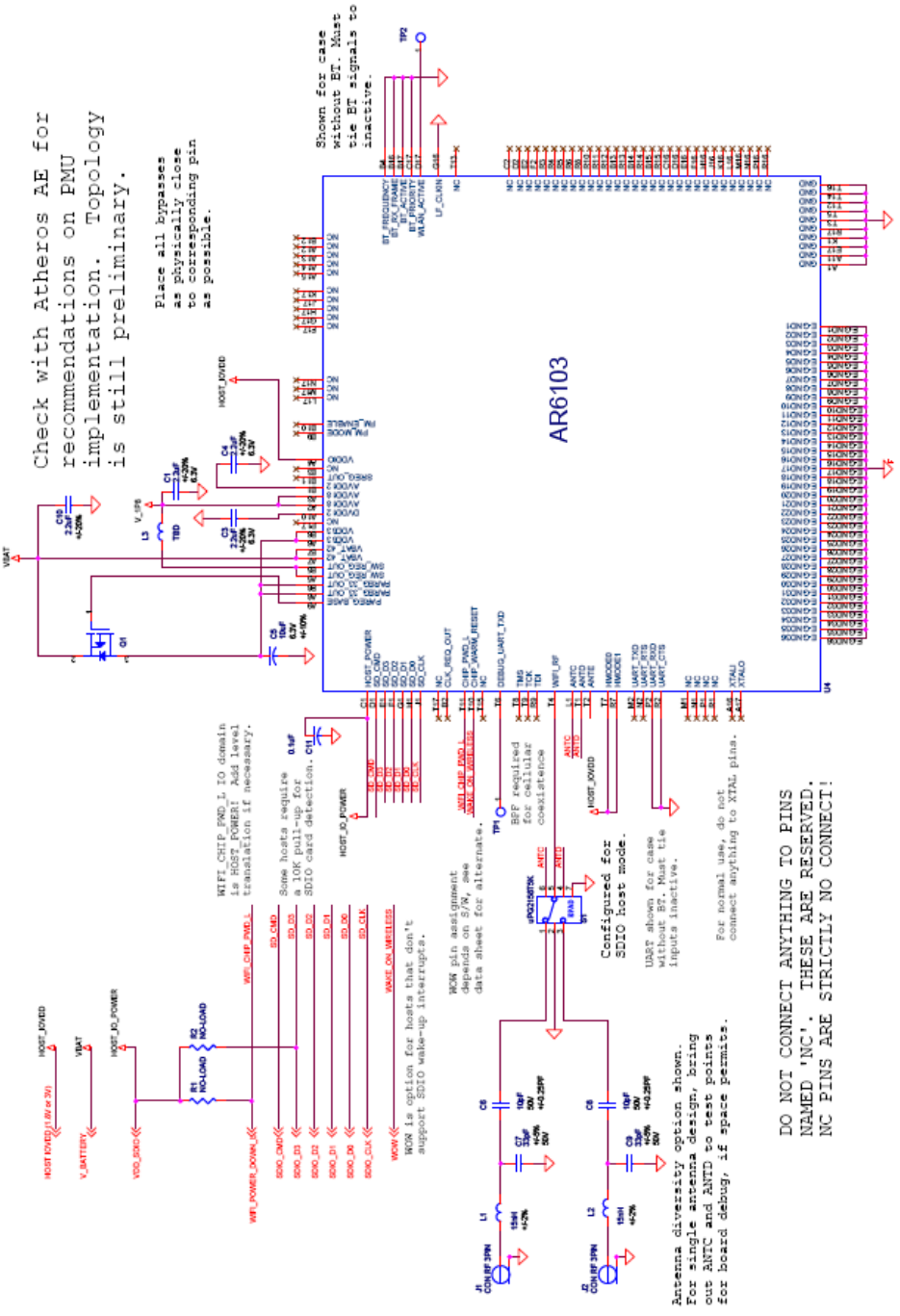


Figure 7-2. **AR6103 Application Schematic with On-Chip PMU**

7.4.2 External Supply Configuration

The Application Schematic in Figure 7-1 earlier showed the AR6103 applied in an external supply configuration. PMU related power pins are handled as follows:

- PAREG_BASE – must be connected to external 3V supply.
- VBAT_42 – must be connected to external 3V supply.
- PAREG_33_OUT – bypassed with capacitor, needed for OTP programming.
- SW_REG_OUT – no connect

NOTE: Do not connect to PM_MODE or PM_ENABLE. These modes are not recommended.

7.4.3 Designing for External Supplies with PMU Option

Boards can be designed for external 1.8V and 3.3V supply sources that include load/no-load options which enable PMU mode. These design options are detailed below in Table 7-1.

Table 7-1. **PMU Configuration Options**

Configuration	Load	No-Load	Comment
External 1.8V, 3.3V	1.8V and 3.3V LDOs or source jumpers	Inductor L3 at SW_REG_OUT, transistor Q1.	Refer to Application Schematic Figure 7-2 with PMU for L3 and Q1 identification.
	0-ohm jumper from 3.3V to PAREG_BASE	-	PAREG_BASE must be pulled up to 3.3V when not using on-chip PMU.
	C5 is 2.2uFd	-	Smaller capacitance needed only for OTP programming.
On-chip PMU	Inductor L3 at SW_REG_OUT, transistor Q1	1.8V and 3.3V LDOs or source jumpers.	Refer to Application Schematic with PMU for L3 and Q1 identification.
	-	0-ohm jumper from 3.3V to PAREG_BASE.	Base will be controlled by PAREG_BASE output.
	C5 is 10uFd	-	Larger capacitance is recommended.

7.5 Power Supply Bypassing

The recommended minimum bypass capacitance for each power pin and PMU configuration is shown in Figure 7-2.

Table 7-2. **Power Supply Bypass Recommendations**

PMU Configuration	Supply	Pins	Minimum Capacitance
External 1.8V, 3.3V	3.3V	VBAT_42, VDD33, and PAREG_BASE	2.2uFd
	N/A	PAREG_33_OUT	2.2uFd
Using on-chip PMU	Battery	VBAT_42	2.2uFd
	3.3V	PAREG_33_OUT	10uFd
All	1.8V	AVDD18	2.2uFd
All	Host I/O	HOST_IO_POWER	0.1uFd
All	1.2V	DVDD12	2.2uFd
	1.2V	AVDD12	2.2uFd

7.6 Sleep Clock Option

The AR6103 features an internal low frequency sleep clock and therefore, does not require an external sleep clock source. Designs which use the internal sleep clock must ground the LF_CLKIN pin. The ideal frequency of the sleep clock is 32768 Hz. Because the on-chip oscillator frequency tolerance is not precise, the use of an accurate external sleep clock should reduce system power consumption slightly due to greater precision in sleep duration timing.

7.7 Testability Recommendations

Atheros recommends that designs support two categories of testability associated with board bring-up debugging and NOT associated with manufacturing test:

- Test point pad for DEBUG_UART_TXD (strongly recommended)
- Test point pads for OUTC and OUTD (recommended if space allows)

The Application Schematic, Figure 7-1 shown earlier, displays test point TP1 serving to fulfill the first testability recommendation. Use of this pad consists of tacking a wire to TP1 and running it to an RS-232 level translator for UART COM port monitoring of software debug messages. This provides the visibility which may be essential when debugging unusual board issues.

If PCB layout space allows, access to OUTC and OUTD is desirable for differential RF probing the baseband radio. Such a one-time measurement is unusual, but may potentially be needed if investigating unusual performance issues.

The pin list does identify JTAG pins for the WLAN. These are not recommended for customer designs and should be left as NO CONNECT as indicated in the Application Schematic.

7.8 Power Up/Power Down Sequence

The following two figures show the recommended power up/down and reset sequences for the AR6103 using its internal PMU. They are applicable, in principle, to designs using external supplies too. The VBAT waveform in Figure 7-3 represents battery insertion and removal from the system and not any AR6103 requirements. Figure 7-4 shows the reset and power cycle timing.

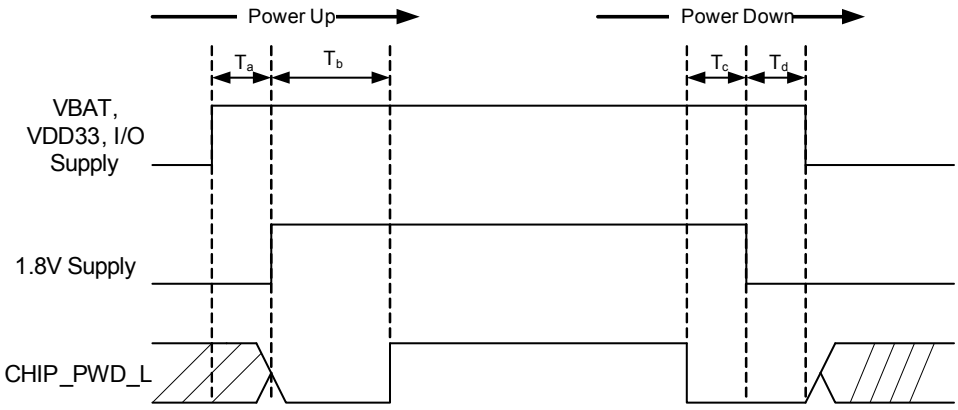
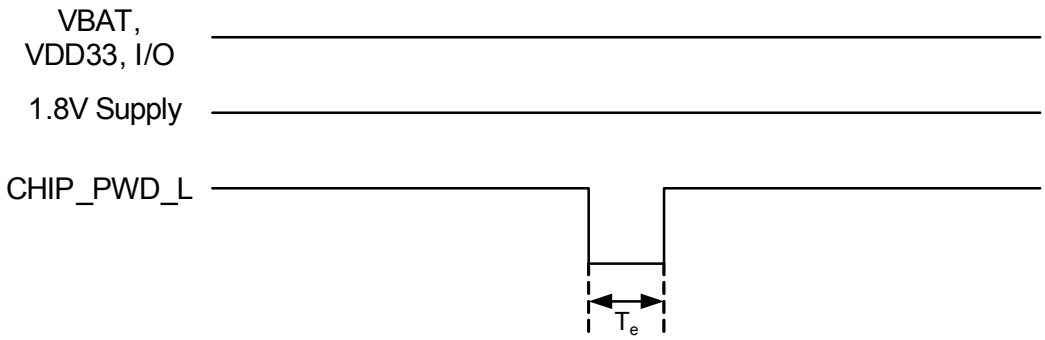


Figure 7-3. **Power Up/Power Down Timing**



VBAT = VBATTERY_42
VDD33 = VDD33_ANT, VDD33_PA, PAREG_BASE
I/O = DVDD_SDIO, DVDD_SOC1, DVDD_SOC2, VDD18_XTAL
1.8V Supply = VREG, AVDD18

Figure 7-4. **Reset and Power Cycle Timing**

Table 7-3 shows the power supply requirements.

Table 7-3. **Power Supply Requirements**

Symbol	Description	Min. (microsec)
T_a	Time between VBAT, VDD33, and I/O supplies valid and 1.8V supply valid.[1]	0
T_b	Time between 1.8V supply valid and CHIP_PWD_L deassertion.	5
T_c	Time between CHIP_PWD_L assertion and 1.8V supply invalid.	0
T_d	Time between 1.8V supply invalid and VBAT, VDD33, and I/O supplies invalid.	N/A[2]
T_e	Length of CHIP_PWD_L pulse.	5

[1] Supply valid represents the voltage level has reached 90% level.
[2] No strict requirement. This parameter can also be negative.

7.9 Host Interface Configuration

The AR6103 host interface is selected through two pins named HMODE0 and HMODE1. These two pins are to be tied low (ground) or high (VDDIO) as determined in Table 7-4. Note that these pins can be tied off directly without any series resistances. Table 7-4 shows the Host Mode Configuration.

Table 7-4. **Host Mode Configuration**

Pin	SDIO	GSPI
HMODE0	HIGH	LOW
HMODE1	HIGH	HIGH

Table 7-5 identifies the pins used for GSPI host interface mode. The pin names associated with the SDIO host interface are redefined as shown in this table as GSPI pin names. Included for technical reference, are the internal GPIO signals which the firmware will reconfigure for GSPI host mode.

Table 7-5. **GSPI Host Mode Pin Definition**

AR6103 Pin Name	Reference GPIO signal	GSPI Pin Name
SD_CMD	9	SPI_MOSI
SD_CLK	14	SPI_CLK
SD_D0	13	SPI_MISO
SD_D1	12	SPI_INT
SD_D2	11	Not used
SD_D3	10	SPI_CS

7.10 Cellular Coexistence

Designs working in close proximity with a cellular radio may require a band-pass filter in-line with the WiFi_RF analog I/O to insure sufficient cellular coexistence. This band-pass filter should provide sufficient rejection of the cellular bands, namely at the 2.17 GHz, 1.99 GHz, 1.91 GHz, 1.79 GHz, and 824 MHz frequencies. The amount of rejection will be application dependent, but plan on requiring at least 40dB rejection. Table 7-6 shows some recommended coexistence band-pass filters.

Table 7-6. **Recommended Co-existence Bandpass Filters**

	Filter Attenuation (dB)					
Cellular Frequencies	**SAFEA2G45RA0F00**	**TDK DEA202450BT-3201B2**	**TDK DEA162450BT-2092AT1-H**	**Soshin HMD847H**	**Soshin HMD844H**	**Soshin HMD848H**
2.17 GHz	41	26	30	20	12	35
1.99 GHz	38	40	40	40	20	40
1.91 GHz	38	40	40	40	20	40
1.79 GHz	38	40	40	40	28	40
824 MHz	53	40	40	40	30	40
Insertion Loss (dB)	2.2	2.5	3.0	2.5	1.5	3.2
Size (L x W x H mm)	1.35 x 1.05 x 0.5	2.0 x 1.25 x 0.8	1.60 x 0.8 x 0.6	2.0 x 1.25 x 1.0	2.0 x 1.25 x 0.8	2.0 x 1.25 x 0.8

When using a band-pass filter, include the appropriate matching circuits to ensure optimum performance. An example using the SAFEA2G45AC0F00 is shown in Figure 7-5 that shows shunt inductors in series tuned upon board bring-up. For SAW filters, the preference for this SAW is for IN to be feeding the Wi-Fi antenna.

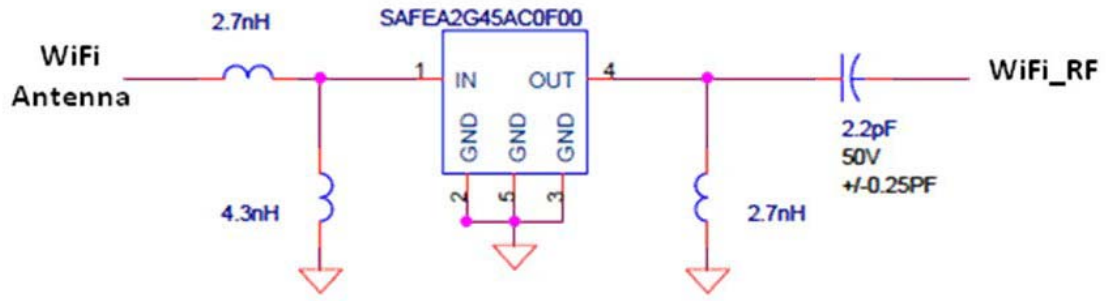


Figure 7-5. **Cellular Coexistence Band-pass Filter Example**

7.11 PCB Layout Requirements

Even though the AR6103 integrates most RF path functionality, care must be taken with the WiFi_RF antenna feed, host interface routing, and power supply bypassing.

7.11.1 RF Layout

An example of the component and via placement is shown in Figure 7-6.

Because the AR6103 integrates most of the RF path, the WiFi_RF port trace routing need to follow the standard RF practices as summarized below:

- The layout should keep solid ground planes under all RF paths, and signal return paths should be uninterrupted.
- To make the most efficient use of board space and maintain tight impedance control, it is recommended to place components as close together as possible (15-20 mils pad-to-pad spacing). In addition, all ground vias need to be placed close to the ground pad itself in order to avoid introducing excessive inductance between the component and ground return path.

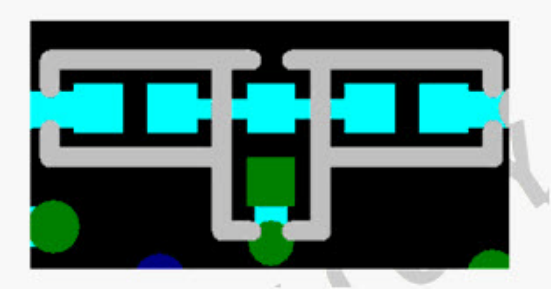


Figure 7-6. **Component and Via Placement Example**

- To aid in maintaining a tight placement and to avoid any deviation from the reference design, it is strongly recommended to use 0201 sized components. In addition, all component values are based on the parasitic characteristics of 0201 components. Using the recommended component size will significantly reduce the potential for performance degradation and the need to re-tune component values.
- It is recommended that RF traces be routed on the top layer with 2nd layer as the ground reference. Use the "Microstrip transmission line" model for all RF paths. The goal is to maintain 50-ohm impedance by using a 9 mil trace width with 5 mil air gap between Layer 1 and Layer 2 and selecting standard FR4 dielectric material.
- All matching components must be placed as close as possible (within 40 mils) to the chip pins.
- Place ground vias as close to component pads as possible in order to avoid introducing additional inductance to the circuit. Implement ground per via pad. Do not share vias.

7.11.2 SDIO Interface

SDIO pads on the outer ring can be routed on layer 1. For the inner ring, drill a micro via from layer 1-2, then route to nearest area where a thru-hole via can be drilled. Then route all the SDIO traces together on the same layer. Make sure SDIO lines are not crossing (parallel and guarded with ground vias). For optimal routing, we recommend routing these traces before any of the other signals.

7.11.3 Power Supply Bypass Capacitance Placement

The following guidelines describe recommended power supply bypass capacitor placement with component references made to the Application Schematic in Figure 7-1 earlier. The AR6103 includes on-chip, many smaller bypass capacitors associated with RF and high frequency bypassing. Only the larger capacitances shown below have placement constraints:

- AVDD18 – Bypass capacitor C1 is a critical component and should be placed within 20 mils of ball pins A2 and A3.

- VDD33 – Bypass capacitor C2 (or C5 in PMU case) is a critical component and should be placed within 20 mils of pins A6 and B6.
- DVDD12 – Place bypass capacitor C3 near pin A10. This supply is less sensitive to noise, so there is more flexibility in its routing.
- AVDD12 – Bypass capacitor C4 is a critical component and should be placed within 20 mils of pin B1.

8. Ordering Information

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