ATHEROS COMMUNICATIONS

June 2009

AR6102 ROCm™ MAC/BB/Radio for 2.4 GHz Embedded WLAN Applications

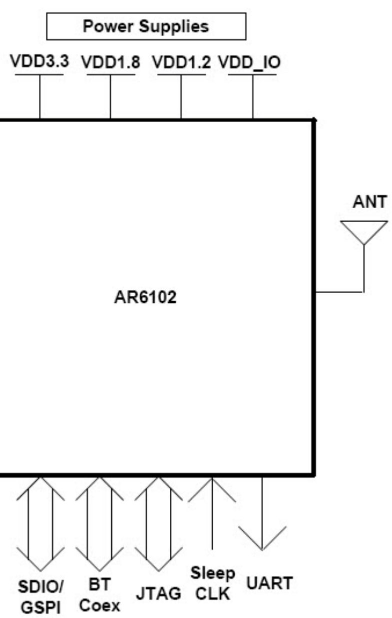
General Description

The Atheros AR6102 is a member of the WLAN ROCm family of chips. The compact size and low power consumption of this design make it an ideal vehicle for adding WLAN to hand-held and other battery-powered consumer electronic devices. The IEEE 802.11g (2.4 GHz) standard is supported by this chipset.

The AR6102 family includes a highly integrated, RF front-end (Power Amplifier, Low-Noise Amplifier and RF switch) and high-frequency reference clock, enabling low-cost designs with minimal external components. Advanced architecture and protocol techniques save power during sleep, stand-by and active states.

The AR6102 family supports 2, 3 and 4 wire Bluetooth coexistence protocols with advanced algorithms for predicting channel usage by the co-located Bluetooth transceiver. A 26MHz reference clock output is also available, eliminating the need for a dedicated BT clock.

The AR6102 provides multiple peripheral interfaces including UART.



Atheros AR6102 Block Diagram

AR6102 Features

- IEEE 802.11b/g compliant
- Data rates of 1–54 Mbps for 802.11g
- Advanced power management to minimize standby, sleep and active power
- Security support for WPS, WPA2, WPA, WAPI and protected management frames
- Support for 2.4 GHz operation in all available bands in all regulatory domains
- Full 802.11e QoS support including WMM and U-APSD
- Support for fast Tx and Rx antenna diversity allowing optimal antenna selection on a per-packet basis
- Supports both SDIO 1.1 and GSPI host interfaces.
- Standard 2, 3 and 4 wire Bluetooth coexistence handshake support
- 16550-compliant UART
- Wake-on-Wireless (WoW) maximizes host sleep duration
- 7.4 x 8 mm LGA package
- Pre-certified to meet FCC, ETSI, and TELEC standards
- Integrated PA, LNA, RF switch and High Freq Reference Clock, minimizing external component count
- Integrated RF shielding
- Suports cellular co-existence with an external band-pass filter

Table of Contents

1. Dimensions and Footprint

This section provides the dimensions and footprint of the AR6102. Figure 1-1 shows the top and side view of the AR6102.

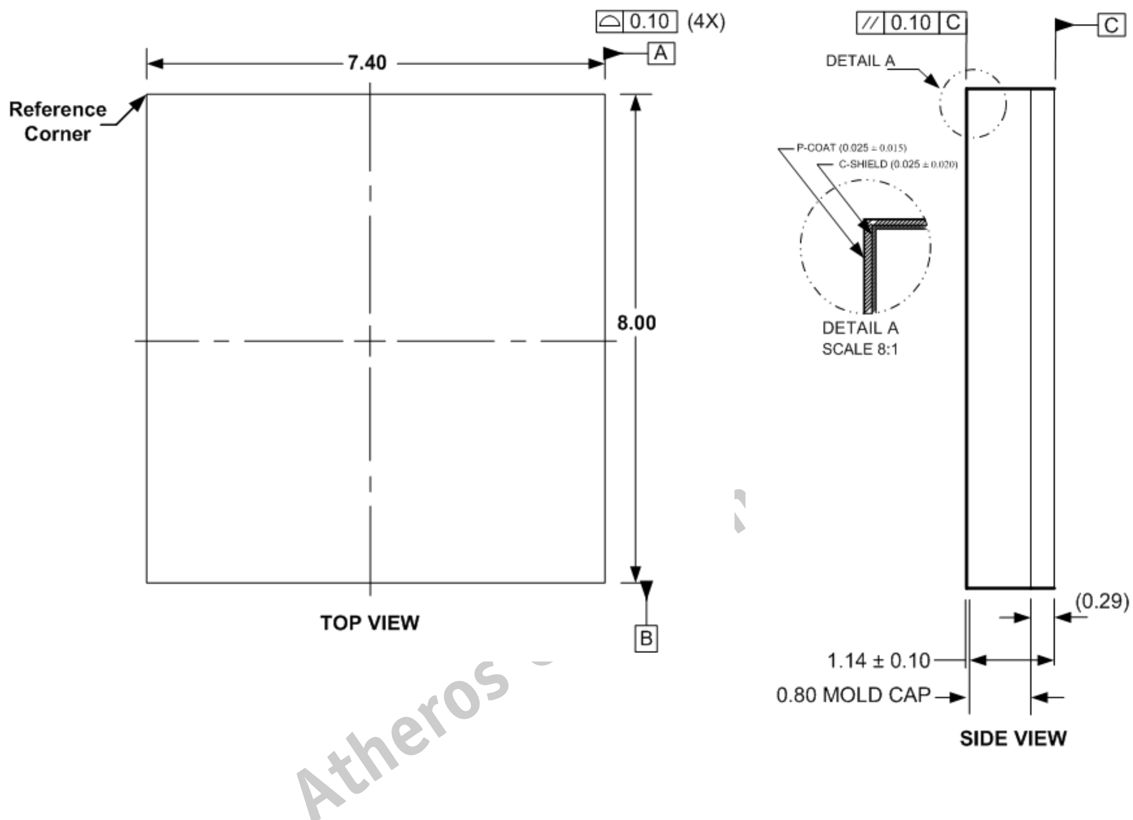


Figure 1-1. **Dimensions and Footprint - Top and Side View**

Figure 1-2 shows the bottom view of the AR6102.

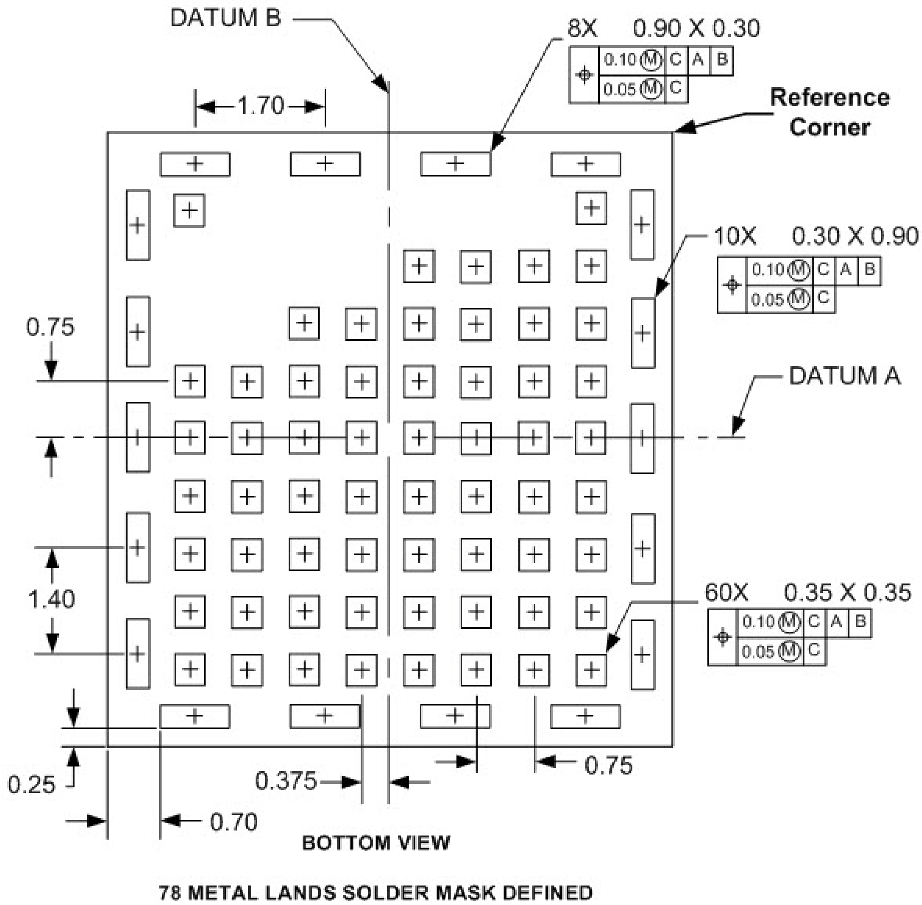


Figure 1-2. **Dimensions and Footprint - Bottom View**

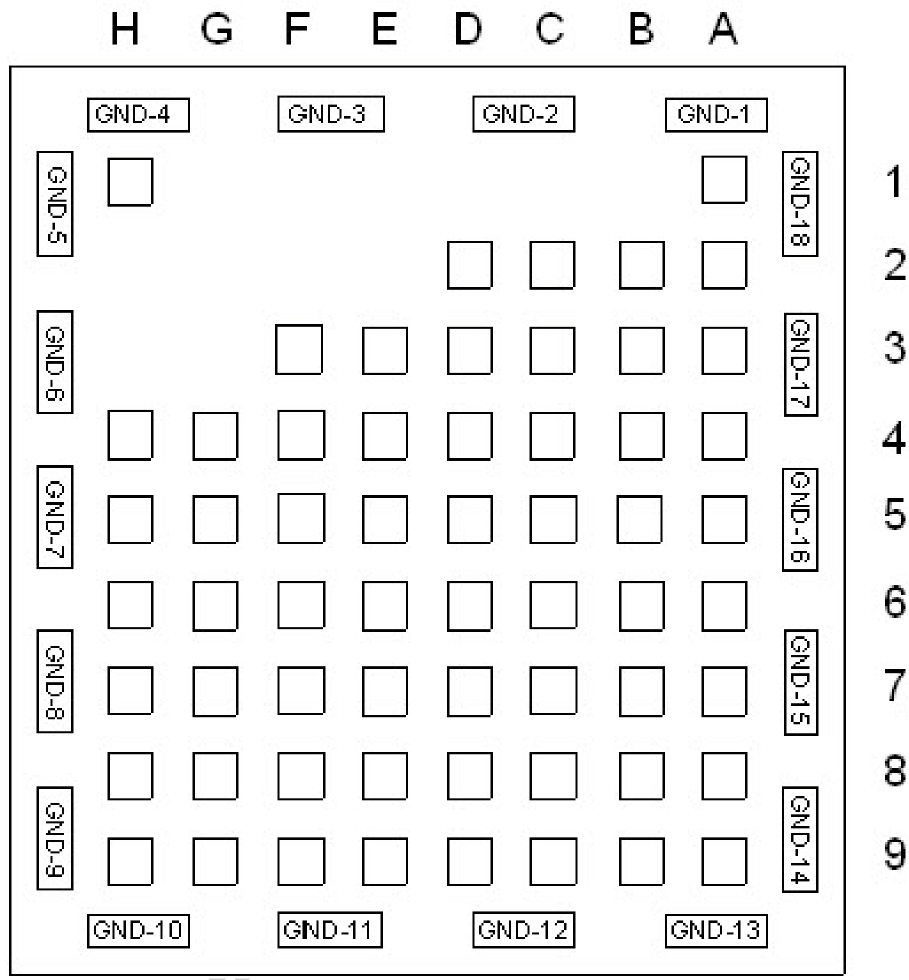


Figure 1-3. **Dimensions and Footprint - Bottom View Details**

2. Pin Assignment and Description

This section provides pin assignments descriptions.

The following nomenclature is used for signal types described in this chapter.

The following nomenclature is used for signal names:

NC	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
A_I/O	Analog input signal
I	Digital input signal
PU	Weak internal pull-up, to prevent signals from floating when left open
PD	Weak internal pull-down, to prevent signals from floating when left open
I/O	A digital bidirectional signal
O	A digital output signal
P	A power or ground signal

See Table 2-1 for the AR6102 package pin assignments.

Table 2-1. **Pin Assignment**

Pin No.	Name	Pin No.	Name
A1	GND	F7	VDD_BT
A2	VCC_FEM	F8	WLAN_ACTIVE
A3	BT_CLK_OUT	F9	VDD18
A4	VDD_12	G4	VDD_GPIO
A5	JTAG_SEL	G5	XTALO
A6	CLK_REQ	G6	ANTD
A7	SYS_RST_L	G7	ANTE
A8	SD_D0	G8	GND
A9	SD_CLK	G9	VDD18
B2	VCC_FEM	H1	RF_OUT
B3	BT_CLK_EN	H4	GND
B4	RSVD_BBPI	H5	ANTA
B5	TXD0	H6	BT_FREQ
B6	CHIP_PWD_L	H7	BT_ACTIVE
B7	SD_D1	H8	GND
B8	SD_D2	H9	GND
B9	TDI	GND-1	GND
C2	GND	GND-2	GND
C3	VDD_1.2VA	GND-3	GND
C4	GND	GND-4	GND
C5	GND	GND-5	GND
C6	WAKE_ON_WLAN	GND-6	GND
C7	SD_D3	GND-7	GND
C8	TDO	GND-8	GND
C9	TMS	GND-9	GND
D2	GND	GND-10	GND
D3	GND	GND-11	GND
D4	GND	GND-12	GND
D5	GND	GND-13	GND
D6	GND	GND-14	GND
D7	SD_CMD	GND-15	GND
D8	TCK	GND-16	GND
D9	CLK32K	GND-17	GND
E3	GND	GND-18	GND
E4	GND		
E5	GND		
E6	GND		
E7	DVDD_SDIO		
E8	HMODE_1		
E9	BT_PRIORITY		
F3	GND		
F4	GND		
F5	GND		
F6	VCC_FEM		

2.1 Pin Description

Table 2-2 describes the pins.

Table 2-2. **Pin Description**

Pin No.	Name	Type	Description	Reset State	Pad Power Supply Domain
			Power Supply		
B2 A2 F6	VCC_FEM	P	Supply for front-end components and switch control lines.	N/A	N/A
C3	VDD_1.2VA	P	Analog 1.2V supply	N/A	N/A
A4	VDD_12	P	Digital 1.2V supply	N/A	N/A
F7	VDD_BT	P	BT-coexistence I/O Supply	N/A	N/A
G4	VDD_GPIO	P	GPIO supply voltage	N/A	N/A
E7	DVDD_SDIO	P	Host interface supply voltage	N/A	N/A
F9	VDD18	P	Analog 1.8V supply	N/A	N/A
G9	VDD18	P	Analog 1.8V supply	N/A	N/A
A1	GND	P	Ground connections	N/A	N/A
C2	GND	P	Ground connections	N/A	N/A
C4	GND	P	Ground connections	N/A	N/A
C5	GND	P	Ground connections	N/A	N/A
D2	GND	P	Ground connections	N/A	N/A
D3	GND	P	Ground connections	N/A	N/A
D4	GND	P	Ground connections	N/A	N/A
D5	GND	P	Ground connections	N/A	N/A
D6	GND	P	Ground connections	N/A	N/A
E3	GND	P	Ground connections	N/A	N/A
E4	GND	P	Ground connections	N/A	N/A
E5	GND	P	Ground connections	N/A	N/A
E6	GND	P	Ground connections	N/A	N/A
F3	GND	P	Ground connections	N/A	N/A
F4	GND	P	Ground connections	N/A	N/A
F5	GND	P	Ground connections	N/A	N/A
G8	GND	P	Ground connections	N/A	N/A
H4	GND	P	Ground connections	N/A	N/A
H8	GND	P	Ground connections	N/A	N/A
H9	GND	P	Ground connections	N/A	N/A
GND-1	GND	P	Ground connections	N/A	N/A
GND-2	GND	P	Ground connections	N/A	N/A

Table 2-2. **Pin Description (continued)**

Pin No.	Name	Type	Description	Reset State	Pad Power Supply Domain
GND-2	GND	P	Ground connections	N/A	N/A
GND-3	GND	P	Ground connections	N/A	N/A
GND-4	GND	P	Ground connections	N/A	N/A
GND-5	GND	P	Ground connections	N/A	N/A
GND-6	GND	P	Ground connections	N/A	N/A
GND-7	GND	P	Ground connections	N/A	N/A
GND-8	GND	P	Ground connections	N/A	N/A
GND-9	GND	P	Ground connections	N/A	N/A
GND-10	GND	P	Ground connections	N/A	N/A
GND-11	GND	P	Ground connections	N/A	N/A
GND-12	GND	P	Ground connections	N/A	N/A
GND-13	GND	P	Ground connections	N/A	N/A
GND-14	GND	P	Ground connections	N/A	N/A
GND-15	GND	P	Ground connections	N/A	N/A
GND-16	GND	P	Ground connections	N/A	N/A
GND-17	GND	P	Ground connections	N/A	N/A
GND-18	GND	P	Ground connections	N/A	N/A
Host Interface					
A8	SD_D0	I/O	SDIO data signal	PU	DVDD_SDIO
B7	SD_D1	I/O	SDIO data signal	PU	DVDD_SDIO
B8	SD_D2	I/O	SDIO data signal	PU	DVDD_SDIO
C7	SD_D3	I/O	SDIO data signal	PU	DVDD_SDIO
D7	DS_CMD	I	SDIO command signal	PU	DVDD_SDIO
A9	SD_CLK	I	SDIO clock signal	-	DVDD_SDIO
RF Port					
H1	RF_OUT	A_I/O	RF I/O port	-	-
Bluetooth Coexistence Interface					
E9	BT_PRIORITY	I/0	Input to WLAN indicating BT Status. Leave as NC when unused.	-	VDD_BT
F8	WLAN_ACTIVE	I/0	Output to BT indicating WLAN Status. Leave as NC when unused.	PD	VDD_BT
H6	BT_FREQ	I/0	Input to WLAN indicating BT Status. Leave as NC when unused.	-	VDD_BT
H7	BT_ACTIVE	I/0	Input to WLAN indicating BT Status	-	VDD_BT

Table 2-2. **Pin Description (continued)**

Pin No.	Name	Type	Description	Reset State	Pad Power Supply Domain
Radio Control Signals					
H5	ANTA	O	Control signal for external RF front-end components. Leave as NC when unused.	PD	VCC_FEM
G6	ANTD	O		PU	
G7	ANTE	O		PD	
Clocking Interface					
D9	CLK32K	I	Input for external 32KHz sleep clock.	-	VDD_GPIO
G5	XTALO	I	Input for external reference clock oscillator. Leave as NC.	-	-
A3	BT_CLK_OUT	O	Buffered reference clock output. Leave as NC when unused.	-	-
Digital Control					
B6	CHIP_PWD_L	I	Chip power down input	PD	DVDD_SDIO
A7	SYS_RST_L	I	Chip reset input	PU	DVDD_SDIO
E8	HMODE_1	I	Host interface selection input	-	VDD_GPIO
A6	CLK_REQ	O	External oscillator enable signal. Leave as NC.	PD	DVDD_SDIO
B3	BT_CLK_EN	I	Input signal to enable buffered clock output. Tie to GND when unused.	-	VDD18
C6	WAKE_ON_WLAN	O	Output signal to interrupt host	PD	VDD_GPIO
System Test					
B4	RSVD_BBPI	NC	Reserved for internal use. Leave as NC.	-	-
B5	TXD0	NC		-	-
A5	JTAG_SEL	NC		-	VDD_GPIO
B9	TDI	NC			DVDD_SDIO
C8	TDO	NC			
D8	TCK	NC			
C9	TMS	NC			

3. Electrical Characteristics

This section describes electrical characteristics of the AR6102.

3.1 Absolute Maximum Ratings

See Table 3-1

Table 3-1. **Absolute Maximum Ratings**

Parameter	Min.	Max.	Unit
VDD_1.2VA	-0.3	1.35	V
VDD_12	-0.3	1.35	V
VDD_BT	-0.3	4.0	V
VDD_GPIO	-0.3	4.0	V
DVDD_SDIO	-0.3	4.0	V
VDD18	-0.3	2.5	V
VCC_FEM	-0.3	4.2	V

3.2 Recommended Operating Conditions

See Table 3-2.

Table 3-2. **Recommneded Operating Conditions**

Parameter	Min.	Typ.	Max.	Unit
VCC_FEM	3.0	3.3	3.6	V
VDD_1.2VA	1.14	1.2	1.26	V
VDD_12	1.14	1.2	1.26	V
VDD_BT	1.71	1.8	3.46	V
VDD_GPIO	1.71	1.8	3.46	V
DVDD_SDIO	1.71	1.8	3.46	V
VDD18	1.71	1.8	1.89	V
T_{case} Commercial	-20	25	85	°C
T_{case} Industrial[1]	-40	25	85	°C

[1]Contact Atheros Sales for Industrial grade parts

3.3 DC Electrical Characteristics

General DC Electrical Characteristics (For 3.3V I/O Operation)

Table 3-3. **General DC Electrical Characteristics (For 3.3 V I/O Operation)**

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage			0.8 x V_{dd}	-	V_{dd} + 0.3	V
V_{IL}	Low Level Input Voltage			–0.3	-	0.2 x V_{dd}	V
I_{IL}	Input Leakage Current	Without Pull-up or Pull-down	0 V < V_{in} < V_{dd} 0 V < V_{out} < V_{dd}	–10		10	µA
		With Pull-up or Pull-down	0 V < V_{in} < V_{dd} 0 V < V_{out} < V_{dd}	–65		65	µA
V_{OH}	High Level Output Voltage		I_{OH} = –4 mA	V_{dd} – 0.35	-	-	V
			I_{OH} = –12 mA[1]	V_{dd} – 0.35	-	-	V
V_{OL}	Low Level Output Voltage		I_{OL} = 4 mA	-	-	0.40	V
			I_{OL} = 12 mA[1]	-	-	0.40	V
C_{IN}	Input Capacitance[2]		-	-	6	-	pF

[1]For these pins only: SDIO_DATA_0, SDIO_DATA_1, SDIO_DATA_2, SDIO_DATA_3
[2]Parameter not tested; value determined by design simulation

Table 3-4. **General DC Electrical Characteristics (For 1.8 V I/O Operation)**

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage			0.8 x V_{dd}	-	V_{dd} + 0.2	V
V_{IL}	Low Level Input Voltage			–0.3	-	0.2 x V_{dd}	V
I_{IL}	Input Leakage Current	Without Pull-up or Pull-down	0 V < V_{in} < V_{dd} 0 V < V_{out} < V_{dd}	–10	-	10	µA
		With Pull-up or Pull-down	0 V < V_{in} < V_{dd} 0 V < V_{out} < V_{dd}	–35	-	35	µA
V_{OH}	High Level Output Voltage		I_{OH} = –2 mA	V_{dd} – 0.35	-	-	V
			I_{OH} = –6 mA[1]	V_{dd} – 0.35	-	-	V
V_{OL}	Low Level Output Voltage		I_{OL} = 2 mA	-	-	0.3	V
			I_{OL} = 6 mA[1]	-	-	0.3	V
C_{IN}	Input Capacitance[2]		-	-	6	-	pF

[1]For these pins only: SDIO_DATA_0, SDIO_DATA_1, SDIO_DATA_2, SDIO_DATA_3
[2]Parameter not tested; value determined by design simulation

3.4 Radio Receiver Characteristics

Table 3-5 summarize the AR6102 receiver characteristics.

Table 3-5. **Receiver Characteristics for 2.4 GHz Operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{rx}	Receive input frequency range	5 MHz channel spacing	2.412	-	2.484	GHz
S_{rf}	Sensitivity	-				dBm
	1 Mbps		-96	-98	-100	
	2 Mbps		-92	-93	-96	
	5.5 Mbps		-89	-92	-94	
	11 Mbps		-85	-88	-91	
	6 Mbps		-91	-93	-96	
	9 Mbps		-89	-92	-95	
	12 Mbps		-89	-91	-93	
	18 Mbps		-87	-88	-92	
	24 Mbps		-83	-85	-88	
	36 Mbps		-80	-82	-85	
	48 Mbps		-75	-77	-81	
	54 Mbps		-73	-75	-77	
IP1dB	Input 1 dB compression (min. gain)	-	-8	-2	-	dBm
IIP3	Input third intercept point (min. gain)	-	-2	+3	-	dBm
ER_{phase}	I,Q phase error		-4	0.5	4	degree
ERamp	I,Q amplitude error		-1	0	1	dB
R_{adj}	Adjacent channel rejection	10 to 20 MHz				dB
	1 Mbps		34	36	-	
	11 Mbps		31	34	-	
	6 Mbps		35	37	-	
	54 Mbps		22	24	-	
TRpowup	Time for power up (from RxOn)	-	-	1.5	-	µs

3.5 Radio Transmitter Characteristics

Table 3-6 a summarize the transmitter characteristics for AR6102.

Table 3-6. **Transmitter Characteristics for 2.4 GHz Operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range	5 MHz center frequency	2.412	-	2.484	GHz
P_{out} SP_{gain}	Mask Compliant CCK output power		-	15	-	dBm
	EVM Compliant OFDM output power for 64 QAM		-	15	-	dBm
	PA gain step	See Note [1]	-1.5	0.5	1.5dB	dB
A_{pl}	Accuracy of power leveling loop	-	-2	-	-2[2]	dB
TTpowup	Time for power up (from TxOn)	-	-	1.5	2	µs

[1]Guaranteed by design.

[2]Overall temperature -20 to 85°C

3.6 Synthesizer Composite Characteristics for 2.4GHz Operation

Table 3-7. **Synthesizer Composite Characteristics for 2.4 GHz Operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pn	Phase noise (at Tx_Out) At 30 KHz offset At 100 KHz offset At 500 KHz offset At 1 MHz offset	 - - - -	 - - - -	 –99 –99 –108 –115	 -95 -95 -100 -105	dBc/Hz
F_c	Center channel frequency	Center frequency at 5 MHz spacing [1]	2.312	-	2.484	GHz
BT_CLK_OUT	Reference oscillator frequency	± 20 ppm	-	26	-	MHz
BT_CLK_OUT_Pn	Phase noise at BT_CLK_OUT At 10KHz offset At 100KHz offset At 1MHz offset				 -149.3 -160.1 -164.1	dBc/Hz
BT_CLK_OUT_AMP	BT_CLK_OUT amplitude			1.2		V pk-pk
TS_{powup}	Time for power up (from sleep)	-	-	0.2	-	ms

[1]Frequency is measured at the Tx output.

3.7 Typical Power Consumption

Table 3-8 illustrate TYPICAL, room temperature power consumption data.

Table 3-8. **AR6102 Typical Power Consumption - Low Power States**

Mode		Current Consumption [mA]			Power Consumption [mW]
		@1.2 V	@1.8 V	@3.3 V	
Standby	CHIP_PWD	0.008	0.000	0.000	0.010
	HOST_OFF	0.050	0.007	0.001	0.076
	SLEEP	0.500	0.007	0.002	0.619
IEEE PS	DTIM=1	1.750	0.707	0.042	3.51
	DTIM=3	0.917	0.240	0.015	1.58
	DTIM=10	0.625	0.077	0.006	0.91

3.7.1 Measurement Conditions for Low Power State

T_amb = 25 ºC

All I/O pins except CHIP_PWD_L are maintained at their default polarities.

VDD_1.2V = VDD_12 = 1.2 V

VDD_BT = VDD_GPIO = VDD18_DVDD_SDIO = 1.8 V

VCC_FEM = 3.3 V

CHIP_PWD - all blocks power gated except for "Power, Clock Management"

HOST_OFF - all blocks power gated except for "Power, Clock Management", "SDIO", and "GSPI."

SLEEP - "LF CLK" running; all blocks voltage scaled or power gated except for "Power, Clock Management", "SDIO", "GSPI", and "GPIO"; internal state is maintained.

Table 3-9. **AR6102 Typical Power Consumption - Rx**

Rate [Mbps]	Rx			
	Current Consumption [mA]			Power Consumption [mW]
	@1.2 V	@1.8 V	@3.3 V	
1	64	28	2	134
2	64	28	2	134
5.5	69	28	2	140
11	69	28	2	140
6	67	28	2	138
9	68	28	2	139
12	68	28	2	139
18	69	28	2	140
24	70	28	2	141
36	71	28	2	143

Table 3-9. **AR6102 Typical Power Consumption - Rx**

	Rx			
	Current Consumption [mA]			Power Consumption
48	73	28	2	145
54	73	28	2	145

3.7.2 Measurement Conditions for Continuous Receive

T_amb = 25 ºC

VDD_12 = VDD_1.2VA = 1.2 V

VDD18 = 1.8 V = DVDD_SDIO = VDD_GPIO = VDD_BT

VCC_FEM = 3.3V

CHIP_PWD - all blocks power gated except for "Power, Clock Management"

HOST_OFF - all blocks power gated except for "Power, Clock Management", "SDIO", and "GSPI."

SLEEP - "LF CLK" running; all blocks voltage scaled or power gated except for "Power, Clock Management", "SDIO", "GSPI", and "GPIO"; internal state is maintained.

Table 3-10. **AR6102 Typical Power Consumption - Tx**

Rate [Mbps]	Target Output Power [dBm]	Current Consumption [mA] @1.2 V	@1.8 V	@3.3 V	Total Power Consumption [mW]
1	15	37	51	126	552
2	15	37	51	126	552
5.5	15	37	51	126	552
11	15	37	51	126	552
6	15	44	65	124	579
9	15	44	65	124	579
12	15	44	65	124	579
18	15	44	65	124	579
24	15	45	65	124	580
36	14	45	58	116	541
48	13	45	55	109	513
54	12	45	65	105	518

3.7.3 Measurement Conditions for Continuous Transmit

T_amb = 25 ºC

VDD_12 = VDD_1.2VA = 1.2 V

VDD18 = 1.8 V = DVDD_SDIO = VDD_GPIO = VDD_BT

VCC_FEM = 3.3V

3.8 Power Sequence Operation

I/O Supply = VDD18, DVDD_SDIO, VDD_GPIO, VDD_BT, VCC_FEM

1.2V Supply = VDD_1.2VA, VDD_12

NOTE: It is important that all I/O supplies come up at the same time. CHIP_PWD_L or SYS_RST_L need to be toggled after all supplies are stable in order to ensure proper reset.

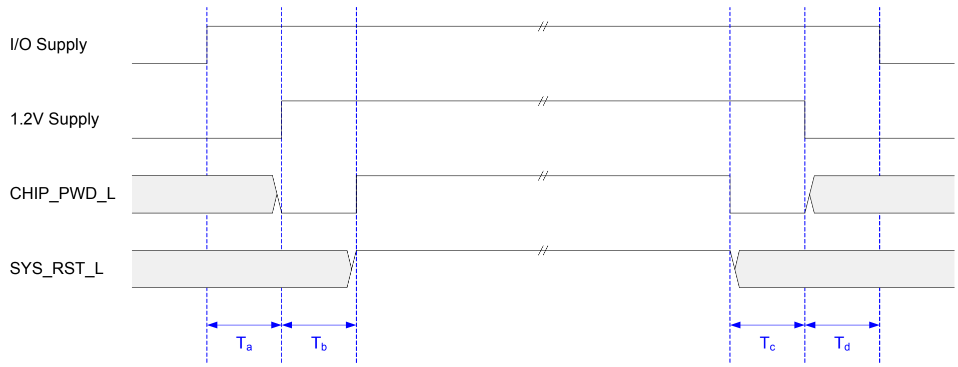


Figure 3-1. **Power Up/Power Down Timing While Asserting CHIP_PWD_L**

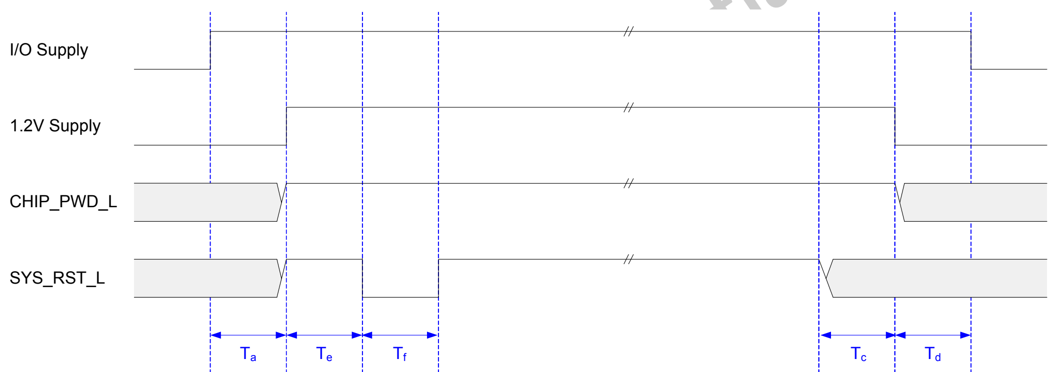


Figure 3-2. **Power Up/Down Timing While Asserting SYS_RST_L**

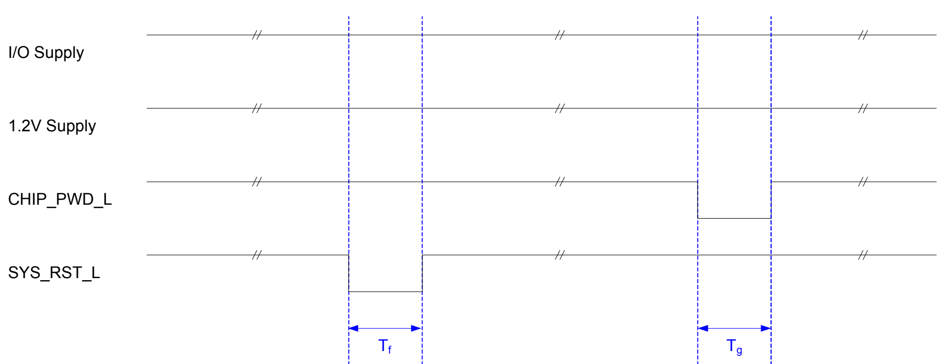


Figure 3-3. **Reset and Power Cycle Timing**

Table 3-11. **Timing Diagram Definitions**

	Description	**Min (μsec)**
T_a	Time between I/O supply valid** and 1.2V supply valid	0[1]
T_b	Time between 1.2V supply valid and CHIP_PWD_L deassertion	5
T_c	Time between CHIP_PWD_L or SYS_RST_L assertion and 1.2V supply invalid	0
T_d	Time between CHIP_PWD_L or SYS_RST_L assertion and 1.2V supply invalid	N/A***
T_e	Time between 1.2V supply valid and SYS_RST_L assertion	0
T_f	Length of SYS_RST_L pulse	1
T_g	Length of CHIP_PWD_L pulse	5

[1] If Ta were negative, there would be additional leakage power which would not exceed 15mW on the 1.2V supply and 150uW on the I/O supply under recommended operating conditions. There would be no functional impact as long as the remainder of the power up timing is followed.
** Supply valid represents the voltage level has reached 90% level.
*** No strict requirement for this parameter.
This parameter can also be negative.

4. AC Specifications

4.1 External 32KHz Input Clock Timing

Figure 4-1 and Table 4-1 show the external 32 KHz input clock timing requirements.

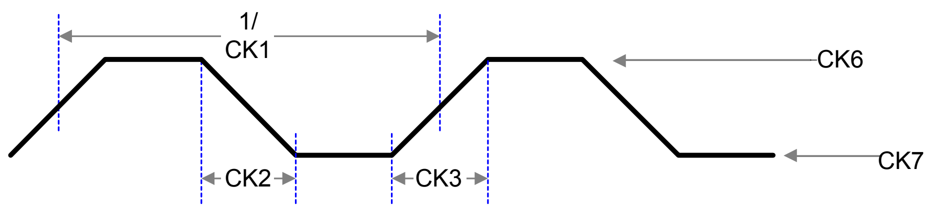


Figure 4-1. **External 32 KHz Input Clock Timing Requirements**

Table 4-1. **External 32 KHz Input Clock Timing**

Symbol	Description	Min	Typ	Max	Unit
CK1	Frequency	-	32.768	-	KHz
CK2	Fall time	1	-	100	ns
CK3	Rise time	1	-	100	ns
CK4	Duty cycle (high-to-low ratio)	15	-	85	%
CK5	Frequency stability	–50	-	50	ppm
CK6	Input high voltage	0.8*VDD_BT	-	VDD_BT+0.2	V
CK7	Input low voltage	-0.3	-	0.2*VDD_BT	V

4.2 SDIO/GSPI Interface Timing

Figure 4-2 shows the write timing for a SDIO style transaction.

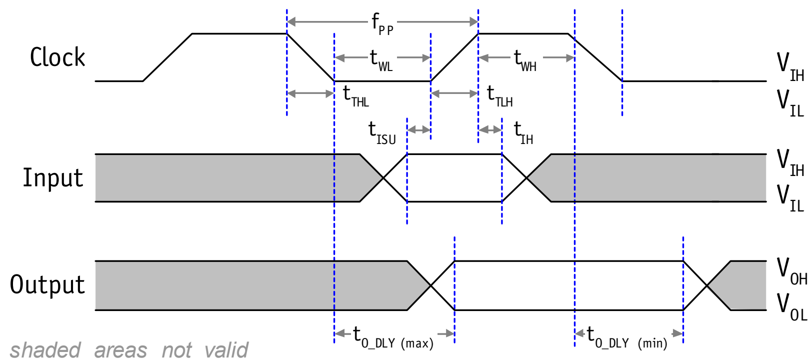


Figure 4-2. **SDIO Timing**

Table 4-2 shows the values for timing constraints for SDIO.

Table 4-2. **SDIO Timing Constraints**

Parameter	Description	Min	Max	Unit	Note
f_{PP}	Clock frequency data transfer mode	0	25	MHz	100 pF ≥ C_L (7 cards)
t_{WL}	Clock low time	10	-	ns	100 pF ≥ C_L (7 cards)
t_{WH}	Clock high time	10	-	ns	100 pF ≥ C_L (7 cards)
t_{TLH}	Clock rise time	-	10	ns	100 pF ≥ C_L (10 cards)
t_{THL}	Clock fall time	-	10	ns	100 pF ≥ C_L (7 cards)
t_{ISU}	Input setup time	5	-	ns	25 pF ≥ C_L (1 card)
t_{IH}	Input hold time	5	-	ns	25 pF ≥ C_L (1 card)
$t_{O\_DLY\ (min)}$	Output delay time during data transfer mode	0	14	ns	25 pF ≥ C_L (1 card)
$t_{O\_DLY\ (max)}$	Output delay time during identification mode	0	50	ns	25 pF ≥ C_L (1 card)

5. Application Guidelines

5.1 Typical 11b/g Application

For applications that require only 802.11b/g single-antenna operation without the need for cellular and/or Bluetooth coexistence, the AR6102 can be used with a minimal number of external passive components. This is especially advantageous for low-cost, small form-factor consumer electronics devices such as PMPs, PNDs, gaming devices, and cameras. See Figure 5-1 for details. This design is the basis of the implementations in subsequent sections.

Table 5-1 shows the minimum RBOM for typical 11b/g application.

5.2 Application Schematic

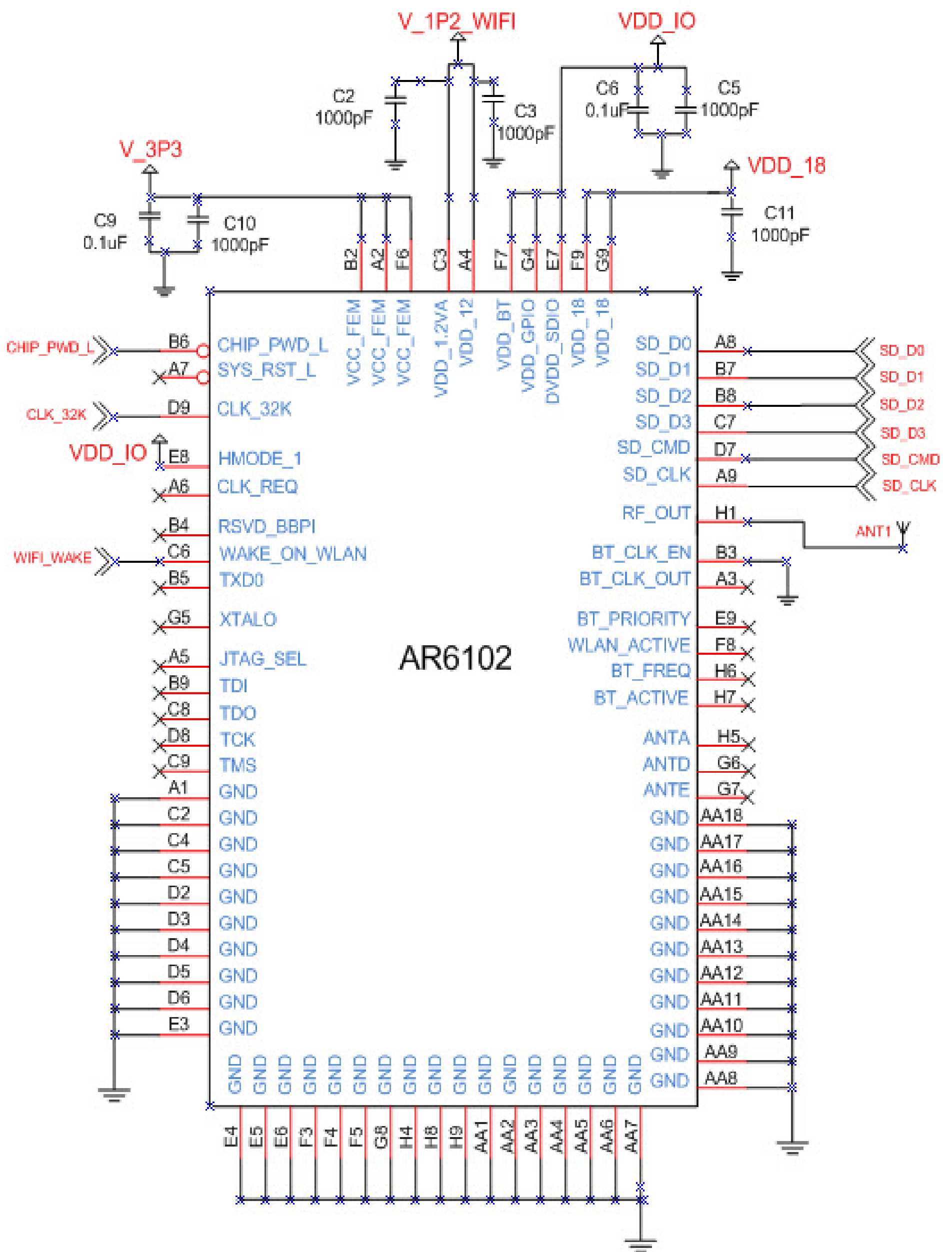


Figure 5-1. **Application Schematic**

Table 5-1. **Minimum RBOM for Typical 11b/g Application**

Item	Qty.	Description	Designator	Size	Value
1	5	Capacitor	C2, C3, C5, C10, C11	0201	1000pF
2	2	Capacitor	C6, C9	0201	0.1uF
3	1	Antenna	ANT1	N/A	N/A

5.3 11b/g Application with Cellular Coexistence Filter

For those applications that are used in an environment with interference from cellular radios, an external band-pass filter may be used with the AR6102. This filter is installed between the AR6102 RF output port and the antenna. Atheros recommends several filters below, each with different characteristics. Depending on design constraints related to size, insertion loss, or attenuation at certain critical frequency bands, an appropriate filter can be chosen. See Table 5-2 for details.

Table 5-3 shows the AR6102 output spur levels for 15dBm 1Mbps transmit.

Table 5-2. **Recommended Co-existence Bandpass Filters**

	Filter Attenuation (dB)					
Cellular Frequencies	Murata LFB212G45CE2D006	TDK DEA202450BT-3201B2	TDK DEA162450BT-2092AT1-H	Soshin HMD847H	Soshin HMD844H	Soshin HMD848H
2.17 GHz	30	26	30	20	12	35
1.99 GHz	35	40	40	40	20	40
1.91 GHz	40	40	40	40	20	40
1.79 GHz	40	40	40	40	28	40
824 MHz	40	40	40	40	30	40
Insertion Loss (dB)	2.7	2.5	3.0	2.5	1.5	3.2
Size (L x W x H mm)	2.0 x 1.25 x 0.6	2.0 x 1.25 x 0.8	1.60 x 0.8 x 0.6	2.0 x 1.25 x 1.0	2.0 x 1.25 x 0.8	2.0 x 1.25 x 0.8

Table 5-3. **Output Spur Levels for 15dBm 1Mbps Transmit**

Modulated Data Rate	Frequency (GHz)	Spur Level
1Mbps	1.8196	-88.75
	1.8461	-83.61
	1.8981	-86.8
	1.9501	-89.56
	2.0021	-94.4
	2.0541	-92.54
	2.1061	-92.56

5.4 11b/g Application with Bluetooth-Coexistence

The AR6102 supports the standard 2, 3, and 4-wire Bluetooth coexistence handshake protocol. As such, it can easily interface with any 3rd party Bluetooth device which supports this interface. The pins used for each coexistence interface are described in the Figure 5-2.

Table 5-4. **Bluetooth Coexistence Interface Pins**

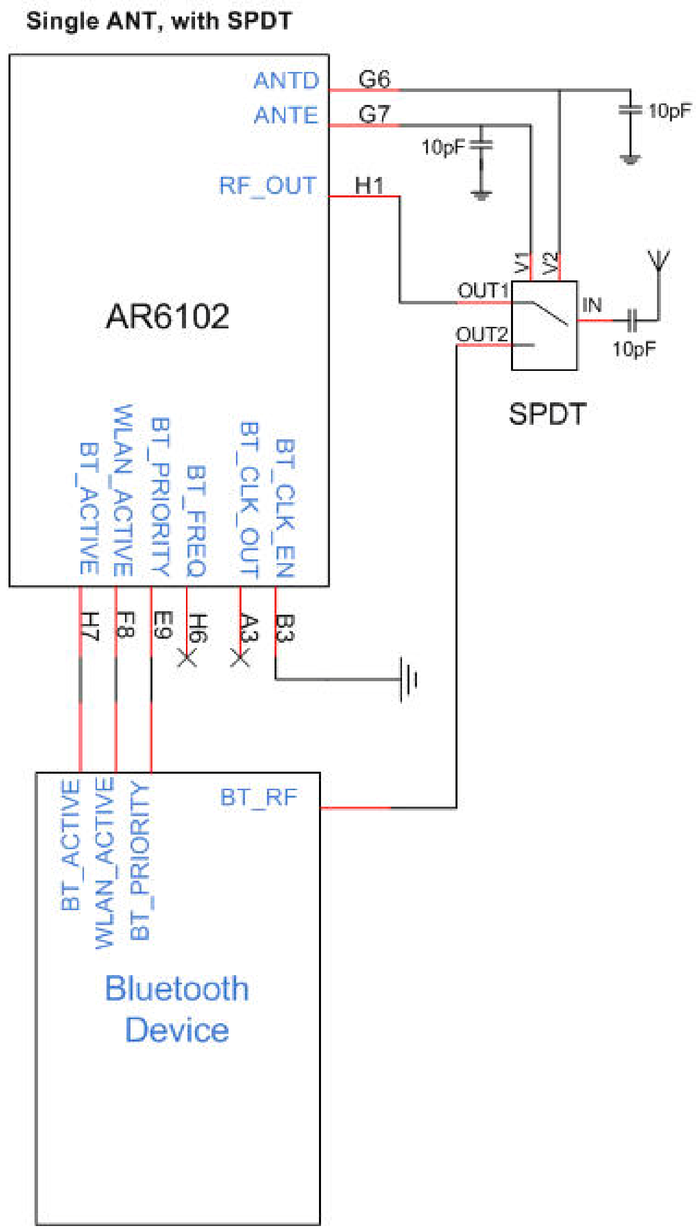
	2-Wire	3-Wire	4-Wire
BT_ACTIVE	Signals when the BT device is expecting or is currently performing Tx or Rx activity. It remains asserted until the BT device is finished using the medium.		
BT_PRIORITY	Not used. Leave as is.	Asserts when current BY activity is high priority (e.e., SCO LMP traffic	Time-shared pin: At the start of BT_ACTIVE, it asserts to indicate BT activity priority. Then indicates BT activity, whether it is Tx or Rx
BT_FREQ	Not used. Leave as is.	Not used. Leave as is.	Indicates whether the BT device is using a restricted channel occupied by WLAN; signal is only applicable for non-AFH BT devices and provides no benefits if using AFH with WLAN, and/or if BT has low RF isolation from WLAN. The functionality of this pin is made obsolete by the Atheros coexistence scheduler.
WLAN_ACTIVE	Indicates whether WLAN grants or blocks BT's Tx/Rx request. The pin polarity is configurable. By default, when asserted, it signals to BT that it has WLAN activity and is blocking BT from using the medium.		

Because the 3-wire interface offers robust coexistence performance and is the most widely adopted, the focus for the implementation will be on this interface. In addition, since most embedded applications utilize a single antenna for WLAN and BT to share, the hardware implementation will focus on the components and control signals that are required for single antenna coexistence.

Given the single-antenna requirement and the fact that WLAN transmit and receive will occur at one port, the following front-end options are available. These options, along with some high level advantages/disadvantages are summarized in the table below

Table 5-5. **Front End Options - Advantages and Disadvantages**

	Single ANT, with SPDT
Advantages	Lowest path loss for both WLAN and BT, which allows for highest output power and receive sensitivy. Targeted for higher performance at longer range.
Disadvantages	No simultaneous WLAN and BT activity, since only one device has access to the antenna at any given time.



V1	V2	IN-OUT1	IN-OUT2
High	Low	ON	OFF
Low	High	OFF	ON

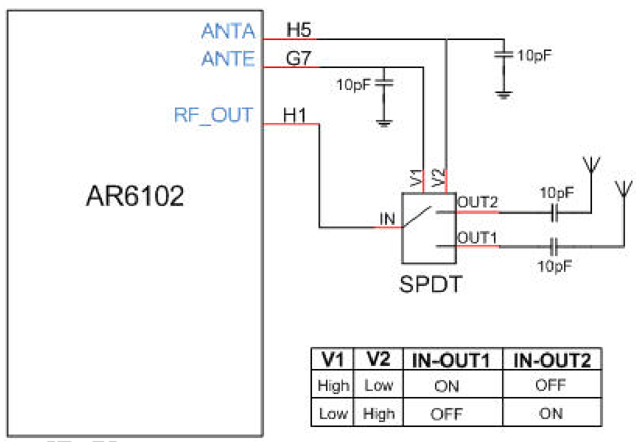
Figure 5-2. **Bluetooth Coexistence Application**

It is important to connect the switch control lines such that BT_RF has the antenna when ANTD is HIGH. The reason for this is that when WLAN is asleep or in power-down/reset mode, ANTD defaults to a HIGH and hence allows BT to take control of the medium while WLAN is not being used. Power to the VCC_FEM pins must be continually supplied in each of the operating modes in order to maintain the switch state. While in power-down or power-save mode, the voltage on ANTD ranges from 1.9 - 2.4V across the full range of VCC_FEM (3.0 - 4.2V). Therefore, it is important to select a switch that operates with a switch control voltage between 1.9 - 2.4V in order to allocate the RF path to BT while the WLAN device is in power-down or power-save mode.

Figure 5-3 depict the major components and signal connections that are necessary for implementing the options summarized in Table 5-5.

5.5 11b/g Application with Antenna Diversity

The AR6102 supports fast antenna diversity with the addition of an external SPDT switch and the use of two antennas. A recommended SPDT switch is the NEC uPG2158T5K. To achieve the maximum benefits of antenna diversity, it is recommended to place the antennas as far apart as possible.



V1	V2	IN-OUT1	IN-OUT2
High	Low	ON	OFF
Low	High	OFF	ON

Figure 5-3. **AR6102 Fast Antenna Diversity Implementation**

5.6 Power Supply Management

The AR6102 requires various power supplies and are described in the table below. The recommended operating conditions for each power supply are also given. It is important to note the current consumption on each supply rail (refer to Table 3-8, 3-9, and 3-10) in order to budget the typical amount of power that needs to be delivered to each supply. Maximum current consumption across temperature and voltage is given in Table 5-6.

5.7 Supply Ripple Tolerance

The maximum ripple that can be tolerated on the VDD18 and 1.2V supplies is 45 mVp-p and 15 mVp-p, respectively.

Table 5-6. **Power Supplies and Recommended Operating Conditions**

Symbol	Description / Recommendations	Min.	Typ.	Max	Unit
VCC_FEM	■ Supplies internal PA and RF switch controls. ■ When using an off-module switch, as in the case for antenna diversity implementations, it is important to make sure that VCC_FEM is at least 100mV higher than the recommended control signal levels of the off-module switch. ■ Maximum current consumption of 165mA.	3.0	3.3	3.6	V
VDD_1.2VA	■ Supplies critical analog RF and baseband blocks such as the 2.4GHz Tx/Rx chain, synthesizer, and current reference circuitry. ■ Bypass this supply with a 1000pF capacitor placed close to the supply pin. Refer to C2 in Section 5.2 and layout guidelines for details. ■ Combined VDD_1.2VA and VDD_12 current is 97mA MAX.	1.14	1.2	1.26	V
VDD_12	■ Supplies the internal digital logic. ■ This can share the same supply as the VDD_1.2VA pin. ■ Bypass this supply with a 1000pF capacitor placed close to the supply pin. Refer to C3 in the "Application Schematic" and layout guidelines for details. ■ Combined VDD_1.2VA and VDD_12 current is 97mA MAX.	1.14	1.2	1.26	V
VDD_BT	■ Supplies the BT co-existence I/O interface: BT_Priority / GPIO0 WLAN_ACTIVE / GPIO1 BT_FREQ / GPIO2 BT_ACTIVE / GPIO3 CLK32K - External 32KHz clock input pin ■ The voltage for this supply should be set at the same level as the voltage of the I/O interface. ■ VDD_BT and sleep clock amplitude should match	1.71	1.8	3.46	V
VDD_GPIO	■ Supplies the WAKE_ON_WLAN pin and UART interface pin. ■ The voltage for this supply should be set at the same level as the voltage of the I/O interface.	1.71	1.8	3.46	V
DVDD_SDIO	■ Supplies the SDIO interface, HMODE_1 strap configuration pin, and JTAG interface. ■ Voltage level should be set at the same level as the host SDIO interface.	1.71	1.8	3.46	V
VDD18	■ Supplies the RF analog circuitry. ■ Bypass this supply with a 1000pF capacitor placed close to the supply pin. Refer to C11 in the and layout guidelines. Refer to C11 in the "Application Schematic" and layout "Application Guidelines" on page 25 for details. ■ Maximum current consumption of 83mA	1.71	1.8	1.89	V

5.8 Grounding

The AR6102 ground pads are not differentiated between digital and analog grounds. As such, all grounds should be connected together on the end application board.

5.9 Host Interfaces and GPIOs

5.9.1 Secure Digital Input/Output (SDIO)

The AR6102 is compliant with SDIO v1.1 specifications. For 4-bit mode, all four SDIO data lines are available. If 1-bit mode is turned on by software, data is sent only over SD_D0; this mode is good for troubleshooting (ie., driver loading issues). The table below describes the SDIO mode pins.

Table 5-7. **SDIO Mode Pins**

Pin Name	SDIO Type	Pad Power Supply	Description
SD_CLK	I	DVDD_SDIO	SDIO input clock from Host (up to 25MHz). No external pull-up resistor needed.
SD_Cmd	I/O		SDIO Command Line Internal pull-up, no external pull-up resistor needed.
SD_D0	I/O		SDIO Data0 Line Internal pull-up, no external pull-up resistor needed.
SD_D1	I/O		SDIO Data1 Line Internal pull-up, no external pull-up resistor needed.
SD_D2	I/O		SDIO Data2 Line Internal pull-up, no external pull-up resistor needed.
SD_D3	I/O		SDIO Data3 Line Internal pull-up, no external pull-up resistor needed.

5.9.2 Dedicated Function Pins

- BT Coexistence
  - Dedicated to WLAN-BT coexistence using a four-wire bus:

    BT_PRIORITY

    WLAN_ACTIVE

    BT_FREQ

    BT_ACTIVE
- Sleep Clock
  - Dedicated to 32KHz clock input (CLK_32K)
- UART Output
  - Dedicated to UART Tx (TXD0)
- Wake-on-Wireless
  - Dedicated for wake-on-wireless feature (WAKE_ON_WLAN), a hardware toggle point from the WLAN device to the HOST. Generally, once the system (and thus the WLAN device) is placed into a low-power state, the WLAN device continues to remain associated with its current AP to receive and monitor incoming frames.
  - If one of a number of specified patters are detected in the frame, the WLAN device wakes up HOST by asserting a hardware pin. Upon wakeup, the driver for the HOST is notified of the change in power state and data connectivity with the AP is re-established. Because this

defaults low, the wake-on-wireless interrupt is active high.

5.10 RF Port Matching

The AR6102 uses a single port, LGA pad H1, as an RF input/output for receive/transmit operation. No external DC-block is necessary.

For optimal performance, all connections to this port, including traces and antennas, should have a 50-ohm impedance.

5.11 External 32KHz Sleep Clock

Two hardware solutions exist for the 32KHz sleep clock:

- External sleep clock driven by an XO
- HOST driven sleep clock

The AR6102 has the ability to provide a buffered 26MHz clock on the BT_CLK_OUT pin. Please refer to Table 3-7 for information about the characteristics of this clock.

5.12 Clock Sharing

To save layout area and BOM, the HOST 32KHz drive option is recommended for use in the end application. When a HOST 32KHz drive or external oscillator is used, the clock should be DC-coupled into the CLK_32K pin.

If the sleep clock voltage swing level exceeds that of the DVDD_SDIO voltage, then a 1K-ohm series resistor at the CLK_32K input is necessary. Depending on the drive strength of the clock source, this resistance may need to be lowered to meet the rise time requirements.

The buffered clock that is driven out on BT_CLK_OUT is enabled by driving BT_CLK_EN to 1.8V. It is enabled using this signal only and can be enabled regardless of the power state of the AR6102 (power-down mode, sleep and awake modes). As long as the VDD_1.2VA and VDD18 supplies are given to the device and the BT_CLK_EN is driven high, the buffered clock output will be available.

There is a minimal current consumption penalty when enabling this clock. Typically, there will be an additional 490uA of current on the VDD18 supply and an additional 458uA on the VDD_1.2VA supply (regardless of operating mode) when the buffered clock is enabled.

5.13 Host Configuration Guidelines

The option to use SDIO is selected by tying HMODE_1 to the same voltage level as VDD_SDIO.

5.14 Layout Guidelines

5.14.1 General Guidelines

A cost effective design can be realized by utilizing vias formed with a 6 mil drill, 11 mil pad, with 2.5 mil angular ring; these can be used to route the 0.35 x 0.35 pads on other layers. The figure below depicts an example of the via placement and escape routes used for each of the inner pads.

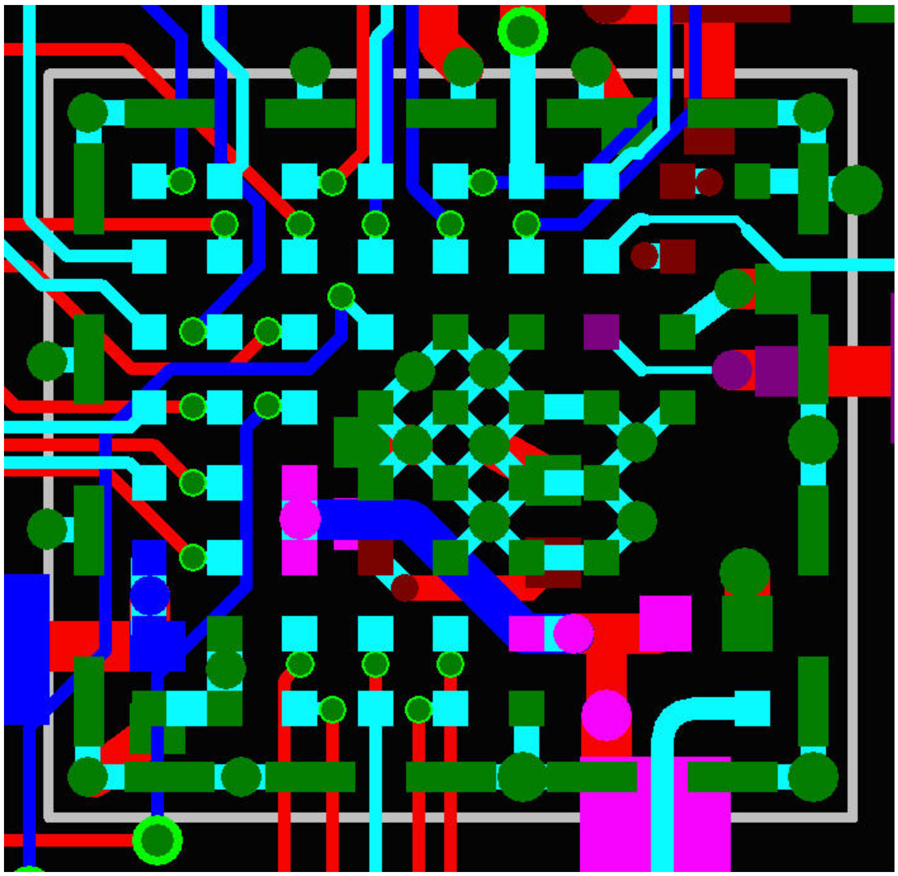


Figure 5-4. **Layout Diagram**

In general, the AR6102 can be routed on a 4-layer board assuming the following layer usage:

Layer 1: Signals and RF traces.

Layer 2: Mainly ground with some signals. RF traces on layer 1 should traverse over solid ground planes on layer 2.

Layer 3: Power planes

Layer 4: More signals

5.14.2 Component Placement

All bypass capacitors depicted in the reference schematic need to be place as close as possible to the AR6102. Placing these bypass components on the backside of the board is fine, as long as the physical distance to the supply pin is reduced. Supplies that share a regulator need to have bypass capacitors placed close to the AR6102 and prior to the traces joining.

5.15 VDD_12 and VDD_1.2VA Power Trace Routing

It is critical to route the VDD_12 and VDD_1.2VA supplies using separate traces. Each trace should have a bypass capacitor placed close to the power supply input pin. The traces should only be connected at a central, noise-free node in a star configuration.

See Figure 5-5 for details. Bypassing these two supplies separately is required for optimal EVM and spectrum mask performance.

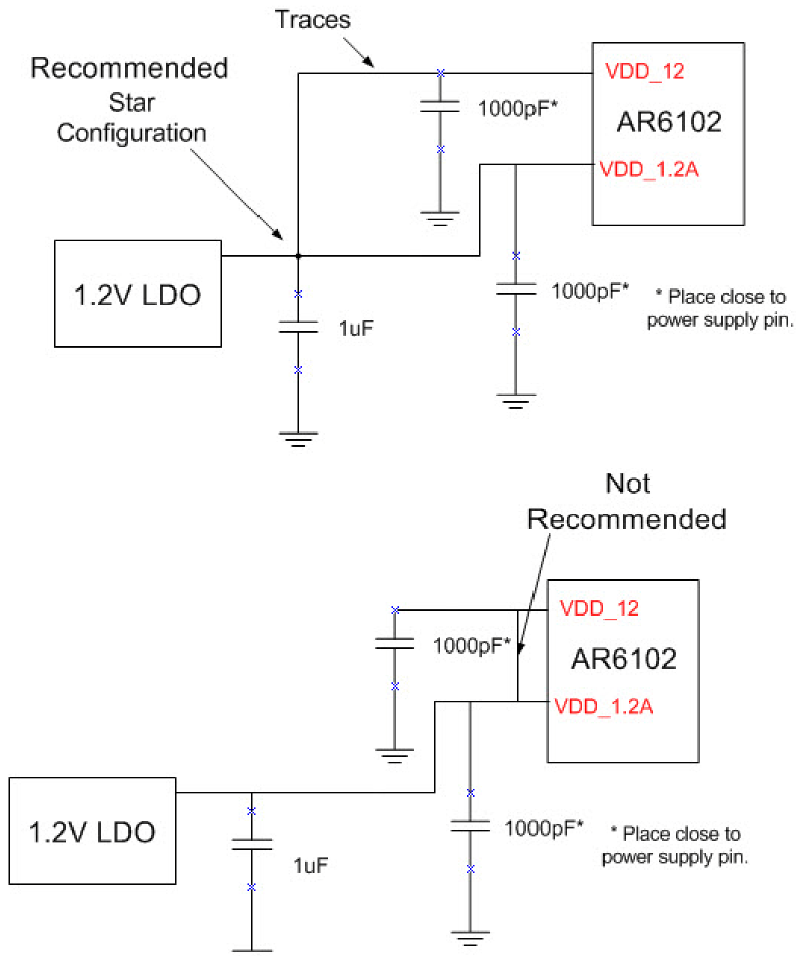


Figure 5-5. **Recommended Star Configuration**

5.15.3 Host Interface Layout

For the layout of the host interface signals SD_CLK, SD_CMD, and SD_D[3:0], the following should be checked:

- Verify that GND with uniform vias between the top and bottom layers is incorporated between the CLK line and the data line(s).
- Avoid connections on data and clock lines due to high speed digital voltage returns and inductive characteristics of vias (which can also incorporate capacitive characteristics due to layer to layer capacitance).
- If the AR6102 is to be used on a development platform, it is recommended to incorporate an extra RC filter on the SD_CLK line or other data lines. This is to allow tenability against different hosts which may require different overshoot handling due to length of the interface traces. Keep capacitor values in the RC filter to a minimal value.

5.15.4 32KHz Clock Signal Layout

For an optimal sleep clock signal layout, the designer must keep the clock trace away from digital and power traces.

5.15.5 Grounding

The layout designer must avoid ground discontinuity. RF traces should have solid grounding directly under the entire trace for proper impedance control.

6. Assembly Guidelines

6.1 Reflow profile

Figure 6-1 shows the Reflow Profile.

See Table 6-1 for the recommended reflow settings.

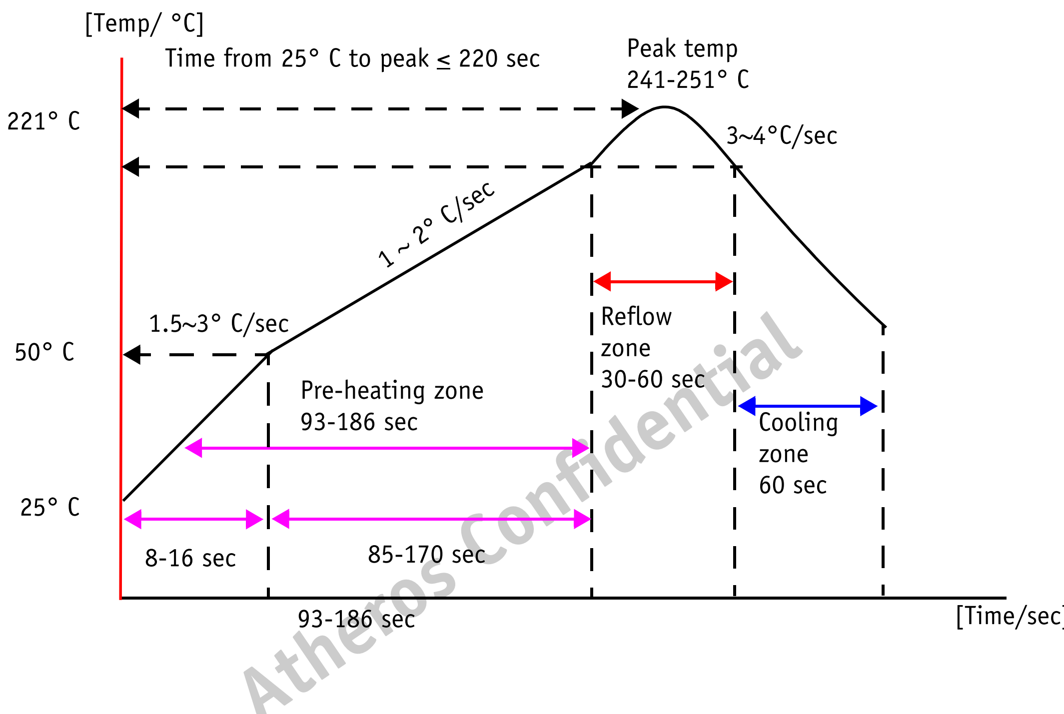


Figure 6-1. **Reflow Profile**

Table 6-1. **Recommended Reflow Settings**

Zone						
	Dry Zone	Pre-heat Zone	Reflow Zone	Peak Zone	Cooling	Atmosphere
Temp ° C	25-50	50-221	221	241-251	217-50	N2
Time (sec)	90	65	45	2	60	

6.2 Solder material recommendations

Manufacturer name: Kester

Solder paste part number: EM808-Sn96.5% Ag3.0% Cu0.5% SAC305 alloy with Type 3 power, water soluble solder paste

7. Package Marking Information

The chapter explains the package marking on the AR6102. See Figure 7-1 for details.

Figure 7-1. **AR6102 Package Marking**

8. Ordering Information

Please contact your local Atheros sales representative at one of the worldwide offices listed below.

Atheros Communications, Inc.
5480 Great America Parkway
Santa Clara, CA 95054
t +1 408.773.5200
f +1 408.773.9940
info@atheros.com

Atheros Communications Irvine
8 Hughes
Irvine, Ca. 92618
t 949.453.2727
f 949.341.0423
info@atheros.com

Atheros Hong Kong Limited
P.O. Box No. 333, Fo Tan Post Office,
N.T., Hong Kong
t +852 8206.1131
f +852 8206.1301
sales_china@atheros.com

Atheros (Shanghai) Co., Ltd.
690 Bibo Road,4F,Unit 9
Shanghai,P.R.China
201203
t +86-21.5080.3680
f +86 21.5027.0100
sales_china@atheros.com

Atheros GmbH
Braunschweiger Str. 8
45886 Gelsenkirchen
Germany
Amy.Chang@atheros.com

Atheros Communications KK-Japan
KDX Shinbashi Bldg.
2-9, 2-chome Shinbashi, Minato-ku,
Tokyo 105-0004, Japan
t +81 3.5501.4100
f +81 3.5501.4129
sales_japan@atheros.com

Atheros Korea
1218, 12F, Downtown Bldg., 22-3
SuNae-dong, Bundang-ku, Seongnam City,
Gyeonggi-do, Korea 463-825
t +82 31.786.0428
sales_korea@atheros.com

Atheros Technology Taiwan Corporation
9F, No.110, Chou Tze St, Nei Hu Dist,
Taipei, Taiwan 114 R.O.C.
t + 886 2.8751.6385
f + 886 2.8751.6397
sales_tw@atheros.com

MKG-0942 Rev. 2

Atheros Communications, Incorporated
5480 Great America Parkway
Santa Clara, CA 95054
t: 408/773-5200
f: 408/773-9940
www.atheros.com