DDR2 SDRAM

SAA64M4.....– 16 Meg x 4 x 4
SAA32M8.....– 8 Meg x 8 x 4
SAA16M16.....– 4 Meg x 16 x 4

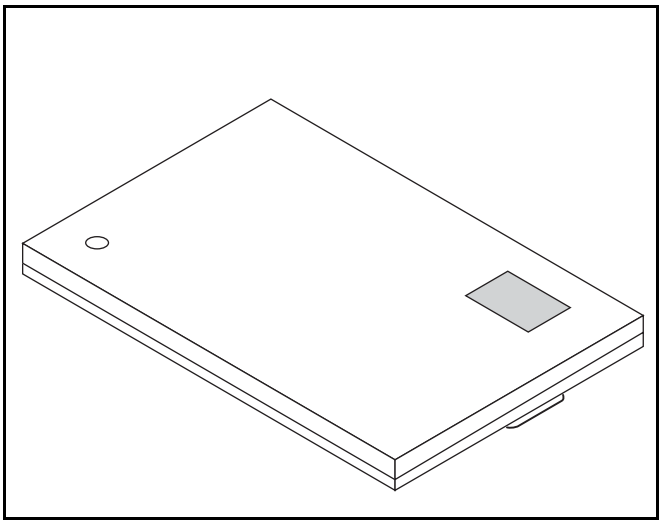
For the latest data sheet, please refer to the SpecTek Web site: http://www.spectek.com

Features

- ROHS compliant
- VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Programmable CAS Latency (CL): 3 and 4
- Posted CAS additive latency (AL): 0, 1, 2, 3, and 4
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)

Options[1, 2]	Designation
• SpecTek Memory	SAA
• Configuration	
64 Meg x 4 (16 Meg x 4 x 4)	64M4
32 Meg x 8 (8 Meg x 8 x 4)	32M8
16 Meg x 16 (4 Meg x 16 x 4)	16M16
• Product Code	
DDR2	Ux[3]
• Density	
256 Megabits	6x[3]
• Voltage/Refresh	
1.8V/8K refresh	O8
• Package – Lead-Free	
x4, x8	
60-ball FBGA (8mm x 12mm)	FIF
x16	
84-ball FBGA (8mm x 14mm)	FPF
• Package – Leaded	
x4, x8	
60-ball FBGA (8mm x 12mm)	FIL
x16	
84-ball FBGA (8mm x 14mm)	FPL
• Timing – Cycle Time	
3.0ns @ CL = 5 (DDR2-667)	-3
3.75ns @ CL = 4 (DDR2-533)	-37E

NOTE:
1. See page 42 for part number options and designations used prior to March 2005.
2. See page 42 for part number options and designations used prior to July 2006.
3. Contact SpecTek Sales for details on availability of the "x" placeholders



Architecture	64 Meg x 4	32 Meg x 8	16 Meg x 16
Configuration	16 Meg x 4 x 4	8 Meg x 8 x 4	4 Meg x 16 x 4
Refresh Count	8K	8K	8K
Row Addressing	8K (A0–A12)	8K (A0–A12)	8K (A0–A12)
Bank Addressing	4 (BA0–BA1)	4 (BA0–BA1)	4 (BA0–BA1)
Column Addressing	2K (A0–A9, A11)	1K (A0–A9)	512 (A0–A8)

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MHz)		^{t}RCD (ns)	^{t}RP (ns)	^{t}Rc (ns)
	CL = 4	CL = 5			
-3	NA	667	15	15	60
-37E	533	533	15	15	60

Part Number Example:
SAA32M8U26AO8FIF-37E

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FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. SpecTek's new FBGA part marking decoder makes it easier to understand FBGA part marking. Visit the SpecTek web site at www.spectek.com/pdfs/fbga_decoder.pdf .

General Description

The 256Mb DDR2 SDRAM is a high-speed, CMOS dynamic random-access memory containing 268,435,456 bits. It is internally configured as a quad-bank DRAM. The functional block diagrams of the 16 Meg x 16, 32 Meg x 8, and 64 Meg x 4 devices, respectively are shown in the Functional Description section. Ball assignments for the 64 Meg x 4 are shown in Figure 1 and signal descriptions are shown in Table 1. Ball assignments for the 32 Meg x 8 and 64 Meg x 4 are shown in Figure 2 and signal descriptions are shown in Table 2.

The 256Mb DDR2 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 256Mb DDR2 SDRAM effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte (LDQS, LDQS#) and one for the upper byte (UDQS, UDQS#).

The 256Mb DDR2 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR2 SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR2 SDRAM provides for programmable read or write burst lengths of four or eight locations. DDR2 SDRAM supports interrupting a burst read of eight with another read, or a burst write of eight with another write. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAMs, the pipelined, multibank architecture of DDR2 SDRAMs allows for concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving power-down mode.

All inputs are compatible with the JEDEC standard for SSTL_18. All full drive-strength outputs are SSTL_18-compatible.

NOTE:
1. The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.
2. Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into two bytes, the lower byte and upper byte. For the lower byte (DQ0 through DQ7) DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ8 through DQ15) DM refers to UDM and DQS refers to UDQS.
3. Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
4. Any specific requirement takes precedence over a general statement.

Figure 1: 84-ball FBGA Pin Assignment (x16), 8mm x 14mm (Top View)

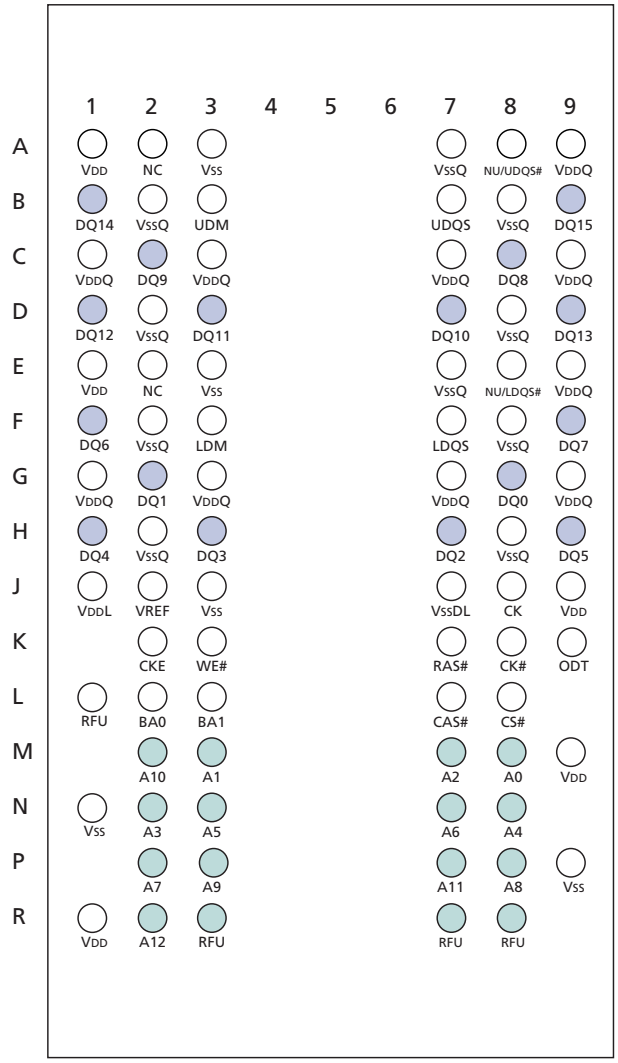


Figure 2: 60-Ball FBGA Pin Assignment (x 4, x 8), 8mm x 12mm (Top View)

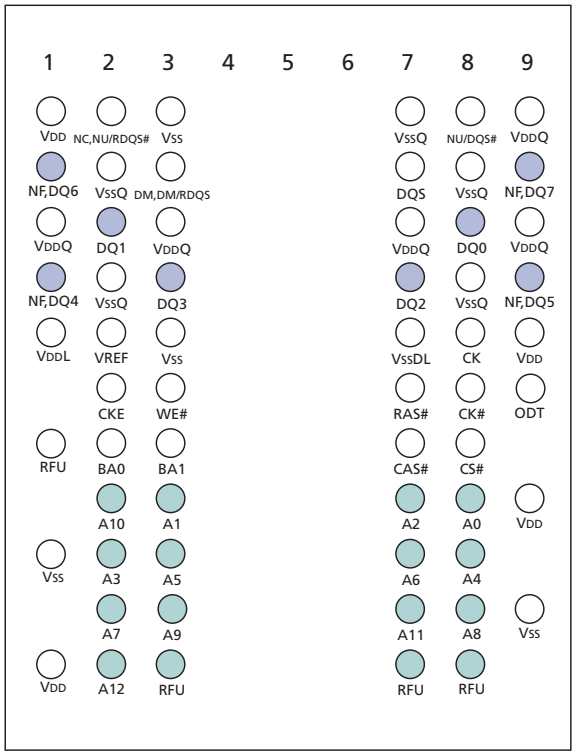


Table 2: FBGA Ball Descriptions 64 Meg x 4, 32 Meg x 8, 16 Meg x 16

x16 FBGA BALL ASSIGNMENT	x4, x8 FBGA BALL ASSIGNMENT	SYMBOL	TYPE	DESCRIPTION
K9	F9	ODT	Input	On-Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ0–DQ15, LDM, UDM, LDQS, LDQS#, UDQS, and UDQS# for the x16; DQ0-DQ7, DQS, DQS#, RDQS, RDQS#, and DM for the x8; DQ0-DQ3, DQS, DQS#, and DM for the x4. The ODT input will be ignored if disabled via the LOAD MODE command.
J8, K8	E8, F8	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
K2	F2	CKE	Input	Clock Enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry, POWER-DOWN exit, output disable, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once Vdd is applied during first power-up. After Vref has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh operation V_{REF} must be maintained.
L8	G8	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple ranks. CS# is considered part of the command code.
K7, L7, K3	F7, G7, F3	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
F3, B3	B3	LDM, UDM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. LDM is DM for lower byte DQ0–DQ7 and UDM is DM for upper byte DQ8–DQ15.
L2, L3	G2, G3	BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LOAD MODE command.

Table 2: FBGA Ball Descriptions 64 Meg x 4, 32 Meg x 8, 16 Meg x 16

x16 FBGA BALL ASSIGNMENT	x4, x8 FBGA BALL ASSIGNMENT	SYMBOL	TYPE	DESCRIPTION
M8, M3, M7, N2, N8, N3, N7, P2, P8, P3, M2, P7, R2	H8, H3, H7, J2, J8, J3, J7, K2, K8, K3, H2, K7, L2	A0–A12	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for Read/Write commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
G8, G2, H7, H3, H1, H9, F1, F9, C8, C2, D7, D3, D1, D9, B1, B9	–	DQ0–DQ15	I/O	Data Input/Output: Bidirectional data bus for 16 Meg x 16.
–	C8, C2, D7, D3, D1, D9, B1, B9	DQ0–DQ7	I/O	Data Input/Output: Bidirectional data bus for 32 Meg x 8.
–	C8, C2, D7, D3	DQ0–DQ3	I/O	Data Input/Output: Bidirectional data bus for 64 Meg x 4.
B7, A8	–	UDQS, UDQS#	I/O	Data Strobe for Upper Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
F7, E8	–	LDQS, LDQS#	I/O	Data Strobe for Lower Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
–	B7, A8	DQS, DQS#	I/O	Data Strobe: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
–	B3, A2	RDQS, RDQS#	Output	Redundant Data Strobe for 32 Meg x 8 only. RDQS is enabled/ disabled via the LOAD MODE command to the Extended Mode Register (EMR). When RDQS is enabled, RDQS is output with read data only and is ignored during write data. When RDQS is disabled, pin B3 becomes Data Mask (see DM pin). RDQS# is only used when RDQS is enabled AND differential data strobe mode is enabled.
A1, E1, J9, M9, R1	A1, E9, H9, L1	V_{DD}	Supply	Power Supply: 1.8V ±0.1V
J1	E1	V_{DDL}	Supply	DLL Power Supply: 1.8V ±0.1V
A9, C1, C3, C7, C9, E9, G1, G3, G7, G9	A9, C1, C3, C7, C9	V_{DDQ}	Supply	DQ Power Supply: 1.8V ±0.1V. Isolated on the device for improved noise immunity.
J2	E2	V_{REF}	Supply	SSTL_18 reference voltage.
A3, E3, J3, N1, P9	A3, E3, J1, K9	V_{SS}	Supply	Ground.
J7	E7	V_{SSDL}	Supply	DLL Ground. Isolated on the device from V_{SS} and V_{SSQ}.
A7, B2, B8, D2, D8, E7, F2, F8, H2, H8,	A7, B2, B8, D2, D8	V_{SSQ}	Supply	DQ Ground. Isolated on the device for improved noise immunity.

Table 2: FBGA Ball Descriptions 64 Meg x 4, 32 Meg x 8, 16 Meg x 16

x16 FBGA BALL ASSIGNMENT	x4, x8 FBGA BALL ASSIGNMENT	SYMBOL	TYPE	DESCRIPTION
A2, E2	A2, B1, B9, D1, D9	NC	–	No Connect: These pins should be left unconnected.
	D1, D9, B1, B9	NF	-	No Function: These pins are used as DQ4-DQ7 on the 32 Meg x 8, but are NF (No Function) on the 16 Meg x 16 configuration.
A8, E8	A2, A8	NU	–	Not Used: If EMR[E10] = 0, A8 and E8 are UDQS# and LDQS#. If EMR[E10] = 1, then A8 and E8 are Not Used.
L1, R3, R7, R8	G1, L3, L7, L8	RFU	–	Reserved for Future Use; Bank address bit BA2(L1) for 1Gb, 2Gb, and 4Gb densities. Row address bits A13(R8), A14(R3) and A15(R7) for higher densities.

Functional Description

The 256Mb DDR2 SDRAM is a high-speed, CMOS dynamic random-access memory containing 268,435,456 bits. The 256Mb DDR2 SDRAM is internally configured as a four-bank DRAM.

The 256Mb DDR2 SDRAM uses a double data rate architecture to achieve high-speed operation. The DDR2 architecture is essentially a 4*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 256Mb DDR2 SDRAM consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

Figure 3: Functional Block Diagram (64 Meg x 4)

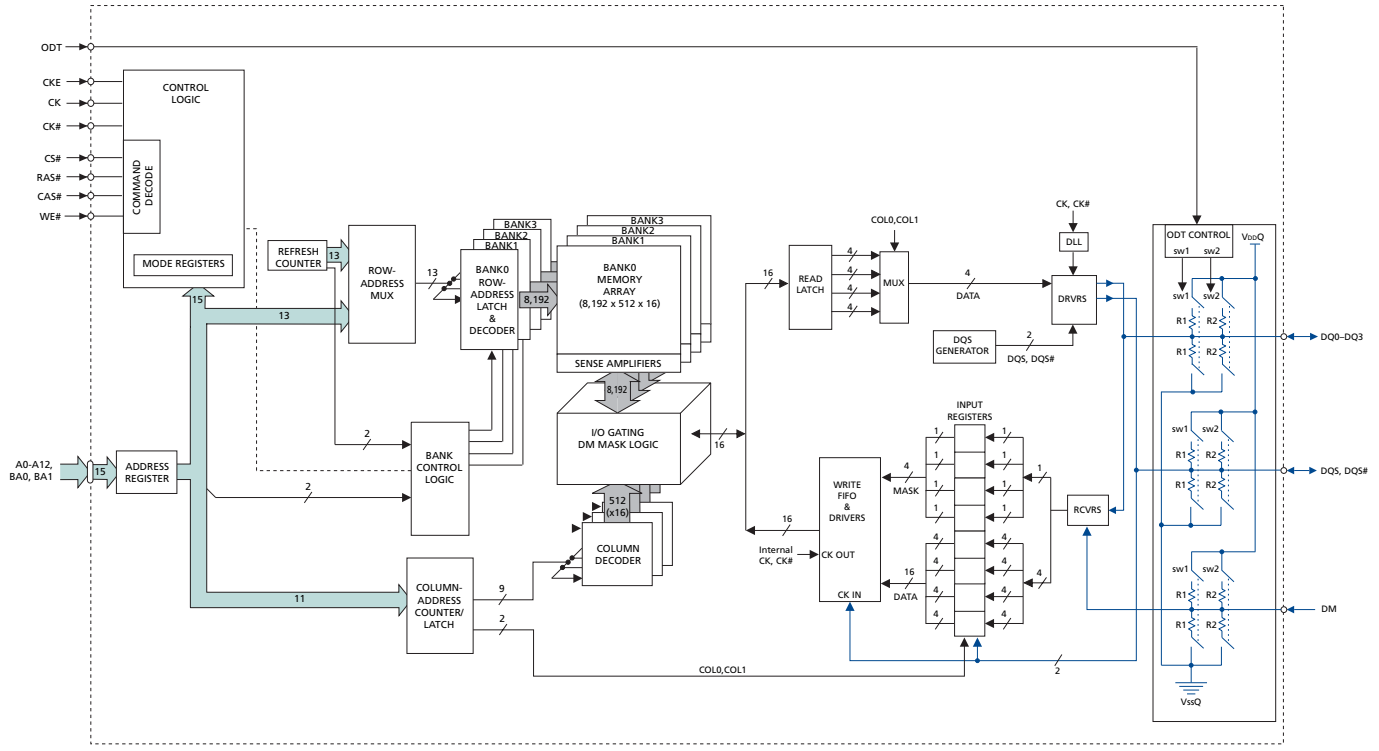


Figure 4: Functional Block Diagram (32 Meg x 8)

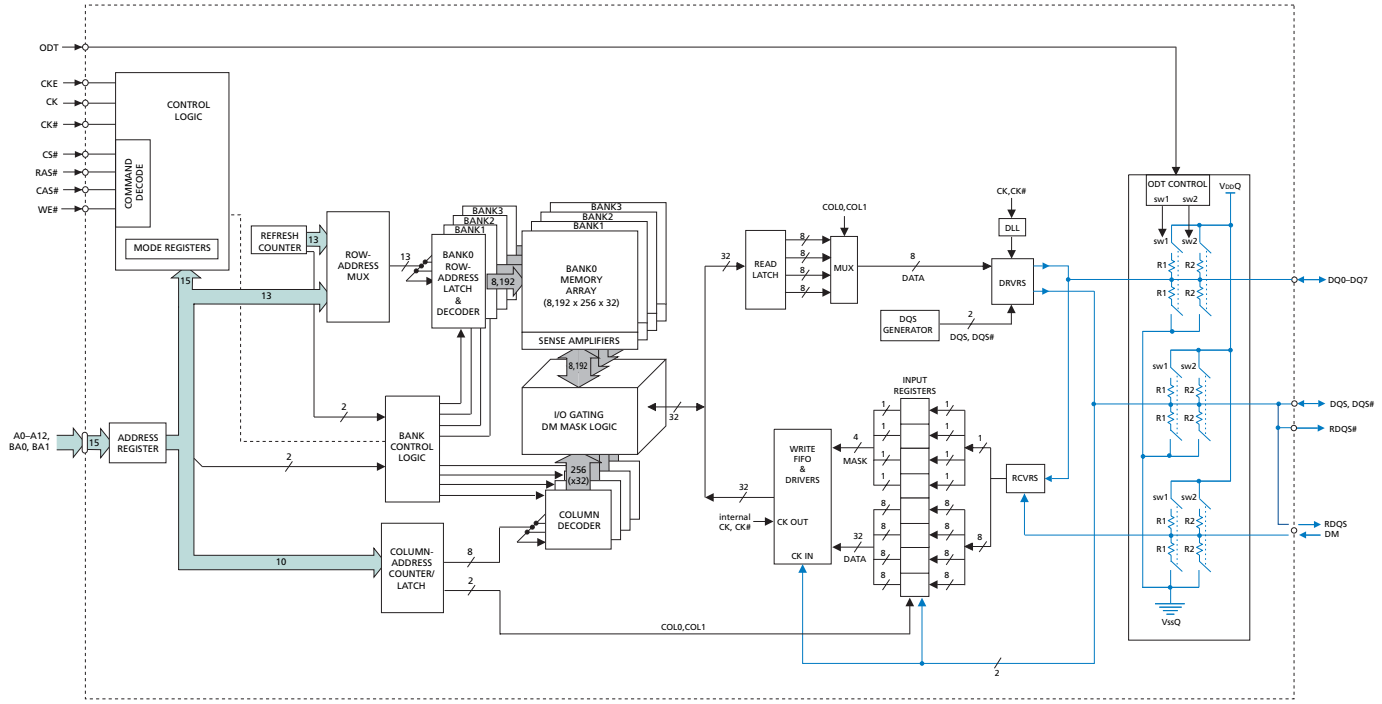
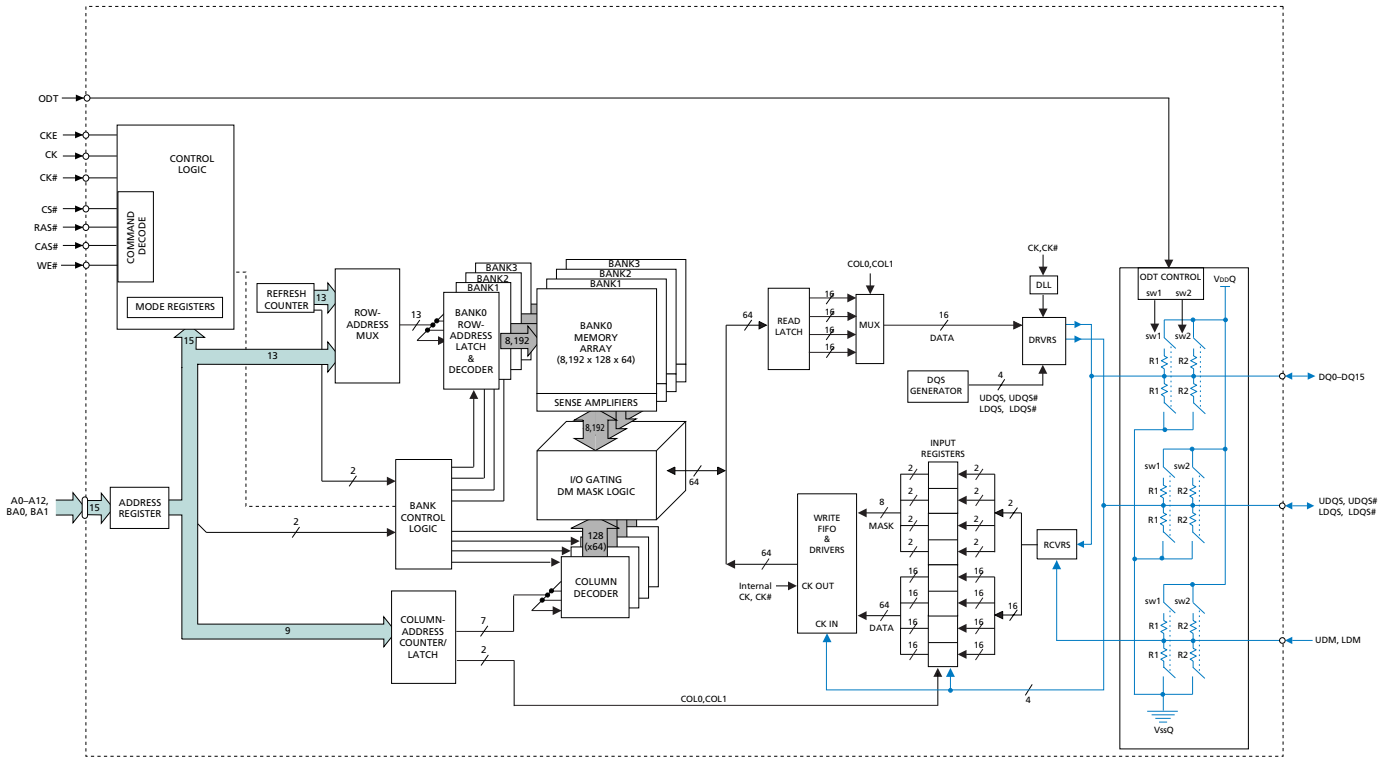


Figure 5: Functional Block Diagram (16 Meg x 16)



Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

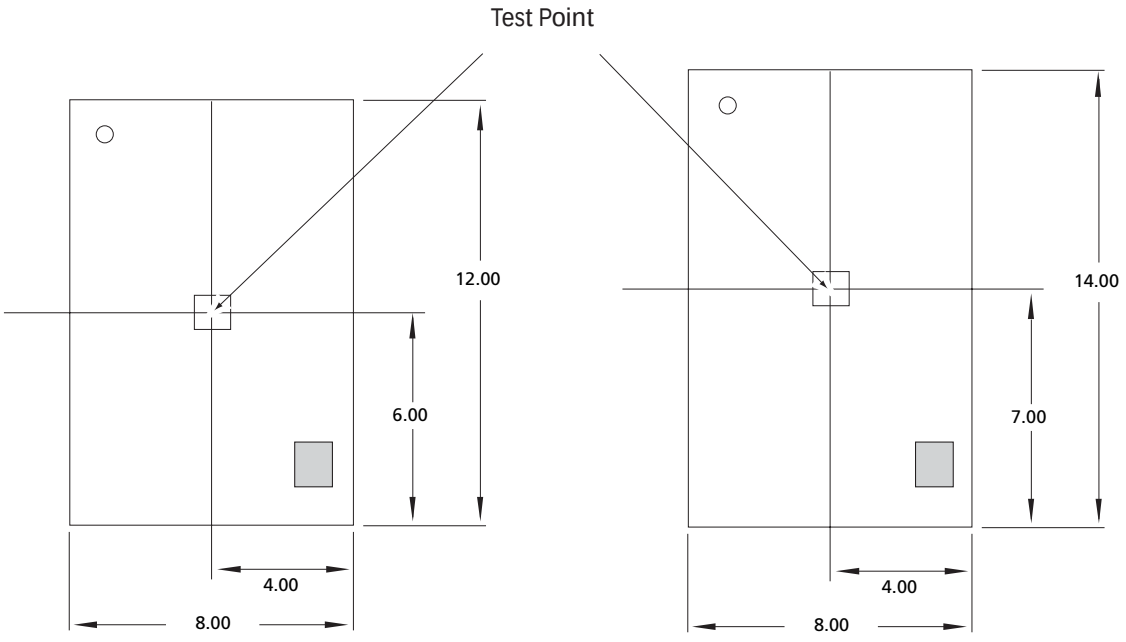
Table 3: Absolute Maximum DC Ratings

Symbol	Parameter	Min	Max	Units
VDD	VDD Supply Voltage Relative to VSS	-1.0	2.3	V
VDDQ	VDDQ Supply Voltage Relative to VSSQ	-0.5	2.3	V
VDDL	VDDL Supply Voltage Relative to VSSL	-0.5	2.3	V
VIN, VOUT	Voltage on any Pin Relative to VSS	-0.5	2.3	V
TSTG	Storage Temperature (T_{case})[1]	-55	100	°C
T_C	Operating Temperature (T_{case})[1, 2]	0	70	°C
I_I	Input Leakage Current Any input 0V ≤ VIN ≤ VDD (All other pins not under test = 0V)	-5	5	µA
I_{OZ}	Output Leakage Current 0V ≤ VOUT ≤ VDDQ DQs and ODT are disabled	-5	5	µA
I_{VREF}	VREF Leakage Current VREF = Valid VREF level	-2	2	µA

NOTE:

1. MAX operating case temperature; T_C is measured in the center of the package illustrated in Figure 6.
2. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.

Figure 6: Example Temperature Test Point Location



8mm x 12mm "FI" FBGA

8mm x 14mm "FP" FBGA

AC and DC Operating Conditions

Table 4: Recommended DC Operating Conditions (SSTL_18)

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Nom	Max	Units	Notes
Supply Voltage	V_{DD}	1.7	1.8	1.9	V	1, 5
V_{DD}L Supply Voltage	V_{DD}L	1.7	1.8	1.9	V	4, 5
I/O Supply Voltage	V_{DD}Q	1.7	1.8	1.9	V	4, 5
I/O Reference Voltage	$V_{REF(DC)}$	0.49 x V_{DD}Q	0.50 x V_{DD}Q	0.51 x V_{DD}Q	V	2
I/O Termination Voltage (system)	V_{TT}	$V_{REF(DC)}$ - 40	$V_{REF(DC)}$	$V_{REF(DC)}$ + 40	mV	3

NOTE:

1. V_{DD} and V_{DD}Q must track each other. V_{DD}Q must be less than or equal to V_{DD}.
2. V_{REF} is expected to equal V_{DD}Q/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±1% of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed ±2 percent of $V_{REF(DC)}$. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
4. V_{DD}Q tracks with V_{DD}; V_{DD}L tracks with V_{DD}.
5. VssQ = VssL = Vss

Table 5: ODT DC Electrical Characteristics

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Nom	Max	Units	Notes
R_{TT} effective impedance value for 75Ω setting EMR (A6, A2) = 0, 1	$R_{TT1(EFF)}$	60	75	90	Ω	1
R_{TT} effective impedance value for 150Ω setting EMR (A6, A2) = 1, 0	$R_{TT2(EFF)}$	120	150	180	Ω	1
Deviation of VM with respect to V_{DD}Q/2	ΔVM	-6%		6%	%	2

NOTE:

1. $R_{TT1(EFF)}$ and $R_{TT2(EFF)}$ are determined by applying $V_{IH(AC)}$ and $V_{IL(AC)}$ to pin under test separately, then measure current $I(V_{IH(AC)})$ and $I(V_{IL(AC)})$ respectively.

$$R_{TT(EFF)} = \frac{V_{IH(AC)} - V_{IL(AC)}}{I(V_{IH(AC)}) - I(V_{IL(AC)})}$$

2. Measure voltage (VM) at tested pin with no load.

$$\Delta VM = \left(\frac{2 \times VM}{V_{DD}Q} - 1\right) \times 100\%$$

Input Electrical Characteristics and Operating Conditions

Table 6: Input DC Logic Levels

All voltages referenced to V_{SS}

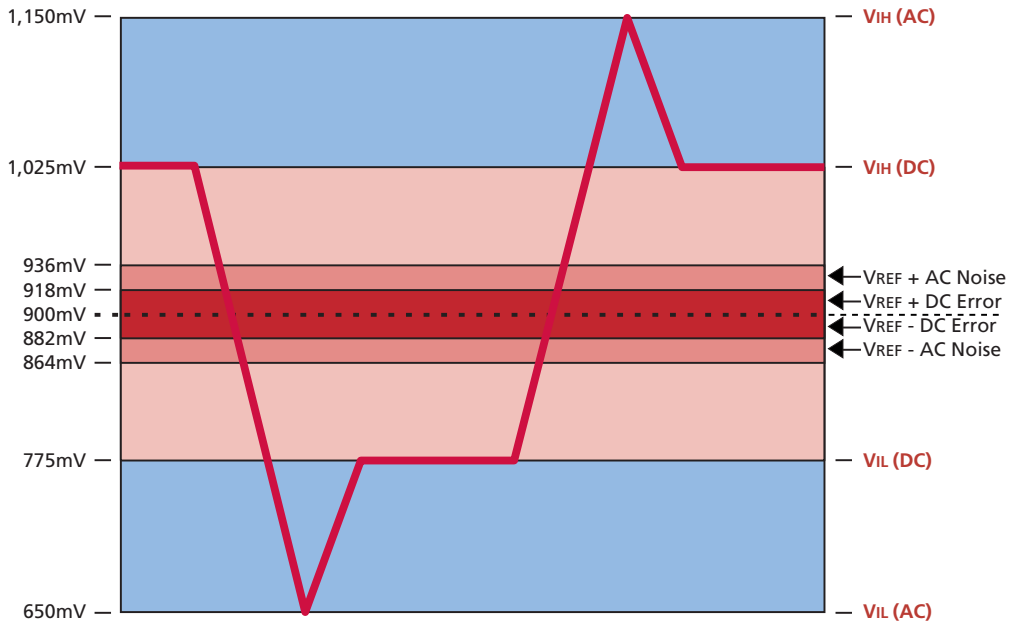
Parameter	Symbol	Min	Max	Units	Notes
Input High (Logic 1) Voltage	V_{IH}(DC)	V_{REF}(DC) + 125	V_{DDQ} + 300	mV	
Input Low (Logic 0) Voltage	V_{IL}(DC)	-300	V_{REF}(DC) - 125	mV	

Table 7: Input AC Logic Levels

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units	Notes
Input High (Logic 1) Voltage	V_{IH}(AC)	V_{REF}(DC) + 250	-	mV	
Input Low (Logic 0) Voltage	V_{IL}(AC)	–	V_{REF}(DC) - 250	mV	

Figure 7: Single-Ended Input Signal Levels



NOTE:

Numbers in diagram reflect nomimal values.

Table 8: Differential Input Logic Levels

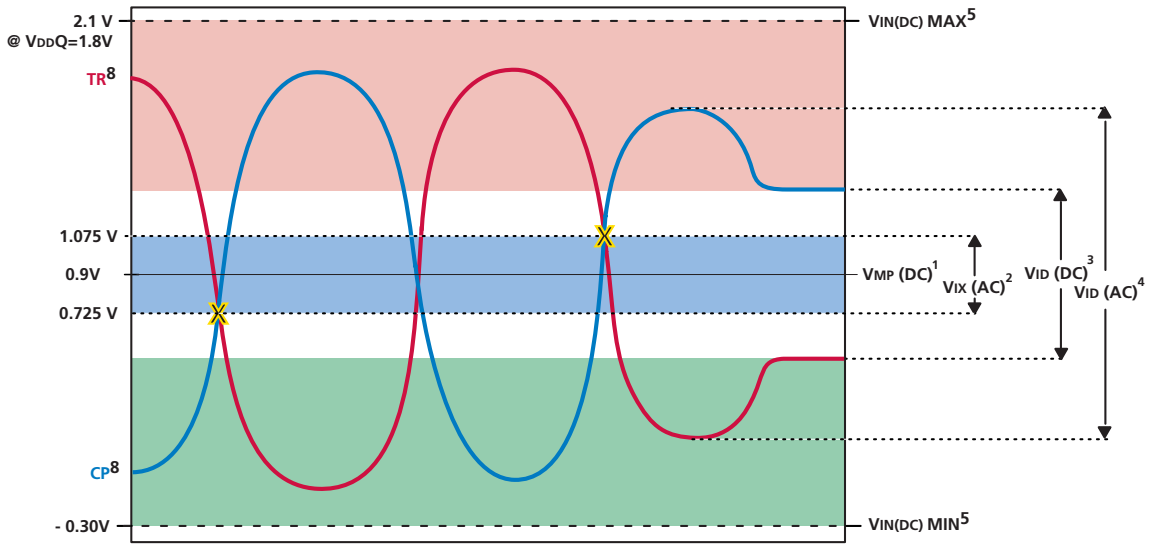
All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units	Notes
DC Input Signal Voltage	V_{IN}(DC)	-300	V_{DDQ} + 300	mV	1
DC Differential Input Voltage	V_{ID}(DC)	250	V_{DDQ} + 600	mV	2
AC Differential Input Voltage	V_{ID}(AC)	500	V_{DDQ} + 600	mV	3
AC Differential Cross-Point Voltage	V_{IX}(AC)	0.50 x V_{DDQ} - 175	0.50 x V_{DDQ} + 175	mV	4
Input Midpoint Voltage	V_{MP}(DC)	850	950	mV	5

NOTE:

1. V_{IN} (DC) specifies the allowable DC execution of each input of differential pair such as CK, CK#, DQS, DQS#, LDQS, LDQS#, UDQS, UDQS#, and RDQS, RDQS#.
2. V_{ID} (DC) specifies the input differential voltage | V_{TR} - V_{CP} | required for switching, where V_{TR} is the true input (such as CK, DQS, LDQS, UDQS, RDQS) level and V_{CP} is the complementary input (such as CK#, DQS#, LDQS#, UDQS#, RDQS#). The minimum value is equal to V_{IH}(DC) - V_{IL}(DC). Differential input signal levels are shown in Figure 8.
3. V_{ID}(AC) specifies the input differential voltage | V_{TR} - V_{CP} | required for switching, where V_{TR} is the true input (such as CK, DQS, LDQS, UDQS, RDQS) level and V_{CP} is the complementary input (such as CK#, DQS#, LDQS#, UDQS#, RDQS#). The minimum value is equal to V_{IH}(AC) - V_{IL}(AC) from Table 7 on page 14.
4. The typical value of V_{IX} (AC) is expected to be about 0.5 x V_{DDQ} of the transmitting device and V_{IX}(AC) is expected to track variations in V_{DDQ}. V_{IX}(AC) indicates the voltage at which differential input signals must cross as shown in Figure 8.
5. V_{MP}(DC) specifies the input differential common mode voltage (V_{TR} + V_{CP})/2 where V_{TR} is the true input (CK, DQS) level and V_{CP} is the complementary input (CK#, DQS#). V_{MP}(DC) is expected to be about 0.5*V_{DDQ}.

Figure 8: Differential Input Signal Levels



NOTE:

1. This provides a minimum of 850mV to a maximum of 950mV and is expected to be V_{DDQ}/2.
2. TR and CP must cross in this region.
3. TR and CP must meet at least V_{ID}(DC) min when static and is centered around V_{MP}(DC).
4. TR and CP must have a minimum 500mV peak-to-peak swing.
5. TR and CP may not be more positive than V_{DDQ} + 0.3V or more negative than V_{SS} - 0.3V.
6. For AC operation, all DC clock requirements must also be satisfied.
7. Numbers in diagram reflect nominal values.
8. TR represents the CK, DQS, RDQS, LDQS and UDQS signals; CP represents CK#, DQS#, RDQS#, LDQS# and UDQS# signals.

Table 9: AC Input Test Conditions

Parameter	Symbol	Min	Max	Units	Notes
Input setup timing measurement reference level BA1-BA0, A0-A12, CS#, RAS#, CAS#, WE#, ODT, DM, UDM, LDM and CKE	V_{RS}	See Note 2			1, 2,
Input hold timing measurement reference level BA1-BA0, A0-A12, CS#, RAS#, CAS#, WE#, ODT, DM, UDM, LDM and CKE	V_{RH}	See Note3			1, 3,
Input timing measurement reference level (single-ended) DQS for x4x8; UDQS, LDQS for x16	$V_{REF(DC)}$	$V_{DD}Q*0.49$	$V_{DD}Q*0.51$	V	1, 4
Input timing measurement reference level (differential) CK, CK# for x4,x8,x16 DQS, DQS# for x4,x8; RDQS, RDQS# for x8 UDQS, UDQS#, LDQS, LDQS# for x16	V_{RD}	$V_{IX(AC)}$		V	1, 5, 6

NOTE:

1. All voltages referenced to V_{SS}.
2. Input waveform setup timing ($^{t}IS_b$) is referenced from the input signal crossing at the $V_{IH(AC)}$ level for a rising signal and $V_{IL(DC)}$ for a falling signal applied to the device under test as shown in Figure 17.
3. Input waveform hold ($^{t}IH_b$) timing is referenced from the input signal crossing at the $V_{IL(DC)}$ level for a rising signal and $V_{IH(DC)}$ for a falling signal applied to the device under test as shown in Figure 17
4. Input waveform setup timing (^{t}DS) and hold timing (^{t}DH) for single-ended data strobe is referenced from the crossing of DQS, UDQS, or LDQS through the V_{REF} level applied to the device under test as shown in Figure 19.
5. Input waveform setup timing (^{t}DS) and hold timing (^{t}DH) when differential data strobe is enabled is referenced from the crosspoint of DQS,DQS# or UDQS,UDQS# or LDQS,LDQS# as shown in Figure 18.
6. Input waveform timing is referenced to the crossing point level (V_{IX}) of two input signals (V_{TR} and V_{CP}) applied to the device under test, where V_{TR} is the "true" input signal and V_{CP} is the "complementary" input signal shown in Figure 20.
7. See "Input Slew Rate Derating" on page 17.

Input Slew Rate Derating

For all input signals the total ^{t}IS (setup time) and ^{t}IH (hold time) required is calculated by adding the data sheet ^{t}IS(base) and ^{t}IH(base) value to the Δ^{t}IS and Δ^{t}IH derating value respectively. Example: ^{t}IS (total setup time) = ^{t}IS(base) + Δ^{t}IS

Setup (^{t}IS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC)min. Setup (^{t}IS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC)MAX. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(DC) to AC region', use nominal slew rate for derating value (Figure 9 on page 18) If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(DC) to ac region', the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value (Figure 10 on page 18)

Hold (^{t}IH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)MAX and the first crossing of VREF(DC). Hold (^{t}IH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)MIN and the first crossing of VREF(DC). If the actual signal is always later than the nominal slew rate line between shaded 'dc to VREF(DC) region', use nominal slew rate for derating value (Figure 11 on page 19) If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(DC) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(DC) level is used for derating value (Figure 12 on page 19)

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(AC) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(AC)).

For slew rates in between the values listed in Table 10, the derating values may obtained by linear interpolation.

Table 10: Setup and Hold Time Derating Values

		CK,CK# Differential Slew Rate						
		2.0 V/ns		1.5 V/ns		1.0 V/ns		
		Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Units
Command/ Address Slew rate (V/ns)	4.0	+187	+94	+217	+124	+247	+154	ps
	3.5	+179	+89	+209	+119	+239	+149	ps
	3.0	+167	+83	+197	+113	+227	+143	ps
	2.5	+150	+75	+180	+105	+210	+135	ps
	2.0	+125	+45	+155	+75	+185	+105	ps
	1.5	+83	+21	+113	+51	+143	+81	ps
	1.0	0	0	+30	+30	+60	+60	ps
	0.9	-11	-14	+19	+16	+49	+46	ps
	0.8	-25	-31	+5	-1	+35	+29	ps
	0.7	-43	-54	-13	-24	+17	+6	ps
	0.6	-67	-83	-37	-53	-7	-23	ps
	0.5	-110	-125	-80	-95	-50	-65	ps
	0.4	-175	-188	-145	-158	-115	-128	ps
	0.3	-285	-292	-255	-262	-225	-232	ps
	0.25	-350	-375	-320	-345	-290	-315	ps
	0.2	-525	-500	-495	-470	-465	-440	ps
	0.15	-800	-708	-770	-678	-740	-648	ps
	0.1	-1450	-1125	-1420	-1095	-1390	-1065	ps

Figure 9: Nominal Slew Rate for tIS

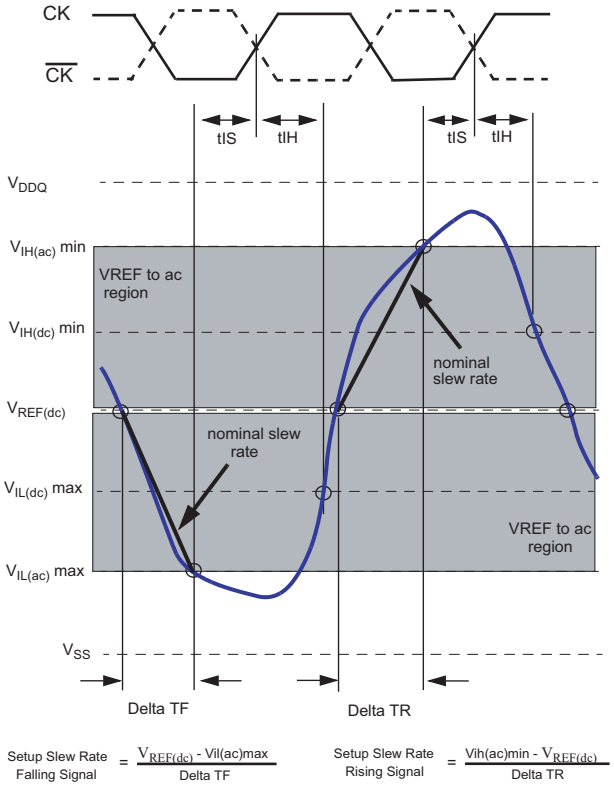


Figure 10: Tangent Line for tIS

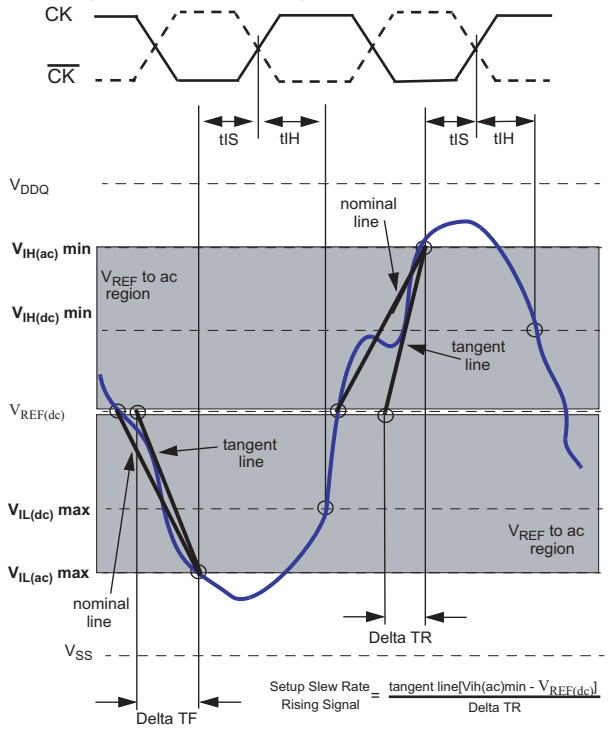


Figure 11: Nominal Slew Rate for ^{t}IH

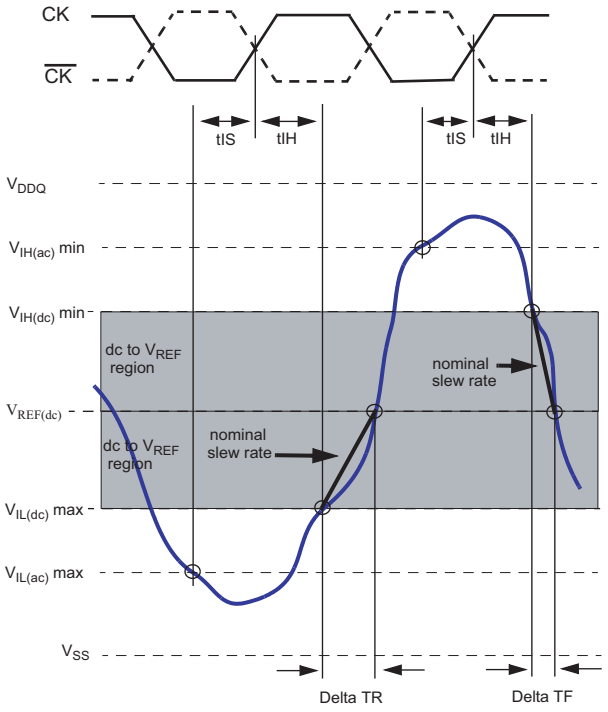
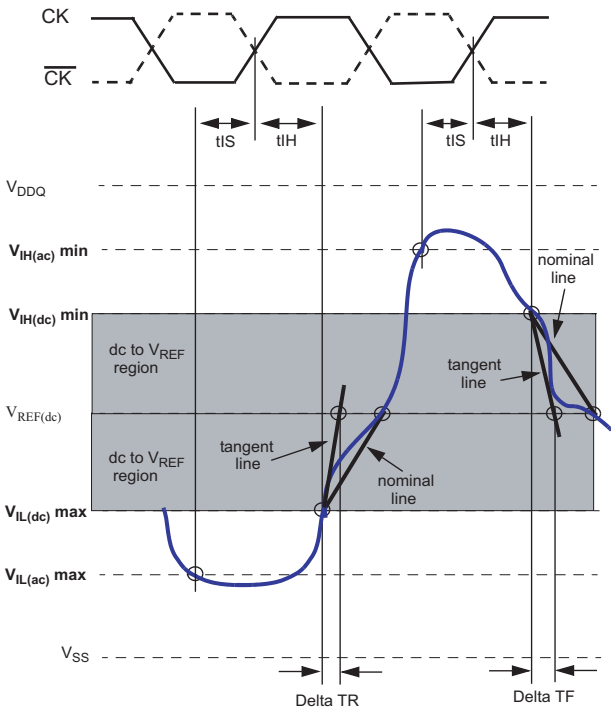


Figure 12: Tangent Line for ^{t}IH



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line [} V_{REF(dc)} \text{ - Vil(dc)max]}}{\text{Delta TR}}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line [Vih(dc)min - } V_{REF(dc)} \text{]}}{\text{Delta TF}}$$

Data Slew Rating

Table 11: ^{t}DS, ^{t}DH Derating Values

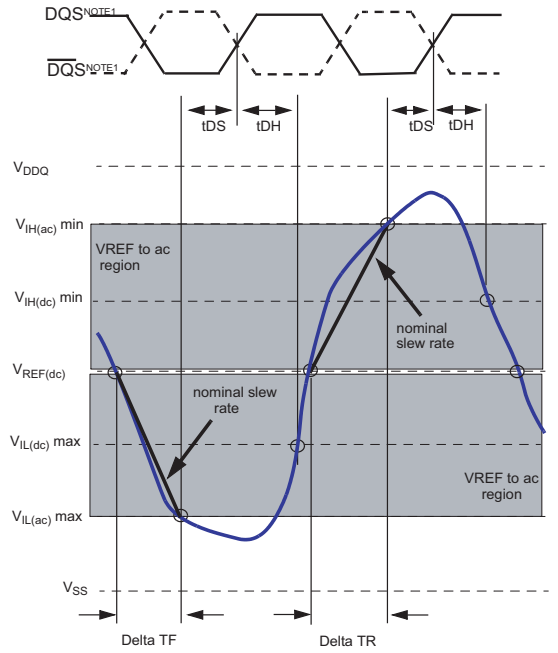
Note 1; all units in ps

		DQS,DQS# Differential Slew Rate																	
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns		0.8V/ns	
		Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH
DQ Slew rate V/ns	2.0	125	45	125	45	125	45	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	83	21	83	21	83	21	95	33	-	-	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
	0.9	-	-	-11	-14	-11	-14	1	-2	13	10	25	22	-	-	-	-	-	-
	0.8	-	-	-	-	-25	-31	-13	-19	-1	-7	11	5	23	17	-	-	-	-
	0.7	-	-	-	-	-	-	-31	-42	-19	-30	-7	-18	5	-6	17	6	-	-
	0.6	-	-	-	-	-	-	-	-	-43	-59	-31	-47	-19	-35	-7	-23	5	-11
	0.5	-	-	-	-	-	-	-	-	-	-	-74	-89	-62	-77	-50	-65	-38	-53
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-127	-140	-115	-128	-103	-116

NOTE:

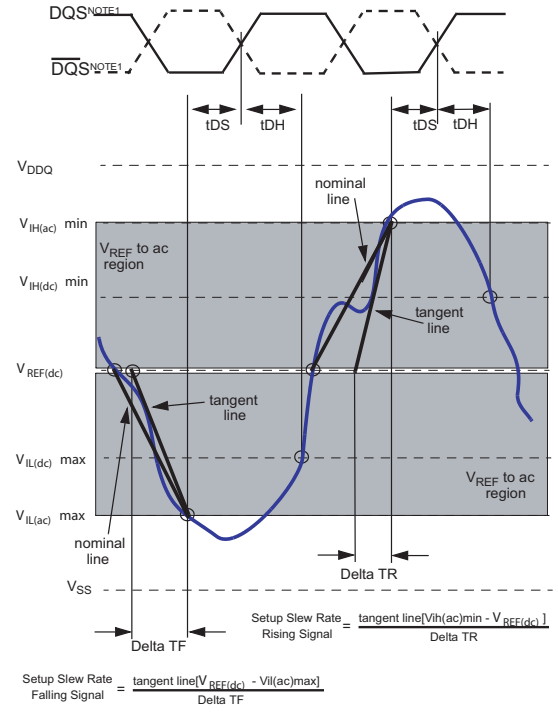
1. For all input signals the total ^{t}DS (setup time) and ^{t}DH (hold time) required is calculated by adding the datasheet value to the derating value listed in Table 11.
2. Setup (^{t}DS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of Vih(ac)min. Setup (^{t}DS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value (see Figure 13) If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 14)
3. Hold (^{t}DH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of $V_{REF(dc)}$. Hold (^{t}DH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of $V_{REF(dc)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region', use nominal slew rate for derating value (see Figure 15) If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 16)
4. Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL}$(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}$(ac).
5. For slew rates in between the values listed in Table 11, the derating values may obtained by linear interpolation.
6. These values are typically not subject to production test. They are verified by design and characterization.

Figure 13: Nominal Slew Rate for tDS



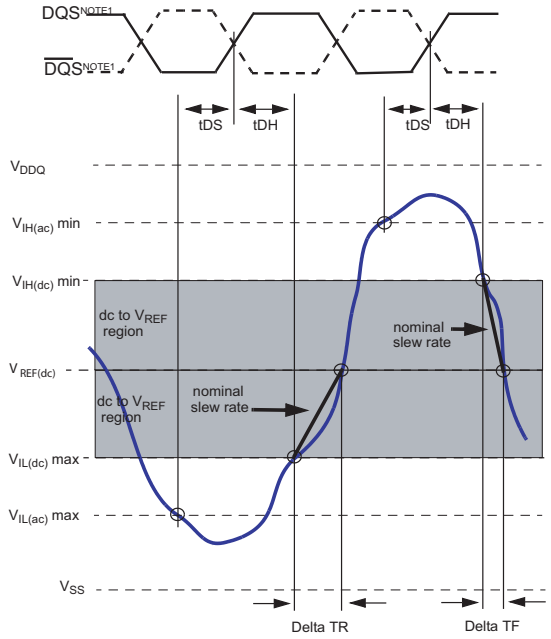
NOTE1 DQS, DQS# signals must be monotonic between Vil(dc)max and Vih(dc)min.

Figure 14: Tangent Line for tDS



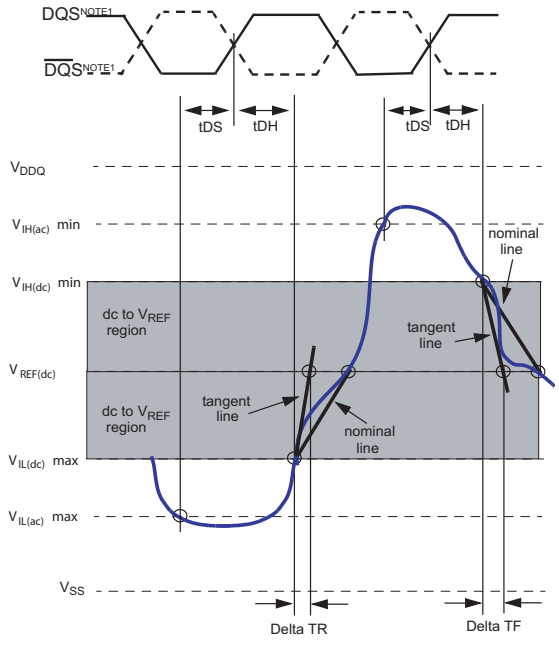
NOTE1 DQS, DQS# signals must be monotonic between Vil(dc)max and Vih(dc)min.

Figure 15: Nominal Slew Rate for tDH



NOTE1 DQS, DQS# signals must be monotonic between Vil(dc)max and Vih(dc)min.

Figure 16: Tangent Line for tDH



NOTE1 DQS, DQS# signals must be monotonic between Vil(dc)max and Vih(dc)min.

Figure 17: AC Input Test Signal Waveform Command/Address pins

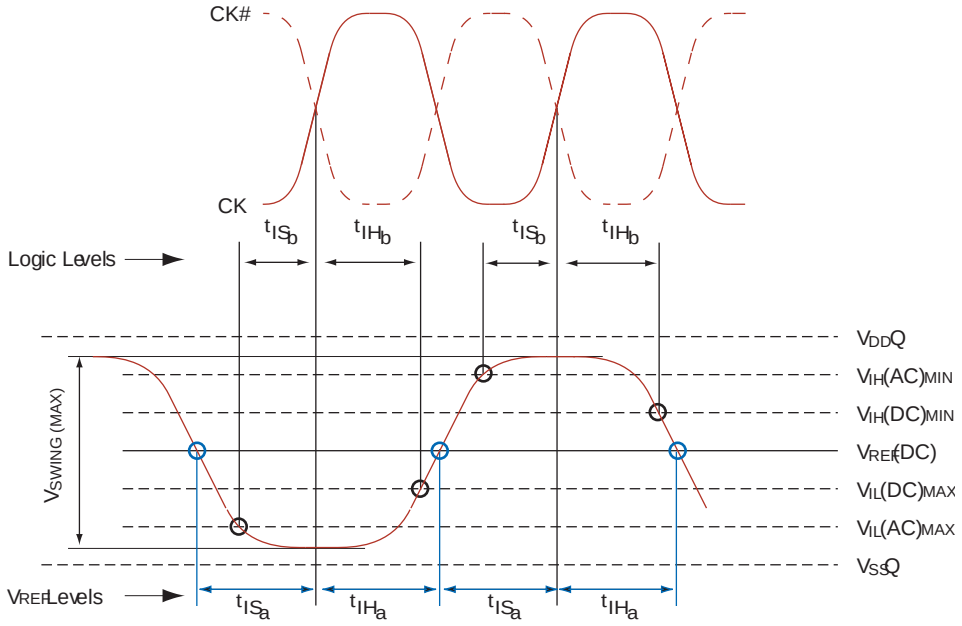


Figure 18: AC Input Test Signal Waveform for Data with DQS,DQS# (differential)

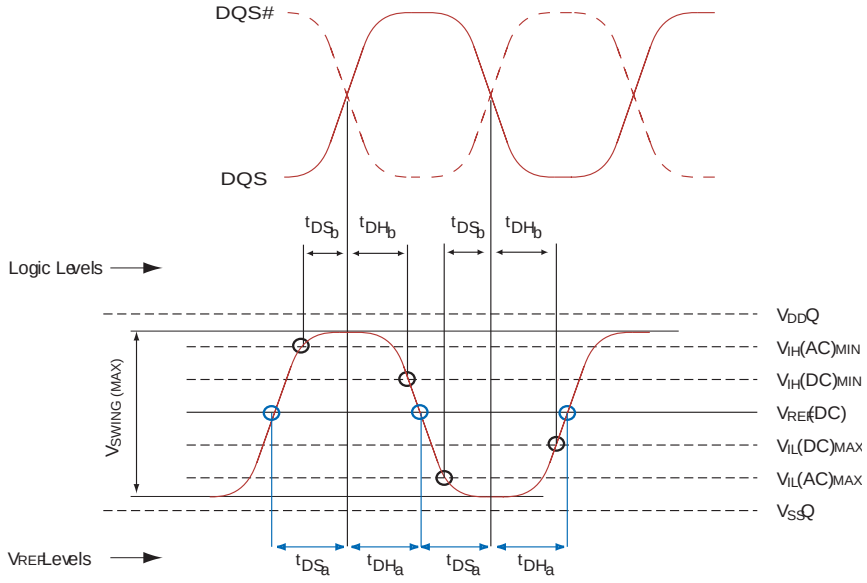


Figure 19: AC Input Test Signal Waveform for Data with DQS (single-ended)

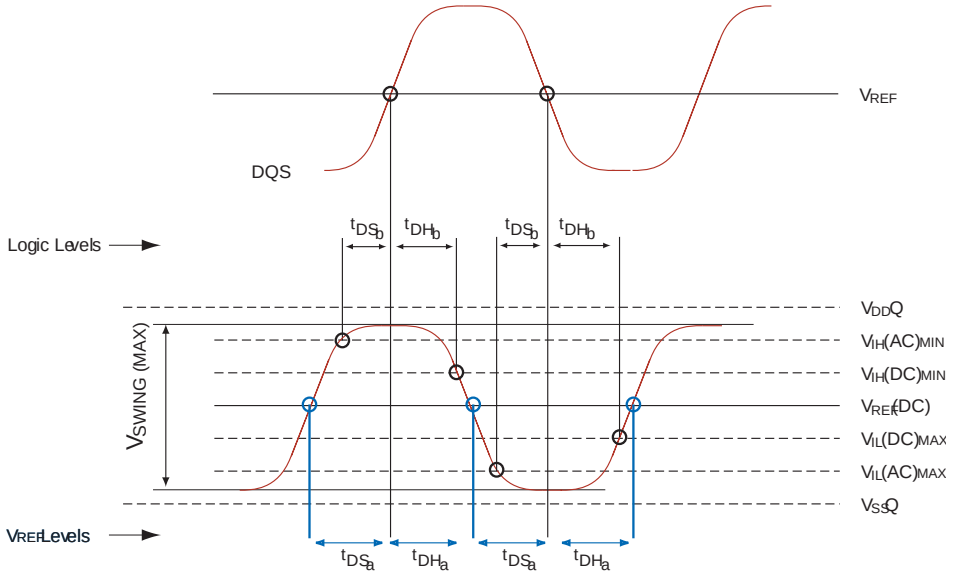
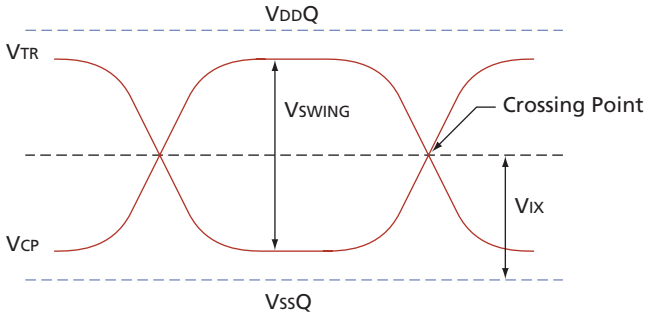


Figure 20: AC Input Test Signal Waveform (differential)



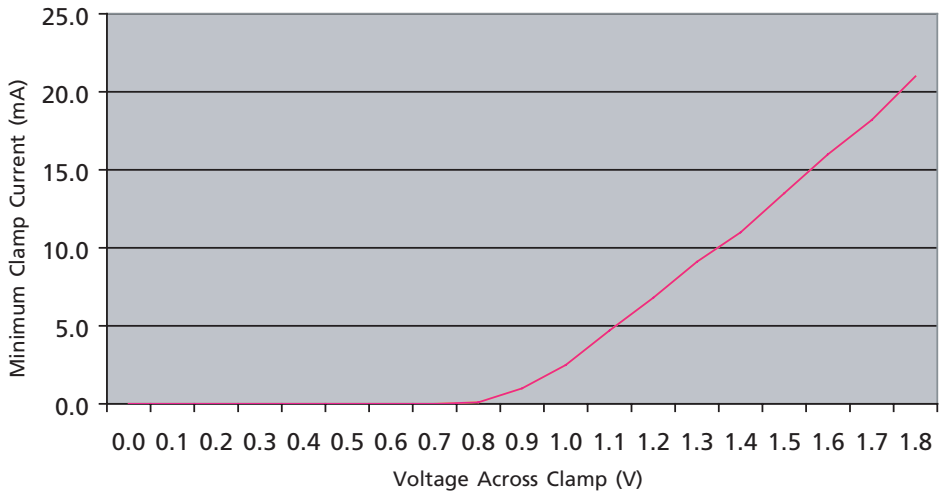
Power and Ground Clamp Characteristics

Power and ground clamps are provided on the following input-only pins: BA1-BA0, A0-A12, CS#, RAS#, CAS#, WE#, ODT, and CKE.

Table 12: Input Clamp Characteristics

Voltage Across Clamp (V)	Minimum Power Clamp Current (mA)	Minimum Ground Clamp Current (mA)
0.0	0.0	0.0
0.1	0.0	0.0
0.2	0.0	0.0
0.3	0.0	0.0
0.4	0.0	0.0
0.5	0.0	0.0
0.6	0.0	0.0
0.7	0.0	0.0
0.8	0.1	0.1
0.9	1.0	1.0
1.0	2.5	2.5
1.1	4.7	4.7
1.2	6.8	6.8
1.3	9.1	9.1
1.4	11.0	11.0
1.5	13.5	13.5
1.6	16.0	16.0
1.7	18.2	18.2
1.8	21.0	21.0

Figure 21: Input Clamp Characteristics



AC Overshoot/Undershoot Specification

Table 13: Address and Control Pins

Applies to BA1-BA0, A0-A12, CS#, RAS#, CAS#, WE#, CKE, ODT

Parameter	Specification	
	-3	-37E
Maximum peak amplitude allowed for overshoot area (See Figure 22)	0.9V	0.9V
Maximum peak amplitude allowed for undershoot area (See Figure 23)	0.9V	0.9V
Maximum overshoot area above V_{DD} (See Figure 22)	0.75V-ns	0.56V-ns
Maximum undershoot area below V_{SS} (See Figure 23)	0.75V-ns	0.56V-ns

Table 14: Clock, Data, Strobe, and Mask Pins

Applies to DQ0–DQxx, DQS, DQS#, RDQS, RDQS#, UDQS, UDQS#, LDQS, LDQS#, DM, UDM, LDM

Parameter	Specification	
	-3	-37E
Maximum peak amplitude allowed for overshoot area (See Figure 22)	0.9V	0.9V
Maximum peak amplitude allowed for undershoot area (See Figure 22)	0.9V	0.9V
Maximum overshoot area above V_{DDQ} (See Figure 22)	0.38V-ns	0.28V-ns
Maximum undershoot area below V_{SSQ} (See Figure 23)	0.38V-ns	0.28V-ns

Figure 22: Overshoot

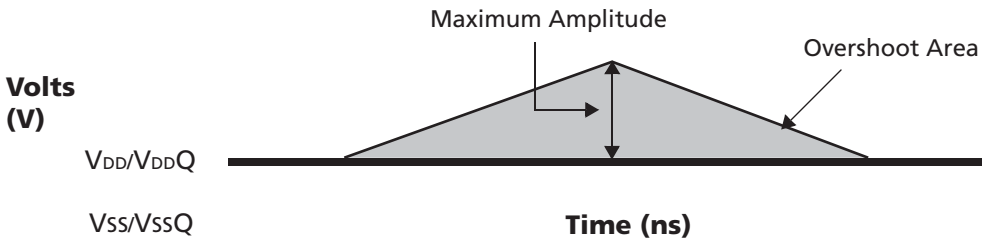
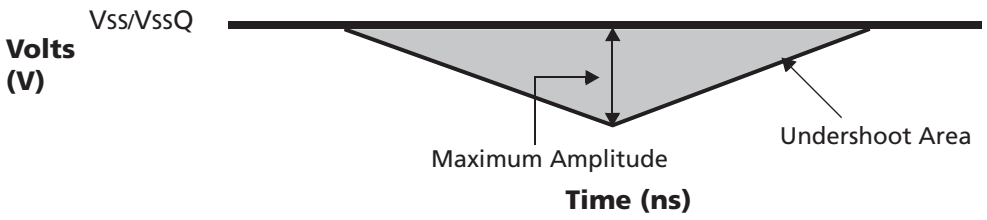


Figure 23: Undershoot



Output Electrical Characteristics and Operating Conditions

Table 15: Differential AC Output Parameters

Parameter	Symbol	Min	Max	Units	Notes
AC Differential Cross-Point Voltage	$V_{OX}(AC)$	0.50 x $V_{DD}Q$ - 125	0.50 x $V_{DD}Q$ + 125	mV	1
AC Differential Voltage Swing	V_{SWING}	1.0		mV	

NOTE:

1. The typical value of $V_{OX}(AC)$ is expected to be about 0.5 x $V_{DD}Q$ of the transmitting device and V_{OX} (AC) is expected to track variations in $V_{DD}Q$. $V_{OX}(AC)$ indicates the voltage at which differential output signals must cross.

Figure 24: Differential Output Signal Levels

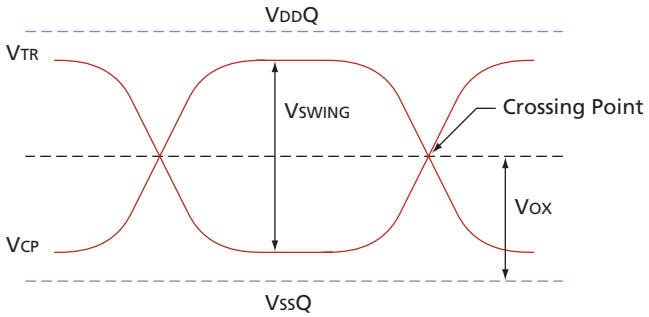


Table 16: Output DC Current Drive

Parameter	Symbol	Value	Units	Notes
Output Minimum Source DC Current	I_{OH}	-13.4	mA	1,3,4
Output Minimum Sink DC Current	I_{OL}	13.4	mA	2,3,4

NOTE:

1. For I_{OH} (DC); $V_{DD}Q$ = 1.7V, V_{OUT} = 1420mV. (V_{OUT} - $V_{DD}Q$)/I_{OH} must be less than 21Ω for values of V_{OUT} between $V_{DD}Q$ and $V_{DD}Q$ - 280mV.
2. For I_{OL} (DC); $V_{DD}Q$ = 1.7V, V_{OUT} = 280mV. V_{OUT}/I_{OL} must be less than 21Ω for values of V_{OUT} between 0V and 280mV.
3. The DC value of V_{REF} applied to the receiving device is set to V_{TT}.
4. The values of I_{OH} (DC) and I_{OL} (DC) are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} (MIN) plus a noise margin and V_{IL} (MAX) minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (See output IV curves) along a 21Ω load line to define a convenient driver current for measurement.

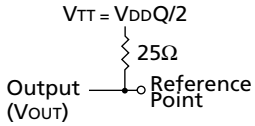
Table 17: Output Characteristics

Parameter	Symbol	Min	Nom	Max	Units	Notes
Output impedance		12.6	18	23.4	Ωs	1,2
Pull-up and Pull-down mismatch		0		4	Ωs	1,2,3
Output slew rate		1.5		5	V/ns	1,4,5

NOTE:

1. Absolute specifications: 0°C ≤ T_{case} ≤ +85°C; $V_{DD}Q$ = +1.8V ±0.1V, V_{DD} = +1.8V ±0.1V.
2. Impedance measurement condition for output source DC current: $V_{DD}Q$ = 1.7V; V_{OUT} = 1420mV; (V_{OUT} - $V_{DD}Q$)/I_{OH} must be less than 23.4Ω for values of V_{OUT} between $V_{DD}Q$ and $V_{DD}Q$ - 280mV. Impedance measurement condition for output sink DC current: $V_{DD}Q$ = 1.7V; V_{OUT} = 280mV; V_{OUT}/I_{OL} must be less than 23.4Ω for values of V_{OUT} between 0V and 280mV.
3. Mismatch is absolute value between pull-up and pull-down, both are measured at same temperature and voltage.
4. Output slew rate for falling and rising edges is measured between V_{TT} - 250mV and V_{TT} + 250mV for single ended signals. For differential signals (e.g. DQS - DQS#) output slew rate is measured between DQS - DQS# = -500mV and DQS# - DQS = +500mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.
5. The absolute value of the slew rate as measured from V_{IL} (DC)MAX to V_{IH} (DC) MIN is equal to or greater than the slew rate as measured from V_{IL} (AC) MAX to V_{IH} (AC) MIN. This is guaranteed by design and characterization.

Figure 25: Output Slew Rate Load



Full Strength Pull-Down Driver Characteristics

Figure 26: Full Strength Pull-Down Characteristics

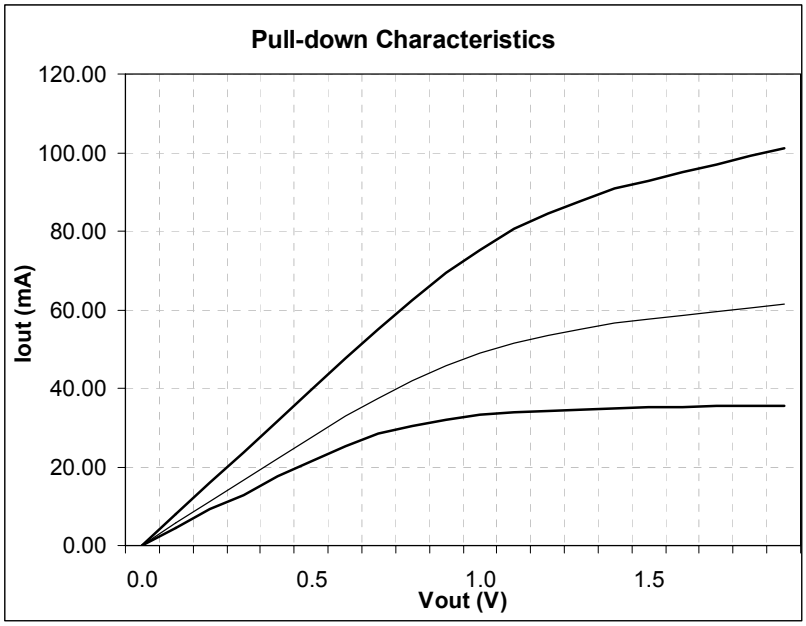


Table 18: Pulldown Current (mA)

Voltage (V)	Minimum	Nominal	Maximum
0.0	0.00	0.00	0.00
0.1	4.3	5.63	7.95
0.2	8.6	11.3	15.90
0.3	12.9	16.52	23.85
0.4	16.9	22.19	31.80
0.5	20.4	27.59	39.75
0.6	23.28	32.39	47.70
0.7	25.44	36.45	55.55
0.8	26.79	40.38	62.95
0.9	27.67	44.01	69.55
1.0	28.38	47.01	75.35
1.1	28.96	49.63	80.35
1.2	29.46	51.71	84.55
1.3	29.90	53.32	87.95
1.4	30.29	54.9	90.70
1.5	30.65	56.03	93.00
1.6	30.98	57.07	95.05
1.7	31.31	58.16	97.05
1.8	31.64	59.27	99.05
1.9	31.96	60.35	101.05

Full Strength Pull-Up Driver Characteristics

Figure 27: Full Strength Pull-up Characteristics

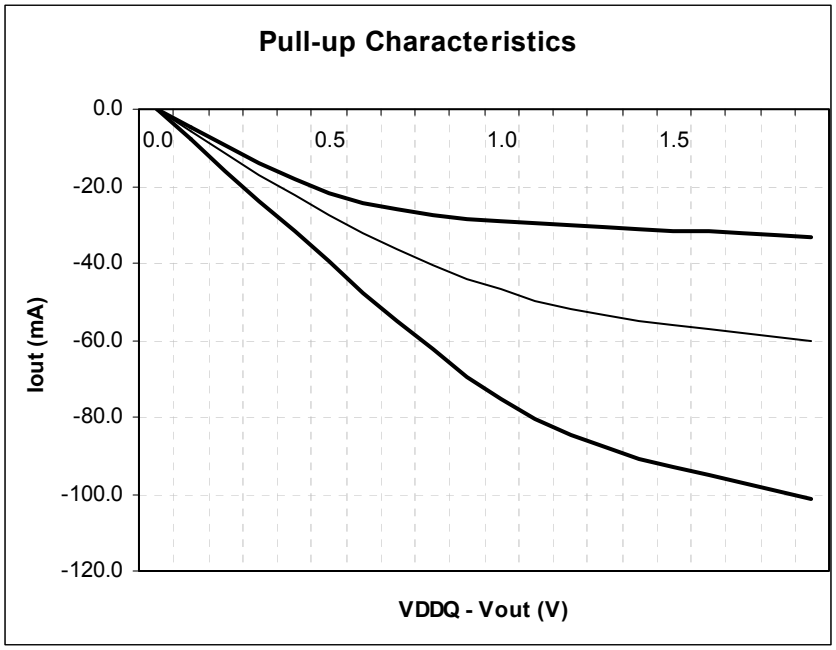


Table 19: Pull-Up Current (mA)

Voltage (V)	Minimum	Nominal	Maximum
0.0	0.00	0.00	-0.00
0.1	-4.3	-5.63	-7.95
0.2	-8.6	-11.3	-15.90
0.3	-12.9	-16.52	-23.85
0.4	-16.9	-22.19	-31.80
0.5	-20.4	-27.59	-39.75
0.6	-23.28	-32.39	-47.70
0.7	-25.44	-36.45	-55.55
0.8	-26.79	-40.38	-62.95
0.9	-27.67	-44.01	-69.55
1.0	-28.38	-47.01	-75.35
1.1	-28.96	-49.63	-80.35
1.2	-29.46	-51.71	-84.55
1.3	-29.90	-53.32	-87.95
1.4	-30.29	-54.90	-90.70
1.5	-30.65	-56.03	-93.00
1.6	-30.98	-57.07	-95.05
1.7	-31.31	-58.16	-97.05
1.8	-31.64	-59.27	-99.05
1.9	-31.96	-60.35	-101.05

FBGA Package Capacitance

Table 20: Input Capacitance

Parameter	Symbol	Min	Max	Units	Notes
Input Capacitance: CK, CK#	CCK	1.0	2.0	pF	1
Delta Input Capacitance: CK, CK#	CDCK	–	0.25	pF	2
Input Capacitance: BA1-BA0, A0-A12, CS#, RAS#, CAS#, WE#, CKE, ODT	CI	1.0	2.0	pF	1
Delta Input Capacitance: BA1-BA0, A0-A12, CS#, RAS#, CAS#, WE#, CKE, ODT	CDI	–	0.25	pF	2
Input/Output Capacitance: DQs, DQS, DM, NF	CIO	2.5	4.0	pF	1
Delta Input/Output Capacitance: DQs, DQS, DM, NF	CDIO	–	0.5	pF	3

NOTE:

1. This parameter is sampled. V_{DD} = +1.8V ±0.1V, $V_{DD}Q$ = +1.8V ±0.1V, V_{REF} = V_{SS}, f = 100 MHz, T_{CASE} = 25°C, V_{OUT} (DC) = $V_{DD}Q/2$, V_{OUT} (peak to peak) = 0.1V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
2. The input capacitance per pin group will not differ by more than this maximum amount for any given device.
3. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.

IDD Specifications and Conditions

Table 21: DDR2 IDD Specifications and Conditions

Notes: 1–5; notes appear on page 33.

Parameter/Condition	Symbol	Config	-3	-37E	Units
Operating one bank active-precharge current; $^{t}CK = {}^{t}CK$ (IDD), $^{t}RC = {}^{t}RC$ (IDD), $^{t}RAS = {}^{t}RAS$ MIN (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD0	x4, x8	TBD	80	mA
		x16	TBD	80	
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $^{t}CK = {}^{t}CK$ (IDD), $^{t}RC = {}^{t}RC$ (IDD), $^{t}RAS = {}^{t}RAS$ MIN (IDD), $^{t}RCD = {}^{t}RCD$ (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD1	x4, x8	TBD	90	mA
		x16	TBD	90	
Precharge power-down current; All banks idle; $^{t}CK = {}^{t}CK$ (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	IDD2P	x4, x8, x16	TBD	5	mA
Precharge quiet standby current; All banks idle; $^{t}CK = {}^{t}CK$ (IDD); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	IDD2Q	x4, x8	TBD	35	mA
		x16	TBD	35	
Precharge standby current; All banks idle; $^{t}CK = {}^{t}CK$ (IDD); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD2N	x4, x8	TBD	35	mA
		x16	TBD	35	
Active power-down current; All banks open; $^{t}CK = {}^{t}CK$ (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	IDD3P	Fast PDN Exit MR[12] = 0	TBD	25	mA
		Slow PDN Exit MR[12] = 1	TBD	6	
Active standby current; All banks open; $^{t}CK = {}^{t}CK$(IDD), $^{t}RAS = {}^{t}RAS$ MAX (IDD), $^{t}RP = {}^{t}RP$(IDD); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD3N	x4, x8	TBD	40	mA
		x16	TBD	40	
Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $^{t}CK = {}^{t}CK$ (IDD), $^{t}RAS = {}^{t}RAS$ MAX (IDD), $^{t}RP = {}^{t}RP$ (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD4W	x4, x8	TBD	160	mA
		x16	TBD	180	
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; $^{t}CK = {}^{t}CK$ (IDD), $^{t}RAS = {}^{t}RAS$ MAX (IDD), $^{t}RP = {}^{t}RP$ (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD4R	x4, x8	TBD	150	mA
		x16	TBD	160	
Burst refresh current; $^{t}CK = {}^{t}CK$ (IDD); Refresh command at every ^{t}RFC (IDD) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD5	x4, x8	TBD	170	mA
		x16	TBD	170	
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	IDD6	x4, x8, x16	TBD	5	mA

Table 21: DDR2 IDD Specifications and Conditions (Continued)

Notes: 1–5; notes appear on page 33.

Parameter/Condition	Symbol	Config	-3	-37E	Units
Operating bank interleave read current; All bank interleaving reads, IOUT= 0mA; BL = 4, CL = CL (IDD), AL = tRCD (IDD)-1 x tCK (IDD); tCK = tCK (IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = tRCD(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING; See IDD7 Conditions for detail.	IDD7	x4, x8	TBD	240	mA
		x16	TBD	240	

NOTE:

1. IDD specifications are tested after the device is properly initialized. 0°C ≤ T_{CASE} ≤ 85°C.
   VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V, VDDL= +1.8V ±0.1V, VREF = VDDQ/2.
2. Input slew rate is specified by AC Parametric Test Conditions.
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, DQS#, RDQS, RDQS#, LDQS, LDQS#, UDQS, and UDQS#. IDD values must be met with all combinations of EMR bits 10 and 11.
5. Definitions for IDD Conditions:
   LOW is defined as VIN ≤ VIL (AC) (MAX).
   HIGH is defined as VIN ≥ VIH (AC) (MIN).
   STABLE is defined as inputs stable at a HIGH or LOW level.
   FLOATING is defined as inputs at VREF = VDDQ/2.
   SWITCHING is defined as inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals.
   Switching is defined as inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

Table 22: General IDD Parameters

IDD Parameter	-3	-37E	Units
CL (IDD)	5	4	tCK
tRCD (IDD)	15	15	ns
tRC (IDD)	60	60	ns
tRRD (IDD) - x4/x8		7.5	ns
tRRD (IDD) - x16		10	ns
tCK (IDD)		3.75	ns
tRAS MIN (IDD)	15	45	ns
tRAS MAX (IDD)		70,000	ns
tRP (IDD)		15	ns
tRFC (IDD)		127.5	ns

IDD7 Conditions

The detailed timings are shown below for IDD7. Changes will be required if timing parameter changes are made to the specification.

Table 23: IDD7 Timing Patterns

All Bank Interleave Read operation

Speed Grade	IDD7 Timing Patterns for x4/x8/x16
-3	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D
-37E	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D

NOTE:

1. Legend: A = active; RA = read auto precharge; D = deselect.
2. All banks are being interleaved at minimum ^{t}RC (IDD) without violating ^{t}RRD (IDD) using a burst length of 4.
3. Control and address bus inputs are STABLE during DESELECTs.
4. IOUT = 0mA.

Table 24: AC Operating Conditions (Sheet 1 of 4)

Notes: 1–5; notes appear on page 38; 0°C ≤ T_{case} ≤ +85°C; VDDQ = +1.8V ±0.1V, VDD = +1.8V ±0.1V

AC CHARACTERISTICS			SYMBOL	-3		-37E		UNITS	NOTES
PARAMETER				MIN	MAX	MIN	MAX		
Clock	Clock cycle time	CL = 4	^{t}CK (4)			3,750	8,000	ps	16, 25
		CL = 5	^{t}CK (5)	3,000	8,000			ps	16, 25
	CK high-level width		^{t}CH	0.45	0.55	0.45	0.55	^{t}CK	19
	CK low-level width		^{t}CL	0.45	0.55	0.45	0.55	^{t}CK	19
	Half clock period		^{t}HP	MIN (^{t}CH, ^{t}CL)		MIN (^{t}CH, ^{t}CL)		ps	20
	Clock jitter		^{t}JIT	TBD	TBD	TBD	TBD	ps	18

Table 24: AC Operating Conditions (Sheet 2 of 4)

Notes: 1–5; notes appear on page 38; 0°C ≤ T_{case} ≤ +85°C; VDDQ = +1.8V ±0.1V, VDD = +1.8V ±0.1V

AC CHARACTERISTICS		SYMBOL	-3		-37E		UNITS	NOTES
	PARAMETER		MIN	MAX	MIN	MAX		
Data	DQ output access time from CK/CK#	^tAC	-600	+600	-500	+500	ps	
	Data-out high-impedance window from CK/CK#	^tHZ		^tAC MAX		^tAC MAX	ps	8, 9
	Data-out low-impedance window from CK/CK#	^tLZ	^tAC MIN	^tAC MAX	^tAC MIN	^tAC MAX	ps	8, 10
	DQ and DM input setup time relative to DQS	^tDS_a	400		350		ps	7, 15, 22
	DQ and DM input hold time relative to DQS	^tDH_a	400		350		ps	7, 15, 22
	DQ and DM input setup time relative to DQS	^tDS_b	150		100		ps	7, 15, 22
	DQ and DM input hold time relative to DQS	^tDH_b	275		225		ps	7, 15, 22
	DQ and DM input pulse width (for each input)	^tDIPW	0.35		0.35		^tCK	
	Data hold skew factor	^tQHS		450		400	ps	
	DQ–DQS hold, DQS to first DQ to go nonvalid, per access	^tQH	^tHP -^tQHS		^tHP -^tQHS		ps	15, 17
	Data valid output window (DVW)	^tDVW	^tQH - ^tDQSQ		^tQH - ^tDQSQ		ns	15, 17
Data Strobe	DQS input high pulse width	^tDQSH	0.35		0.35		^tCK	
	DQS input low pulse width	^tDQSL	0.35		0.35		^tCK	
	DQS output access time from CK/CK#	^tDQSCK	-500	+500	-450	+450	ps	
	DQS falling edge to CK rising – setup time	^tDSS	0.2		0.2		^tCK	
	DQS falling edge from CK rising – hold time	^tDSH	0.2		0.2		^tCK	
	DQS–DQ skew, DQS to last DQ valid, per group, per access	^tDQSQ		350		300	ps	15, 17
	DQS read preamble	^tRPRE	0.9	1.1	0.9	1.1	^tCK	36
	DQS read postamble	^tRPST	0.4	0.6	0.4	0.6	^tCK	36
	DQS write preamble setup time	^tWPRES	0		0		ps	12, 13
	DQS write preamble	^tWPRE	0.25		0.25		^tCK	
	DQS write postamble	^tWPST	0.4	0.6	0.4	0.6	^tCK	11
	Write command to first DQS latching transition	^tDQSS	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	^tCK	

Table 24: AC Operating Conditions (Sheet 3 of 4)

Notes: 1–5; notes appear on page 38; 0°C ≤ T_{case} ≤ +85°C; VDDQ = +1.8V ±0.1V, VDD = +1.8V ±0.1V

AC CHARACTERISTICS		SYMBOL	-3		-37E		UNITS	NOTES
	PARAMETER		MIN	MAX	MIN	MAX		
Command and Address	Address and control input pulse width for each input	^tIPW	0.6		0.6		^tCK	
	Address and control input setup time	^tIS_a	600		500			6, 22
	Address and control input hold time	^tIH_a	600		500			6, 22
	Address and control input setup time	^tIS_b	350		250			6, 22
	Address and control input hold time	^tIH_b	475		375			6, 22
	CAS# to CAS# command delay	^tCCD	2		2		^tCK	
	ACTIVE to ACTIVE (same bank) command	^tRC	55		55		ns	34
	ACTIVE bank *a* to ACTIVE bank *b* command	^tRRD (x4, x8)	7.5		7.5		ns	28
		^tRRD (x16)	10		10		ns	28
	ACTIVE to READ or WRITE delay	^tRCD	15		15		ns	
	Four Bank Activate period	^tFAW (x4, x8)	37.5		37.5		ns	31
	Four Bank Activate period	^tFAW (x16)	50		50		ns	31
	ACTIVE to PRECHARGE command	^tRAS	40	70,000	40	70,000	ns	21, 34
	Internal READ to precharge command delay	^tRTP	7.5		7.5		ns	24, 28
	Write recovery time	^tWR	15		15		ns	28
	Auto precharge write recovery + precharge time	^tDAL	$^tWR + ^tRP$		$^tWR + ^tRP$		ns	23
	Internal WRITE to READ command delay	^tWTR	10		7.5		ns	28
	PRECHARGE command period	^tRP	15		15		ns	32
	PRECHARGE ALL command period	^tRPA	$^tRP + ^tCK$		$^tRP + ^tCK$		ns	32
	LOAD MODE command cycle time	^tMRD	2		2		^tCK	
	CKE LOW to CK,CK# uncertainty	^tDELAY	5.83	5.83	4.375	4.375	ns	29
Refresh	REFRESH to Active or Refresh to Refresh command interval	^tRFC	75	70,000	75	70,000	ns	14
	Average periodic refresh interval	^tREFI		7.8		7.8	µs	14
Self Refresh	Exit self refresh to non-READ command	^tXSNR	^tRFC (MIN) + 10		^tRFC (MIN) + 10		ns	
	Exit self refresh to READ command	^tXSRD	200		200		^tCK	
	Exit self refresh timing reference	^tISXR	350		250		ps	6, 30

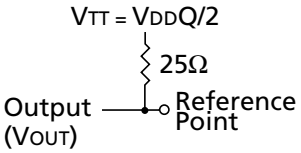
Table 24: AC Operating Conditions (Sheet 4 of 4)

Notes: 1–5; notes appear on page 38; 0°C ≤ T_{case} ≤ +85°C; VDDQ = +1.8V ±0.1V, VDD = +1.8V ±0.1V

AC CHARACTERISTICS		SYMBOL	-3		-37E		UNITS	NOTES
	PARAMETER		MIN	MAX	MIN	MAX		
ODT	ODT turn-on delay	^{t}AOND	2	2	2	2	^{t}CK	
	ODT turn-on	^{t}AON	^{t}AC (MIN)	^{t}AC (MAX) + 1000	^{t}AC (MIN)	^{t}AC (MAX) + 1,000	ps	26
	ODT turn-off delay	^{t}AOFD	2.5	2.5	2.5	2.5	^{t}CK	
	ODT turn-off	^{t}AOF	^{t}AC (MIN)	^{t}AC (MAX) + 600	^{t}AC (MIN)	^{t}AC (MAX) + 600	ps	27
	ODT turn-on (power-down mode)	^{t}AONPD	^{t}AC (MIN) + 2,000	2 x ^{t}CK + ^{t}AC (MAX) + 1000	^{t}AC (MIN) + 2000	2 x ^{t}CK + ^{t}AC (MAX) + 1,000	ps	
	ODT turn-off (power-down mode)	^{t}AOFPD	^{t}AC (MIN) + 2,000	2.5 x ^{t}CK + ^{t}AC (MAX) + 1,000	^{t}AC (MIN) + 2,000	2.5 x ^{t}CK + ^{t}AC (MAX) + 1,000	ps	
	ODT to power-down entry latency	^{t}ANPD	3		3		^{t}CK	
	ODT power-down exit latency	^{t}AXPD	8		8		^{t}CK	
Power-Down	Exit active power-down to READ command, MR[bit12=0]	^{t}XARD	2		2		tCK	
	Exit active power-down to READ command, MR[bit12=1]	^{t}XARDS	6 - AL		6 - AL		^{t}CK	
	Exit precharge power-down to any non-READ command.	^{t}XP	2		2		^{t}CK	
	Exit precharge power-down to READ command.	^{t}XPRD	6 - AL		6 - AL		^{t}CK	
	CKE minimum high/low time	^{t}CKE	3		3		^{t}CK	35

Notes

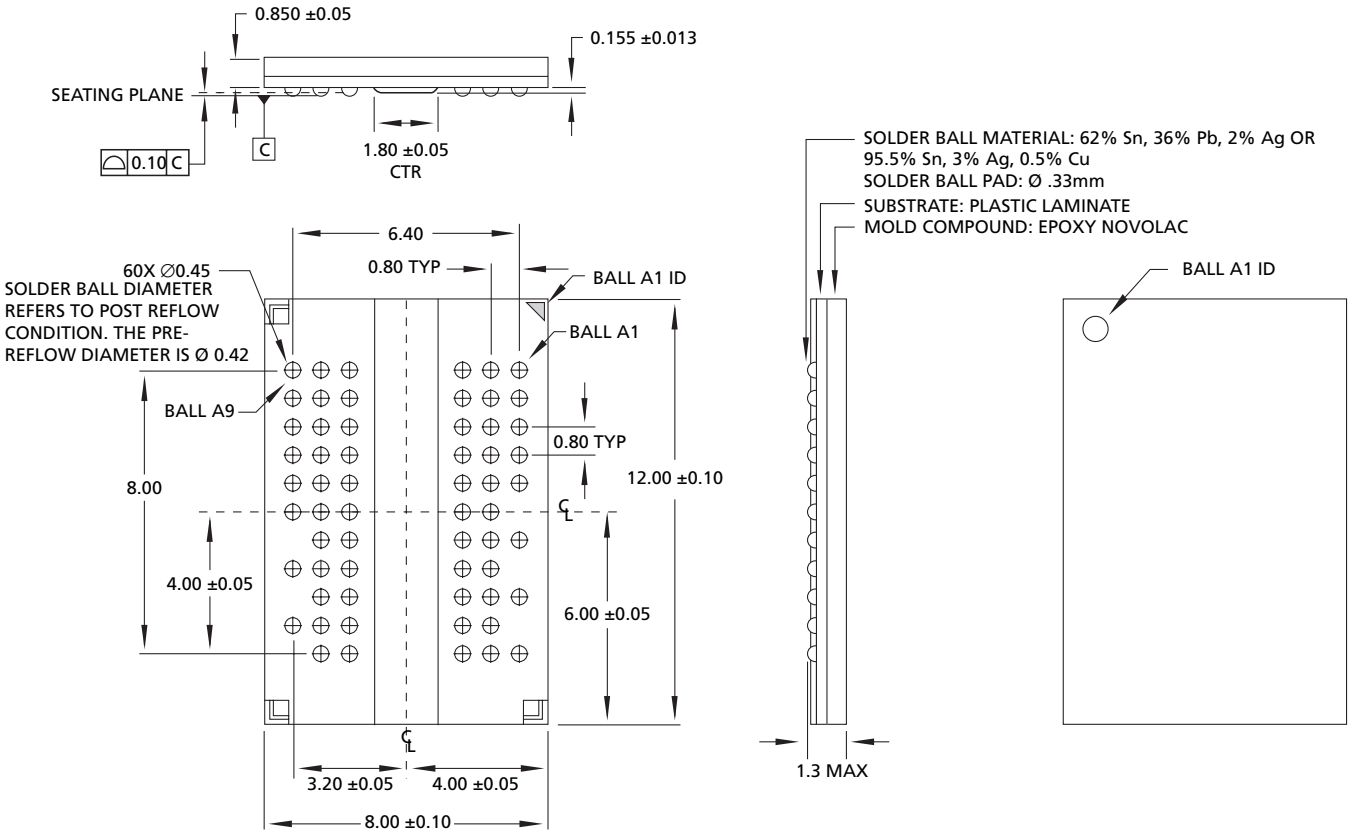
1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.0V in the test environment and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1.0V/ns for signals in the range between V_{IL} (AC) and V_{IH} (AC). Slew rates less than 1.0V/ns require the timing parameters to be derated as specified.
5. The AC and DC input level specifications are as defined in the SSTL_18 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. Command/Address minimum input slew rate is at 1.0V/ns. Command/Address input timing must be derated if the slew rate is not 1.0V/ns. This is easily accommodated using $^{t}IS_{b}$ and the Setup and Hold Time Derating Values table. ^{t}IS timing ($^{t}IS_{b}$) is referenced from V_{IH}(AC) for a rising signal and V_{IL}(AC) for a falling signal. ^{t}IH timing ($^{t}IH_{b}$) is referenced from V_{IH}(AC) for a rising signal and V_{IL}(DC) for a falling signal. The timing table also lists the $^{t}IS_{b}$ and $^{t}IH_{b}$ values for a 1.0V/ns slew rate; these are the "base" values.
7. Data minimum input slew rate is at 1.0V/ns. Data input timing must be derated if the slew rate is not 1.0V/ns. This is easily accommodated if the timing is referenced from the logic trip points. ^{t}DS timing ($^{t}DS_{b}$) is referenced from V_{IH}(AC) for a rising signal and V_{IL}(AC) for a falling signal. ^{t}IH timing ($^{t}IH_{b}$) is referenced from V_{IH}(DC) for a rising signal and V_{IL}(DC) for a falling signal. The timing table lists the $^{t}DS_{b}$ and $^{t}DH_{b}$ values for a 1.0V/ns slew rate.
   If the DQS/DQS# differential strobe feature is not enabled, timing is no longer referenced to the crosspoint of DQS/DQS#. Data timing is now referenced to V_{REF}, provided the DQS slew rate is not less than 1.0V/ns. If the DQS slew rate is less than 1.0V/ns, then data timing is now referenced to V_{IH}(AC) for a rising DQS and V_{IL}(DC) for a falling DQS.
8. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (^{t}HZ) or begins driving (^{t}LZ).
9. This maximum value is derived from the referenced test load. ^{t}HZ (MAX) will prevail over ^{t}DQSCK (MAX) + ^{t}RPST (MAX) condition.
10. ^{t}LZ (MIN) will prevail over a ^{t}DQSCK (MIN) + ^{t}RPRE (MAX) condition.
11. The intent of the Don't Care state after completion of the postamble is the DQS-driven signal should either be high, low or High-Z and that any signal transition within the input switching region must follow valid input requirements. That is if DQS transitions high (above V_{IH}DC(min) then it must not transition low (below V_{IH}(DC) prior to ^{t}DQSH(min).
12. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
13. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on ^{t}DQSS.
14. The refresh period is 64ms. This equates to an average refresh rate of 7.8125µs. However, a REFRESH command must be asserted at least once every 70.3µs or ^{t}RFC (MAX). To ensure all rows of all banks are properly refreshed, 8192 REFRESH commands must be issued every 64ms.
15. Referenced to each output group: x4 = DQS with DQ0–DQ3; x8 = DQS with DQ0–DQ7; x16 = LDQS with DQ0–DQ7; and UDQS with DQ8–DQ15.
16. CK and CK# input slew rate must be ≥ 1V/ns (≥ 2 V/ns if measured differentially).

17. The data valid window is derived by achieving other specifications - ^{t}HP. (^{t}CK/2), ^{t}DQSQ, and ^{t}QH(^{t}QH = ^{t}HP - ^{t}QHS). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived.
18. ^{t}JIT specification is currently TBD.
19. MIN(^{t}CL, ^{t}CH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. This value can be greater than the minimum specification limits for ^{t}CL and ^{t}CH). For example, ^{t}CL and ^{t}CH are = 50 percent of the period, less the half period jitter [^{t}JIT(HP)] of the clock source, and less the half period jitter due to cross talk [^{t}JIT(cross talk)] into the clock traces.
20. ^{t}HP (MIN) is the lesser of ^{t}CL minimum and ^{t}CH minimum actually applied to the device CK and CK# inputs.
21. READs and WRITEs with auto precharge *are* allowed to be issued before ^{t}RAS (MIN) is satisfied since ^{t}RAS lockout feature is supported in DDR2 SDRAM.
22. VIL/VIH DDR2 overshoot/undershoot. See "AC Overshoot/Undershoot Specification" on page 74.
23. ^{t}DAL = (nWR) + (^{t}RP/^{t}CK): For each of the terms above, if not already an integer, round to the next highest integer. ^{t}CK refers to the application clock period; nWR refers to the ^{t}WR parameter stored in the MR[11,10,9]. Example: For -37E at ^{t}CK = 3.75 ns with ^{t}WR programmed to four clocks. ^{t}DAL = 4 + (15 ns/3.75 ns) clocks = 4 +(4) clocks = 8 clocks.
24. The minimum READ to internal PRECHARGE time. This parameter is only applicable when ^{t}RTP/(2*^{t}CK) > 1. If ^{t}RTP/(2*^{t}CK) ≤ 1, then equation AL + BL/2 applies. Notwithstanding, ^{t}RAS (MIN) has to be satisfied as well. The DDR2 SDRAM will automatically delay the internal PRECHARGE command until ^{t}RAS (MIN) has been satisfied.
25. Operating frequency is only allowed to change during self refresh mode (See "Self Refresh" on page 28), precharge power-down mode (See "Power-Down Mode" on page 31), and system reset condition (see "Reset Function (CKE Low Anytime)" on page 2.
26. ODT turn-on time ^{t}AON (MIN) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn-on time ^{t}AON (MAX) is when the ODT resistance is fully on. Both are measured from ^{t}AOND.
27. ODT turn-off time ^{t}AOF (MIN) is when the device starts to turn off ODT resistance. ODT turn off time ^{t}AOF (MAX) is when the bus is in high impedance. Both are measured from ^{t}AOFD.
28. This parameter has a two clock minimum requirement at any ^{t}CK.
29. ^{t}DELAY is calculated from ^{t}IS + ^{t}CK + ^{t}IH so that CKE registration LOW is guaranteed prior to CK, CK# being removed in a system RESET condition. "Reset Function (CKE Low Anytime)" on page 2.
30. ^{t}ISXR is equal to ^{t}IS and is used for CKE setup time during self refresh exit shown in Figure 31 on page 30.
31. No more than 4 bank ACTIVE commands may be issued in a given ^{t}FAW(min) period. ^{t}RRD(min) restriction still applies. The ^{t}FAW(min) parameter applies to all 8 bank DDR2 devices, regardless of the number of banks already open or closed.
32. tRPA timing applies when the PRECHARGE(ALL) command is issued, regardless of the number of banks already open or closed. If a single-bank PRECHARGE command is issued, ^{t}RP timing applies. ^{t}RPA(min) applies to all 8-bank DDR2 devices.
33. Value is minimum pulse width, not the number of clock registrations.
34. Applicable to Read cycles only. Write cycles generally require additional time due to Write recovery time (^{t}WR) during auto precharge.
35. ^{t}CKE (MIN) of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of ^{t}IS + 2 * ^{t}CK + ^{t}IH.
36. This parameter is not referenced to a specific voltage level, but specified whwen the device output is no longer driving (^{t}RPST) or beginning to drive (^{t}RPRE).

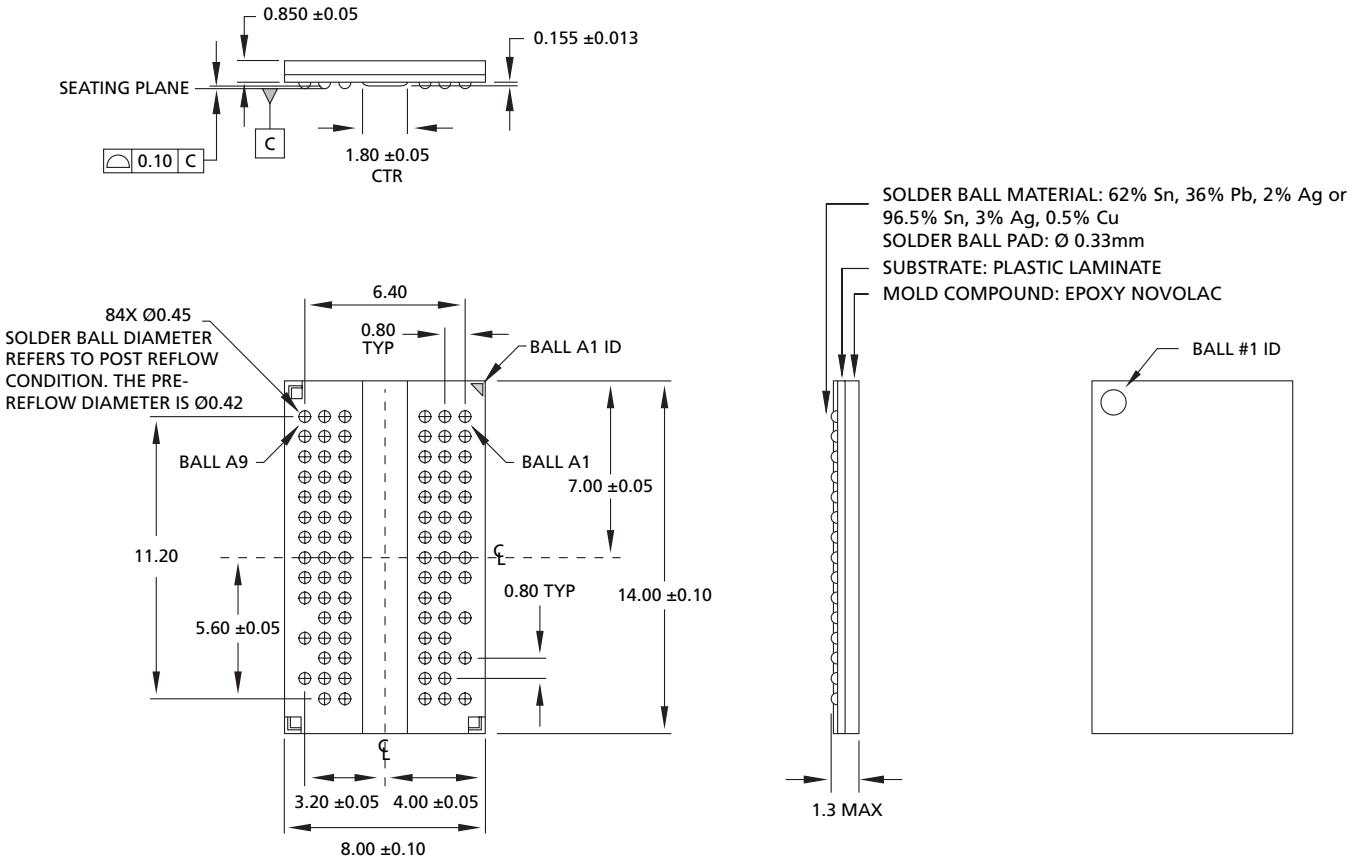
Figure 28: Package Drawing 60-Ball (8mm x 12mm) FBGA



NOTE:

All dimensions are in millimeters.

Figure 29: Package Drawing 84-Ball (8mm x 14mm) FBGA



NOTE:

All dimensions are in millimeters.

Data Sheet Designation

No Mark: This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

Part Number Options and Designations Prior to March 2005

Options	Designation
• SpecTek DDR2 Family (Call SpecTek Sales for details on availability of "x" placeholders)	SAAUx6x
• Voltage	
1.8V	0
1.9V	A
• Refresh	
8K refresh	8
• Configuration	
64 Meg x 4 (16 Meg x 4 x 4)	64M4
32 Meg x 8 (8 Meg x 8 x 4)	32M8
16 Meg x 16 (4 Meg x 16 x 4)	16M16
• FBGA Package Lead-Free	
x4, x8	
60-ball FBGA (8mm x 12mm)	FI
x16	
84-ball FBGA (8mm x 14mm)	FP
• Timing – Cycle Time	
3.0ns @ CL = 5 (DDR2-667)	-3
3.75ns @ CL = 4 (DDR2-533)	-37E

Part Number Options and Designations Prior to July 2006

Options	Designation
• SpecTek Memory	SAA
• Configuration	
64 Meg x 4 (16 Meg x 4 x 4)	64M4
32 Meg x 8 (8 Meg x 8 x 4)	32M8
16 Meg x 16 (4 Meg x 16 x 4)	16M16
• Product Code	
DDR2	Ux
• Density	
256 Megabits	6x
• Voltage/Refresh	
1.8V/8K refresh	O8
• Package – Lead-Free	
x4, x8	
60-ball FBGA (8mm x 12mm)	FIF
x16	
84-ball FBGA (8mm x 14mm)	FPF
• Package – Leaded	
x4, x8	
60-ball FBGA (8mm x 12mm)	FIL
x16	
84-ball FBGA (8mm x 14mm)	FPL
• Timing – Cycle Time	
3.0ns @ CL = 5 (DDR2-667)	-3
3.75ns @ CL = 4 (DDR2-533)	-37E

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Revision History

Rev. C, Pub. 07/06

- Updated Part number on page 1.
- Added Leaded and Lead-Free designators on page 1.

Rev. B, Pub. 3/05

- Updated Options/Designations on page 1.
- Moved Options/Designations prior to 3/04 to page 42.
- Added web link to page 5.

Rev. A, Preliminary, Pub. 10/04

- Original publication