METANOIA

MT3302 Datasheet

2012

MT3302 Datasheet

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Contents

List of Figures

List of Tables

Chapter 1

General description

1.1 Description of MT3302

The MT3302 is a highly integrated Analog Front End (AFE) for VDSL2 and ADSL/2/2+ application which provides all analog functions necessary for receiving and transmitting VDSL2 data according to ETSI and ANSI. The high integrity with low distortion and noise reduces the need for complex and costly external components. A serial control interface allows the software programming of various functional blocks. Power back off combined with power down for each block provides the flexible power saving policy. An on-chip clean up PLL provides all the required internal clocks. As single port device it is intended to be used in customer premises equipment (CPE). The full 8MHz/12MHz/17MHz/30MHz bandwidth support in downstream and upstream direction also allows the use in central office (CO).
In transmit path, it includes an interpolation filter, a 14-bit DAC, a smoothing LPF and a high performance line driver. The transmit signal bandwidth can be as wide as 30MHz with high linearity. A programmable attenuation is designed from 0dB down to -20dB in 0.5dB steps is designed for power back off. The internal line driver provides sufficient power settings required by the VDSL2 standards for PSD masks.
The receive path consists of a variable gain amplifier (VGA), an anti-aliasing LPF, a HPF, a sophisticated 14-bit ADC and a decimation filter. The VGA has a minimum gain setting of -6dB and a maximum of 48dB. The HPF cutoff frequency can be set from 32kHz to 3MHz which do more echo rejection from transmit band.
The MT3302 AFE provides highly integrated solution for VDSL2. It is available in a space saving 64-pin QFN package and is specified over the commercial (-40C to +85C) temperature range.

Chapter 2

Electrical Characteristics

2.1 Electrical characteristics for MT3302

2.1.1 Power Requirements

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Analog supply voltage DAC, LD	V_{DD-A1}	4.75	5	5.25	V	
Analog supply voltage VGA,ADC,PLL	V_{DD-A2}	2.375	2.5	2.625	V	
Digital core supply voltage	V_{DD-0}	2.375	2.5	2.625	V	
I/O-supply voltage	$V_{DD-I/O}$	1.1	-	3.5*	V	
Power consumption	$P_{SUPPLY1}$	-	1440	-	mW	line power = 14.5dBm crest factor = 14.5dB

Table 2.1: MT3302 Power Requirements

*The supply voltage for the digital I/O's can take any voltage between 1.1V and 3.5V.

2.1.2 Transmit path

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input data rate	DR_{TX}	35.328	-	70.656	V	Different data rate for different profile.
Resolution	Res_{TX}	-	14	-	$bits$	
Max. output voltage	$V_{outmaxTX}$	8	-	-	V_{dpp}	0dBfs, PBO=0dB, concept of synthesized impedance
Common more output voltage	$V_{outCMTX}$	-	$V_{DD-A1}/2$	3.5*	V	
Max. output current	$I_{outmaxTX}$	800	-	-	mA	
Output noise in-band	PSD_{IBLTX}	-	-128	-	dBm/Hz	line referred, 138kHz...30MHz
Output noise out-of-band	PSD_{OBLTX}	-	-128	-	dBm/Hz	line referred, >30MHz
Signal BW lower corner frequency	f_{lowTX}	-	32	-	kHz	
Signal BW upper corner frequency	f_{highTX}	30	-	-	MHz	
Passband ripple	PBR_{TX}	-	0.5	-	dB	line referred, >30MHz
Total harmonic distortion	THD_{TX-3}	-	-	-70	dBc	$f_{in} = 1, 4, 6, 10MHz$ @ -3dBfs harmonic in band
Missing band depth	MBD_{TX}	-	55	-	dB	
Power pack off range	GR_{PBO}	-14.5	-	0	dB	
PBO step size	SS_{PBO}	-	0.5	-	dB	
PBO accuracy	SS_{PBOADJ}	-0.5	-	0.5	dB	

Table 2.2: Transmit path

2.1.3 Receive path

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Output data rate	DR_{RX}	35.328	-	70.656	V	Different data rate for different profile.
Resolution	Res_{RX}	-	14	-	$bits$	
Max. input voltage	$V_{inmaxRX}$	-	3.6	-	V_{dpp}	VGA gain = 0dB
VGA gain range	GR_{VGA}	-6	-	48	dB	
VGA step size	SS_{VGA}	-	2 1	- -	dB dB	$Gain = -6dB - - + 12dB$ $Gain = +12dB - - + 48dB$
VGA accuracy	SS_{VGAADJ}	-0.5	-	0.5	dB	
Signal BW lower corner frequency	f_{lowRX}	-	32	-	kHz	
Signal BW upper corner frequency	f_{highRX}	30	-	-	MHz	
Passband ripple	PBR_{RX}	-	1	-	dB	
Total harmonic distortion	THD_{RX-3}	-	-	-70	dBc	$f_{in} = 1, 4, 6, 10MHz$ @ -3dBfs harmonic in band
Input noise	PSD_{LRX}	-	-135	-	dBm/Hz	
Missing band depth	MBD_{RX}	-	55	-	dB	

Table 2.3: Transmit path

2.1.4 Xtal oscillator

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Frequency	f_{OSC}	-	35.328	-	MHz	Xtal TBD
Capacitor trimming range	$\triangle C_{trim}$	6	-	38	pF	

Table 2.4: Xtal oscillator

2.1.5 Digital I/O's

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input high	V_{IH}	$V_{DD-I/O} * 0.8$	-	-	V	
Input low	V_{IL}	-	-	$V_{DD-I/O} * 0.2$	V	
Output high	V_{OH}	$V_{DD-I/O} * 0.1$	-	-	V	
Output low	V_{OL}	-	-	0.1	V	
Input capacitance	C_{in}	-	-	5	pF	
Output capacitance	C_{load}	-	-	30	pF	60MHz signal

Table 2.5: Digital I/O's

2.1.6 I/O timing

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Clock period	T_{CLK30}	-	28.871	-	ns	$CLK30 = 1/f_{OSC}$
Clock duty cycle	DC	-	50	-	%	CLK30
Rise/fall time	T_R/T_F	-	2.5	-	ns	20% to 80%
Invalid time ADC,DOUT	$T_{invalidADC}$	0	-	6	ns	See figure 2.1
Setup time DAC	$T_{setupDAC}$	12	-	-	ns	
Hold time DAC	$T_{holdDAC}$	0	-	-	ns	

Table 2.6: I/O timing

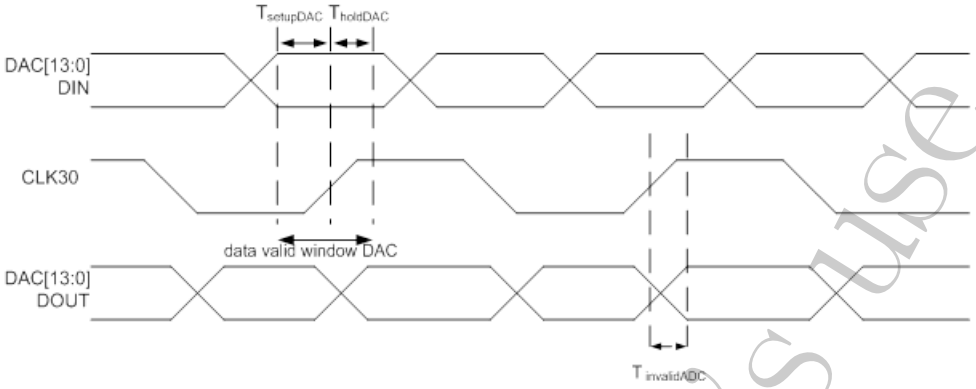

Figure 2.1: Data and control interface timing.

Chapter 3

Thermal Characteristics

3.1 Thermal characteristics for MT3302

3.1.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Storage Temperature	T_{STG}	-65	-	125	$°C$	
Junction Temperature	T_J	-40	-	125	$°C$	
Electrostatic Discharge Voltage Capability	V_{ESD}	-	-	2	kV	

Table 3.1: Absolute Maximum Ratings

3.1.2 Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Analog supply voltage DAC,LD	V_{DD-A1}	-	5	-	V	
Analog supply voltage VGA, ADC, PLL	V_{DD-A2}	-	2.5	-	V	
Digital core supply voltage	V_{DD-D}	-	2.5	-	V	
I/O-supply voltage	$V_{DD-I/O}$	1.1	-	3.5	V	
Ambient temperature	T_{AMB}	-40	25	85	$°C$	

Table 3.2: Operating Conditions

3.1.3 Thermal Resistance

Parameter	Symbol	Value	Unit	Conditions
Junction to ambient temperature	θ_{ja}	24.38	$°C/W$	4 layer PCB, 0m/s airflow
Junction to case temperature	θ_{jc}	2.41	$°C/W$	4 layer PCB, 0m/s airflow

	Material	Dimension (mm)	Thermal conductivity $(W/mm°C)$	Remark
PKG size(mm)	$9 \times 9 \times 0.8$			
Chip	Silicon	5.000×5.630	0.147	MT3302
Die Attach	EN4900GC	5.000×5.630	$0.200E-02$	-
Lead Frame	Olin194	-	$0.259E+00$	-
Die Pad	Olin194	7.800×7.800	$0.259E+00$	-
Compound	CEL9220HF	-	$0.101E-02$	-
PCB	4 layers	76.2×114.3	$0.1200E-01$	-

Table 3.3: Thermal Resistance

Chapter 4

Pin configuration

4.1 Pin assignment for MT3302

Pin	Symbol	Pad Type	Description
1	LDFBP	AI	Internal LD Feedback Input P
2	LDFBN	AI	Internal LD Feedback Input N
3	NC	DI	
4	DAC0	DI	Data 0,Interpolator/DAC input
5	DAC1	DI	Data 1,Interpolator/DAC input
6	DAC2	DI	Data 2,Interpolator/DAC input
7	DAC3	DI	Data 3,Interpolator/DAC input
8	DAC4	DI	Data 4,Interpolator/DAC input
9	VDD2.5(DIG)	Supply	Digital power supply (2.5V)
10	VDD2.5(DAC)	Supply	Analog power supply DAC,(2.5V)
11	DAC5	DI	Data 5,Interpolator/DAC input
12	DAC6	DI	Data 6,Interpolator/DAC input
13	DAC7	DI	Data 7,Interpolator/DAC input
14	DAC8	DI	Data 8,Interpolator/DAC input
15	DAC9	DI	Data 9,Interpolator/DAC input
16	DAC10	DI	Data 10,Interpolator/DAC input
17	DAC11	DI	Data 11,Interpolator/DAC input
18	DAC12	DI	Data 12,Interpolator/DAC input
19	DAC13	DI	Data 13,Interpolator/DAC input
20	VDD(PLL)	Supply	Analog power supply bandgap REF/DCXO/PLL,(2.5V)
21	XTAL1	AI	Oscillator crystal pin 1
22	XTAL2	AI	Oscillator crystal pin 2
23	VDD5	Supply	Analog power supply bandgap, REF/Switches/DAC,(5.0V)
24	NC		
25	VDDxIF	Supply	Digital power supply data interface, (3.3V)
26	ADC13	DO	Data 13,ADC/Decimator output
27	ADC12	DO	Data 12,ADC/Decimator output
28	ADC11	DO	Data 11,ADC/Decimator output
29	ADC10	DO	Data 10,ADC/Decimator output
30	ADC9	DO	Data 9,ADC/Decimator output
31	ADC8	DO	Data 8,ADC/Decimator output
32	ADC7	DO	Data 7,ADC/Decimator output
33	VDD5IF	Supply	Digital power supply (5.0V)
34	VDD2.5(DIG)	Supply	Digital power supply (2.5V)
35	SERDATAOUT	DO	Serial control interface data output
36	CLK30	DO	Clock 35MHz Out
37	VDDxIF	Supply	Digital power supply data interface,(3.3V)

Pin	Symbol	Pad Type	Description
38	SERDATAIN	DI	Serial control interface data input
39	VDD2.5(ADC)	Supply	Analog power supply ADC,(2.5V)
40	ADC6	DO	Data 6,ADC/Decimator output
41	ADC5	DO	Data 5,ADC/Decimator output
42	ADC4	DO	Data 4,ADC/Decimator output
43	ADC3	DO	Data 3,ADC/Decimator output
44	ADC2	DO	Data 2,ADC/Decimator output
45	VDD5(VGA)	Supply	Analog power supply VGA,(5V)
46	VDDxIF	Supply	Digital power supply data interface,(3.3V)
47	ADC1	DO	Data 1,ADC/Decimator output
48	ADC0	DO	Data 0,ADC/Decimator output
49	GND		
50	GND		
51	GND		
52	VGAINP	AI	VGA input P
53	VGAINN	AI	VGA input N
54	VDD2.5(VGA)	Supply	Analog power supply VGA,(2.5V)
55	HYBINP	AI	Hybrid input P
56	HYBINN	AI	Hybrid input N
57	OUTP1	AO	Positive line driver output 1
58	VDD_LD	Supply	Analog power supply line driver,(5.0V)
59	VDD_LD	Supply	Analog power supply line driver,(5.0V)
60	OUT_N1	AO	Negative line driver output1
61	OUT_P2	AO	Positive line driver output2
62	VDD_LD	Supply	Analog power supply line driver,(5.0V)
63	VDD_LD	Supply	Analog power supply line driver,(5.0V)
64	OUT_N2	AO	Negative line driver output 2

Table 4.1: Pin assignment MT3302

Note: Package bottom pad is used as the ground pin as well as the heat sink function. Therefore, it must be assigned and soldered carefully to the PCB.

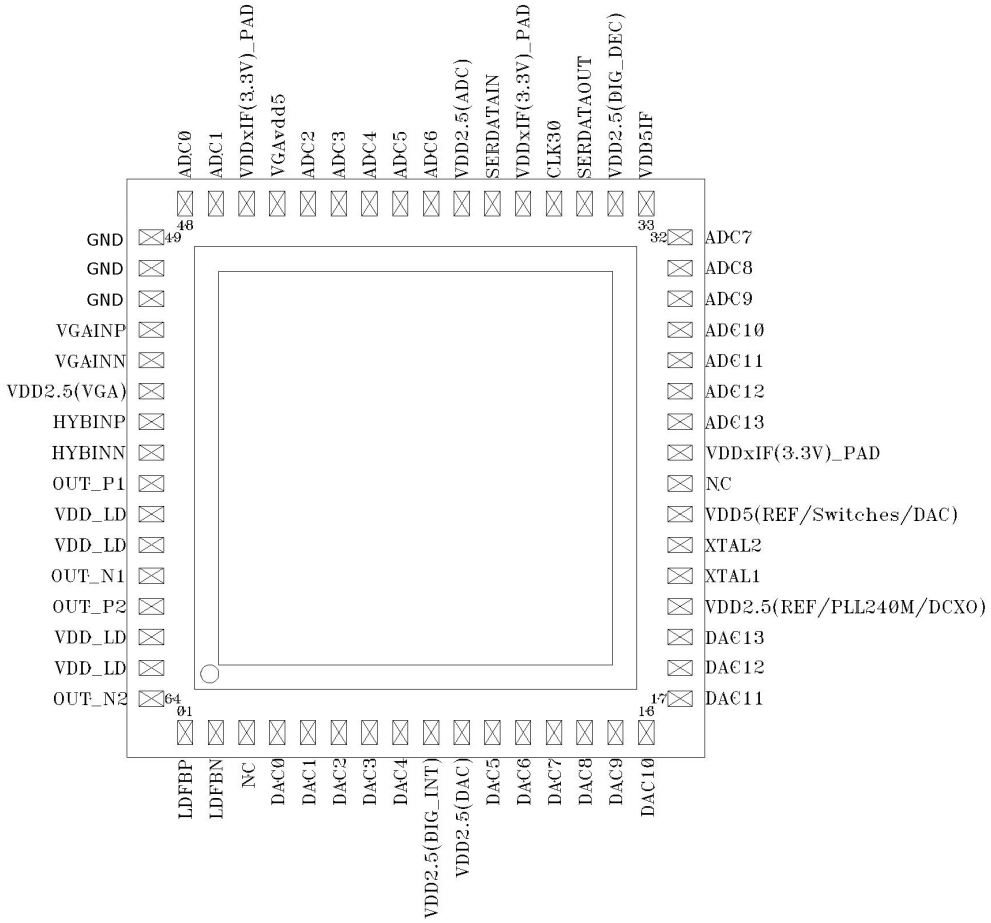

Figure 4.1: Pin diagram for MT3302

Chapter 5

Package

5.1 Package Information for MT3302

The MT3302 is packaged in a 9mm×9mm, 64 pin Quad Flat No lead package (QFN) suitable for surface mounting, as shown in figure 5.1.

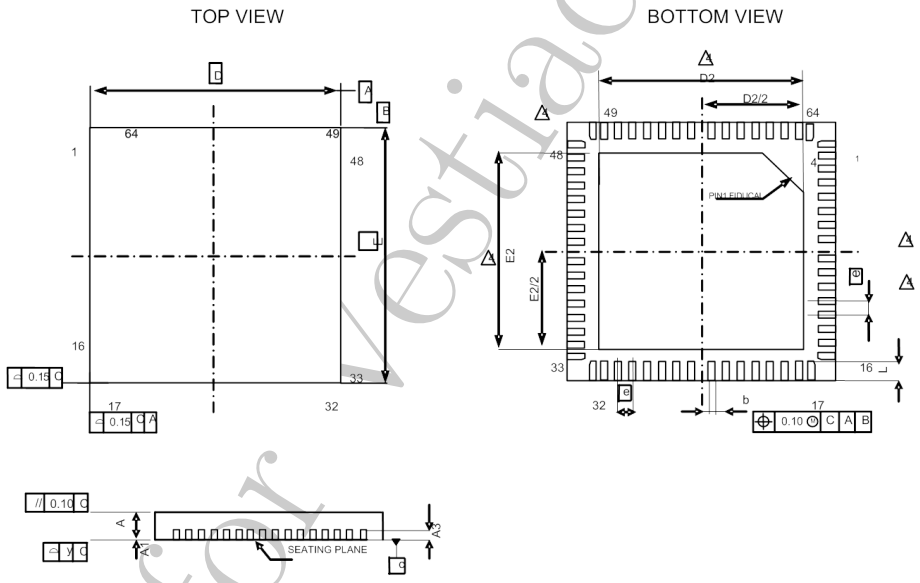

Figure 5.1: Package diagram for MT3302

Symbol	Dimension (mm)			Dimension (MIL)		
	MIN	NOM.	MAX	MIN	NOM	MAX
A	0.7	0.75	0.80	27.6	29.5	31.5
A1	0	0.02	0.05	0	0.79	1.97
A3		0.203 REF			8 REF	
b	0.18	0.25	0.28	7.1	9.8	11.0
D		9.00 BSC			354.3 BSC	
D2	7.20	7.30	7.40	283	287	291
E		9.00 BSC			354.3 BSC	
E2	7.20	7.30	7.40	283	287	291
e		0.50 BSC			19.7 BSC	
L	0.35	0.40	0.45	13.8	15.7	17.7
y		0.08			3.15	

Table 5.1: Package variations

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. REFER TO JEDEC STD. MO-220 WMMD.
3. DIMENSION “b” APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL TIP.
4. LEADFRAME MATERIAL IS OLIN194 AND THICKNESS IS 0.203mm (8 MIL).

Chapter 6

Ordering information

6.1 Ordering Information for MT3302

Part Number:
MT3302GN-A3: 1 port xDSL AFE chip with 64-QFN package.

Prefix	Part No.	RoHS	Package type	Version
MT	3302	G: Green product N: Pb product	N:QFN P:QFP L:LQFP C:CHIP B:BGA	A3

Table 6.1: MT3302 part number explanation