METANOIA

MT2311 Datasheet

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MT2311 Datasheet

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Chapter 1

Introduction

The MT2311 is part of the Metanoia MT23-family of VDSL2 chipset solutions. MT2311 is a single chip, programmable Discrete Multi-Tone (DMT) Digital Subscriber Loop (DSL) digital modulator/ demodulator processor unit for VDSL2/ADSL2+. The Device supports all committee T1E1.4 and ITU-T G.993.2 VDSL and G.992.3 ADSL2+ discrete multi-tone based specifications, as well as IEEE 802.3 10PASS-TS.

Chapter 2

Applications

The great flexibility of Metanoia's PHY module approach enables a huge variety of suitable applications, all from point-to-point solutions for industrial use to cornerstone of super high end residential- or media gateways. Below are a few application examples.

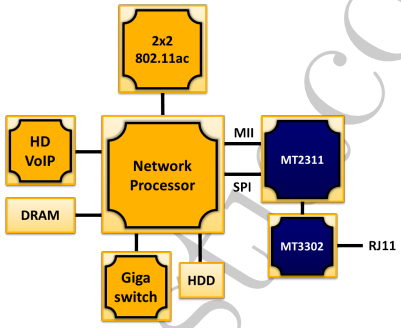

Figure 2.1: High End Gateway for the future smart home.

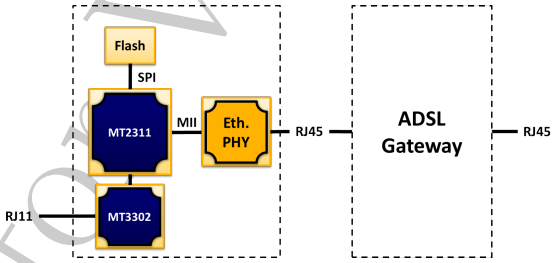

Figure 2.2: VDSL2 bridge to upgrade already deployed ADSL Gateways with VDSL capabilities.

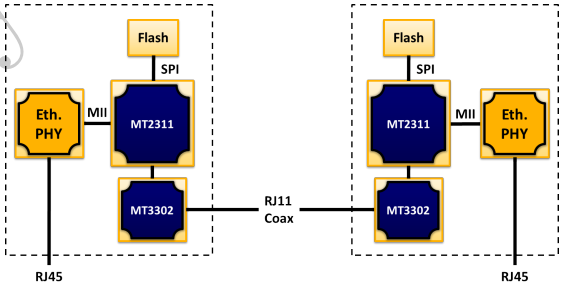

Figure 2.3: Point to point bridges for a number of Ethernet extension applications.

Chapter 3

Features of MT2311

The features of MT2311 are described below; further, the chip is operated through API commands which are described in an additional document.

General Features

- ⋆ Single chip configurable DMT data pump supporting 100Mbps/100Mbps DS/US payload data rate.
- ⋆ Conformance to T1E1, ITU-T standards for VDSL2,ADSL2/2+ and current IEEE 802.3ah draft for 10PASS-TS (EFM)
- ⋆ Supports G.inp PHY layer retransmissions described in ITU-T standard G.998.4
- ⋆ Supports G.vector for CPE side described in ITU-T standard G.993.5
- ⋆ Flexible QoS classification and queuing
- ⋆ Supports both UPBO and DPBO
- ⋆ Supports hardware based dual latency path routing
- ⋆ Optimized to support low latency applications as required for voice

Hardware Features

- ⋆ 128-lead thin quad flat package (LQFP)
- ⋆ Two packaging options:
  1. Including MII/RGMII/GMII interfaces
  2. Including MII/RGMII/SMII interfaces
- ⋆ No external RAM required. Internal RAM booted from EEPROM, Flash, or external CPU through SPI or HPI.
- ⋆ PHY software and management through IEEE 802.3 MDIO serial or through Ethernet packets with the Ethernet Boot Management (EBM) protocol

VDSL2 Features

- ⋆ Support all VDSL2 profiles (8 a/b/c/d. 12 a/b. 17a. 30a)
- ⋆ Supports Robust Overhead channel (ROC)
- ⋆ Supports SoS
- ⋆ Supports Seamless Rate Adaptation (SRA), bit-swapping and dynamic interleaver depth (D)-change
- ⋆ Up to 3072 DMT carriers supported in the downstream and upstream directions
- ⋆ All 4096 DMT carriers can be used between U/DS, with four DMT pass-bands per direction
- ⋆ Trellis coding support for up to 3072 DMT carriers in any VDSL2 mode
- ⋆ 4 KHz and 8 KHz (@2k carriers) symbol rates allow variable bandwidth per bin
- ⋆ Configurable band-plan, conforms to NA and EUR band-plans subject to the 3072/4096 and 8-band/4-passband constraints

ADSL1/2/2+ Features

- ⋆ ADSL1/2/2+ fallback
- ⋆ Conformance to ITU-T standards for ADSL1/2/2+
- ⋆ Support 0-255 VPs and 0-65535 VCs
- ⋆ Support up to 8 PVCs
- ⋆ Support ATM UNI cell –AAL5 and OAM cells
- ⋆ Support traffic shaping for upstream/downstream–CBR, UBR, rt-VBR, and nrt-VBR
- ⋆ Support fault Management functions of ATM layer
- ⋆ OAM F4/F5 cells for Segment–to–Segment and end-to-end loopbacks
- ⋆ Support LLC/SNAP and VC-MUX Ethernet bridged/routed encapsulation
- ⋆ Support PPPoA encapsulation
- ⋆ Dynamic reconfiguration
- ⋆ Support each PVC mapping to/from:
  - 802.1Q VLAN tag in Ethernet frame format
  - 802.1P Class of Service in Ethernet frame format
  - Classical IP, i.e. IP over ATM
  - Multiple PVCs to one 802.1Q VLAN mapping

3.1 Description of MT2311

3.1.1 G.inp retransmission procedures

The retransmission function can work in four modes:

- No retransmission
- Only retransmission in upstream

- Only retransmission in downstream
- Retransmission in both directions

At transceiver side the channel coded packets are saved and at the receiving side the G.inp function also stores the received packets until acceptable packets has been delivered.

3.1.2 G.vector operation

The MT2311 provides all G.vector functions for CPE side described in the ITU standard G.993.5.

- Provides VTU-R downstream and upstream vectoring functions.
- For downstream vectoring, VTU-R supports sync symbol reception and error sample computing during initialization and showtime.
- For downstream vectoring, both EOC and Ethernet L2 back channels are viable for error sample reporting.
- For upstream vectoring, VTU-R can transmit modified sync symbol as configured by VTU-O, allowing the latter to estimate channel conditions.

3.1.3 ATM operation

- Support 0-255 VPs and 0-65535 VCs
- Support up to 8 PVCs and dynamic mapping of PVCs
- Support ATM UNI cell - AAL5 and OAM cells
- Support traffic shaping for upstream/downstream - CBR, UBR, rt-VBR, and nrt-VBR
- Support fault Management functions of ATM layer
- OAM F4/F5 cells for Segment-to-Segment and end-to-end loopbacks
- Support LLC/SNAP and VC-MUX Ethernet bridged/routed encapsulation
- Support PPPoA encapsulation
- Dynamic reconfiguration
- Support each PVC mapping to/from
  - 802.1Q VLAN tag in Ethernet frame format
  - 802.1P Class of Service in Ethernet frame format
  - Classical IP, i.e. IP over ATM
  - multiple PVCs to one 802.1Q VLAN mapping

3.1.4 Quality of Service Feature

The following list defines the features of the QoS implementation in MT2311. These features allow the device to route packets between the two VDSL2 latency paths based on priority and to perform scheduling within each path. The QoS function can be applied to any Ethernet interface.

1. For TX, sort Ethernet packets into two latency paths based on the defined packet sorting mode.
2. For RX, Ethernet packets from two latency paths are combined before transmitting on MII.
3. A maximum of four priority queues are supported for one Ethernet channel. Multiple Ethernet bearer channels are not supported when QoS is enabled
4. The QoS engine supports four mutually exclusive packet sorting modes:
   - No sorting. All packets go to the default latency path.(disable QoS function)
   - Sorting based on ethertype field of Ethernet headers..

- Sorting based on VLAN ID range.
- Sorting based on VLAN priority field.

5. A configurable default latency path and queue is provided .

6. The Ethertype used for VLAN detection is configurable to support single and multi-tag (Q-in-Q) traffic.

7. Packets are routed based on the outer most VLAN tag. When multiple layers of VLAN are employed MT2311 will sort based on the outer layer and ignore the any inner layers.

8. Pause/Resume frame backpressure is normally used to avoid FIFO overflows. However, each queue can also be configured to drop packets before an overflow occurs. This mechanism allows low priority packets to be dropped without affecting high priority flows.

3.1.5 Serial Port Interface

The Serial Port Interface (SPI) provides multiple ports that can be used for various purposes. One port will usually be used to control the external AFE while another may be used for EEPROM booting or some other purpose. The ports are all full-duplex serial ports with a lot of flexibility in their programming for communicating with a variety of serial devices. All Serial Ports include comprise independent transmitter and receiver sections and a common serial clock generator.

Serial Port Rates

The Serial Port interface maximum communication rate is 1/4 of the master clock. Since MT2311 can operate up to 150 MHz, the maximum serial rate is 37.5Mbit per second. All Serial Port Interfaces need four system clocks to operate on a single bit of data. When the serial port is the clock master the minimum data rate is equal to the DSP clock frequency divided by 4096.Therefore, 36.6Kbit per second is the minimum speed for clock master mode with a 150 MHz DSP clock.

Serial Port Operation

Words transferred by the SCI are characterized by word length, shift direction, and word alignment. This section describes these characteristics and the programming associated with them.

Word Length

The Serial Port provides full control of the number of bits per word or the word length. The SCI transmit and receive data registers are 24-bits long, so 32-bits words cannot be transmitted or received. For 32-bit words, the first 24 bits contain valid data and the last bits are not defined.

Shift Direction

The Serial Port presents two options for shift direction: most significant bit (MSB) first or least significant bit (LSB) first. To select shift direction, set bit 6 in Control Register B, SHFD. If SHFD is set, the data is shifted into the receive shift register from the SRD lead and out of the transmit shift register to the STD lead with the LSB first. If SHFD is clear, the data is shifted into the receive shift register from the SRD lead and out of the transmit shift register to the STD lead with the MSB first.

Synchronization Signals

Because the Serial Port is a synchronous interface, it requires clock and frame sync signals to define when the data changes and when a new frame begins. In certain modes, the Serial Port also has the option of two flag signals to use for device selection.

Synchronous versus Asynchronous

The Serial Port includes both synchronous and asynchronous modes. In synchronous mode, the transmitters and receiver use the same clock and frame sync; in asynchronous mode, the transmitters and receiver use different clocks and frame syncs. The Serial Port data transfers are synchronized to a clock in both modes. The choice of synchronous versus asynchronous mode is determined by API command. Setting SYN puts the Serial Port is in synchronous mode; clearing SYN puts it in asynchronous mode. In synchronous mode: SCK is an input or an output that both the transmitter and receiver use as the clock signal. SC2 is an input or an output that both the transmitter and receiver use as the frame sync signal. SC0 and SC1 can be used as flag signals.

In Asynchronous Mode

SCK is an input or an output that the transmitter uses as the clock signal.
SC2 is an input or an output that the transmitter uses as the frame sync signal.
SC0 is an input or an output that the receiver uses as the clock signal.
SC1 is an input or an output that the receiver uses as the frame sync signal.
The direction of the SC0, SC1, SC2, and SCK leads is determined by the SCD0, SCD1, SCD2, and SCKD bits, respectively, CRB [3:0]. If one of these bits is clear, the corresponding lead is an input. If one of these bits is set, the corresponding lead is an output.

Serial Clock

SC‘s direction can be controlled via API command.

Frame Sync

The frame sync signal indicates when a new frame begins. In synchronous mode, the SC2 lead is the frame sync for the receiver and transmitter. In asynchronous mode, SC2 is the frame sync signal for the receiver and SC0 is the frame sync signal for transmitter 0. Frame sync is generated only when data is ready to be transmitted, i.e., data is written to a transmit data register. This mode requires that the transmit frame sync be internal (output) and the receive frame sync be external (input) for proper operation. Transmit under-runs are impossible in on-demand mode because there are no transmit time slots, thus they are disabled.

Flags

When the Serial Port is in synchronous mode, the SC0 and SC1 leads are available for use as flags.

SPI Protocol:Clock Stop Mode

A system conforming to this protocol has a master-slave configuration. SPI protocol is a 4-wire interface composed of serial data in (master in slave out), serial data out (master out slave in), shift clock (SCK), and an active (low) slave enable signal. Communication between the master and the slave is determined by the presence or absence of the master clock. Data transfer is initiated by the detection of the master clock and is terminated on absence of the master clock. The slave has to be enabled during this period of transfer. When the SPI is the master, the slave enable is derived from the master transmit frame sync pulse, SC2. The clock stop mode of the Serial Port provides compatibility with the SPI protocol. The SPI supports two SPI transfer formats specified by the clock stop mode field (CKST) in Control Register B. The clock stop mode in conjunction with the CKP bit allows serial clocks to be stopped between transfers using one of four possible timing variations.

SPI Protocol:Start Bit Mode

Some devices require a start bit to indicate the arrival of a data frame. When configured in this mode (SBIT = 1 in Control Register B) an active low start bit precedes the data followed by an active high stop bit. No frame sync is required since the receiving device frames the data. The word length control (WL [4:0]) is adjusted to specify the number of bits.

3.1.6 Host Port Interface

The host port interface (HPI) is an eight/sixteen bit parallel interface. It supports both master and slave mode operation and provides a DMA interface to the DSP memory for block transfers of up to 512 bytes. The HPI can interface with most of the microprocessors and DSPs available on the market without external

components. MT2311 employs a message interface API for command and response. The command and response message format uses HDLC-like framing, similar to the one used in G.997.1. Each command is followed by an acknowledge response typically within 1 ms. If a command is not acknowledged within 10 ms the command can be assumed to be not understood or some other error condition preventing the command can be assumed. Some commands will be acknowledged and then will be followed by a status frame sent from MT2311 to the host at a later time.

3.1.7 Boundary Scan (JTAG) Operation

When boundary scan testing is not being performed, the boundary scan register is transparent, allowing the input and output signals at the device leads to pass to and from the device's internal logic. During boundary scan testing, the boundary scan register disables the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. Data is read out from internal test registers LSB first. The following boundary scan test instructions are supported:

- -EXTEST
- -SAMPLE/PRELOAD
- -BYPASS
- -IDCODE

EXTEST Test Instruction: One of the required boundary scan tests is the external boundary test (EXTEST) instruction. When this instruction is shifted in, the device is forced into an off-line test mode. While in this test mode, the test bus can shift data through the boundary scan registers to control the external input and output leads. The MT2311 is NOT held in Reset.
SAMPLE/PRELOAD Test Instruction: When the SAMPLE/PRELOAD instruction is shifted in, the device remains fully operational. While in this test mode, input data, and data destined for device outputs, can be captured and shifted out for inspection. The data is captured in response to control signals sent to the TAP controller.
BYPASS Test Instruction: There is no explicit decode for bypass instruction. It is always selected by default. Thus any invalid instruction opcode will map to the bypass instruction. When the BYPASS instruction is shifted in, the device remains fully operational. While in this test mode, a scan operation will transfer serial data from the TDI input, through an internal scan cell, to the TDO lead. The purpose of this instruction is to abbreviate the scan path through the circuits that are not being tested to only a single clock delay.
IDCODE Instruction: When the IDCODE instruction is shifted in, the device remains fully operational. The purpose of this instruction is to output the device ID code register on the TDO lead.

Chapter 4

Electrical Characteristics

4.1 Electrical characteristics for MT2311

4.1.1 Absolute Maximum Ratings and Environmental Limitations

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage (CMOS I/O)	VDD_{IO}	-0.3	3.6	V	Note 1,4
Supply voltage (Core)	VDD_{CORE}	-0.3	1.1	V	Note 1,4
Supply Voltage (PLL)	VCC_{PLL}	-0.3	1.1	V	Note 1,4
DC input voltage	V_{IN}	-0.5	5.5	V	Note 1,4,5
Storage temperature range	T_S	-55	+150	$°C$	Note 1
Ambient operating	T_A	0	+85	$°C$	0 ft/min linear
Temperature	ME	5	-	$Level$	Per IPC/JEDEC
Moisture exposure level	RH	30	60	%	Note 2
Relative humidity level	RH	0	100	%	Non-condensing
ESD classification	ESD	2		kV	Note 3

Table 4.1: Values for absolute maximum ratings and environmental limitations.

Notes:

1. Operating conditions outside the min-max ranges specified may cause permanent device failure. Exposure to conditions near the min or max limits for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per JEDEC JESD22-A114-B.
4. Device core is 1.0V only.
5. MT2311 is 5 V compatible in the sense that the output logic 1 (V_{OH}) and output logic 0 (V_{OL}) levels of the MT2311 outputs have been specified at the same voltage levels that have been commonly recognized as logic 1 and logic 0 for the 5 V environment. MT2311 can generally be expected to drive 5 V TTL compatible components. However, while MT2311 outputs are able to meet the minimum input logic switching levels (V_{IH} and V_{IL}) of 5 V TTL compatible components, the output logic 1 output voltage of some 5 V components may exceed the maximum input voltage of MT2311. Depending on the technology and circuit implementation, the 5 V TTL compatible components may drive their outputs anywhere from 3 V to their V_{DD} supply level. CAUTION: Before connecting a 5 V component to the MT2311, always check to be sure that the Maximum V_{OH} of the 5 V device does not exceed the specified Maximum V_{IN} listed in the table above.

4.1.2 Thermal Characteristics

Parameter	Min	Typ	Max	Unit	Conditions
Thermal resistance-junction to ambient	-	18	-	$°C/W$	0 ft/min linear

Table 4.2: Thermal Characteristics

4.1.3 Power Requirements

Parameter	Min	Typ	Max	Unit	Conditions
V_{DDIO}	3.0	3.3	3.6	V	
I_{DDIO}	20	-	-	mA	See notes 1,2
P_{DDIO}	53.4	-	-	mW	See notes 1,2
V_{DDPLL}	3.15	3.3	3.45	V	
I_{DDPLL}	1	1	1	mA	See notes 1,2
P_{DDPLL}	3.2	3.3	3.5	mW	See notes 1,2
V_{DDCORE}	0.9	1.0	1.1	V	
I_{DDCORE}	285	285	315	mA	See notes 1,2
P_{DDCORE}	256.5	285	346.5	mW	See notes 1,2
P_{TOTAL}	313.1	341.5	403.4	mW	See notes 1,2

Table 4.3: Power Requirements

Notes:
1. Typical estimated values with nominal voltages at 25 $°C$.
2. All I_{DD} and P_{DD} values are dependent upon V_{DD}.

4.1.4 Input Parameters For LVTTL

Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	2.0	-	-	V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}	-	-	0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Input leakage current	-10		10	μA	$V_{IN} = V_{DD33} \vee V_{SS}$
Input capacitance	-	5	-	pF	

Table 4.4: Input Parameters For LVTTL

4.1.5 Input Parameters For LVTTLpu

Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	2.0	-	-	V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}	-	-	0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Internal Pull High Resistance	-	28k	-	Ω	$V_{IN} = V_{DD33} \vee V_{SS}$
Input capacitance	-	5	-	pF	

Table 4.5: Input Parameters For LVTTLpu

4.1.6 Output Parameters For CMOS 16mA

Parameter	Min	Typ	Max	Unit	Conditions
V_{OH}	2.4	-	-	V	$I_{OH} = -16mA$
V_{OL}	-	0.2	0.4	V	$I_{OL} = 16mA$
I_{OL}	-	-	16.0	mA	
I_{OH}	-	-	-16.0	mA	
Leakage tristate	-10	-	10	μA	

Table 4.6: Output Parameters For CMOS 16mA

4.1.7 Input/Output Parameters For LVTTL/CMOS 16mA

Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	2.0	-	-	V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}	-	-	0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Input leakage current	-10	-	10	μA	$V_{DD33} = 3.46$
Input capacitance	-	5	-	pF	
V_{OH}	2.4	-	-	V	$I_{OH} = -16mA$
V_{OL}	-	0.2	0.4	V	$I_{OL} = 16mA$
I_{OL}	-	-	16.0	mA	
I_{OH}	-	-	-16.0	mA	

Table 4.7: Input/Output Parameters For LVTTL/CMOS 16mA

Chapter 5

Thermal Characteristics

5.1 Thermal characteristics for MT2311

5.1.1 Thermal Resistance

Parameter	Symbol	Value	Unit	Conditions
Junction to ambient temperature	θ_{ja}	50.28	$°C/W$	4 layer PCB, 0m/s airflow, 25$°C$
Junction to case temperature	θ_{jc}	9.5	$°C/W$	4 layer PCB, 0m/s airflow, 25$°C$

	Material	Dimension (mm)	Thermal conductivity ($W/mm°C$)	Remark
PKG size(mm)	$9 \times 9 \times 0.8$			
Chip	Silicon	4.450x4.4450	0.147	MT2311
Die Attach	CRM1710	4.450×4.450	$0.100E-02$	-
Lead Frame	C7025	-	$0.1703E+00$	-
Die Pad	C7025	6.000×6.000	$0.1703E+00$	-
Compound	G631L	-	$9.201E-04$	-
PCB	4 layers	76.2×114.3	$0.1200E-01$	-

Table 5.1: Thermal Resistance

Chapter 6

Pin configuration

6.1 Pin assignment for MT2311

6.1.1 General pin description

Pin	Symbol	I/O	Description
1	STXCLK	I	SMII TX CLK
2	STXSYNC	I	SMII TX SYNC
3	STXDAT_D1	I	SMII TX data 1
4	STXDAT_D0	I	SMII TX data 0
5	MII_CRS	O	MII carrier sense
6	MII_COL	O	MII collision
7	RGMII/MII_RX	O	MII/RGMII/GMII receive data 3-0
8	RGMII/MII_RX	O	
9	RGMII/MII_RX	O	
10	RGMII/MII_RX	O	
11	RGMII/MII_RX	I/O	MII/RGMII/GMII indicates Rx data valid
12	RGMII/MII_RX	I/O	MII/RGMII/GMII Rx clock
13	MII_RXER	O	MII/RGMII/GMII indicates error on Rx
14	MII_TXER	I	MII/RGMII/GMII indicates error on Tx
15	RGMII/MII_TXCLK	I/O	MII/RGMII/GMII Tx clock
16	RGMII/MII_TXEN	I	MII/RGMII/GMII transmit enable
17	VDDPST	VDD I/O	VDD digital I/O supply
18	VSSPST	VSS I/O	VSS digital I/O supply
19	RGMII/MII_TXD0	I	MII/RGMII/GMII transmit data 0-1
20	RGMII/MII_TXD1	I	
21	VDD	VDD core	VDD digital core supply
22	VSS	VSS core	VSS digital core supplly
23	RGMII/MII_TXD2	I	MII/RGMII/GMII transmit data 2
24	VDD	VDD core	VDD digital core
25	VSS	VSS core	VSS digital core supply
26	RGMII/MII_TXD3	I	MII/RGMII/GMII transmit data 3
27	VDDPST	VDD I/O	VDD digital I/O supply
28	VSSPST	VSS I/O	VSS digital I/O supply
29	SRXDAT0	O	SMII/GMII Rx data 0-1
30	SRXDAT1	O	
31	SRXCLK	O	SMII/GMII Rx CLK
32	SRXSYNC	O	SMII/GMII Rx Sync
33	MDC	I	MDC
34	MDIO	I/O	MDIO
35	VCCOSC(3.3V)	VCC OSC	OSC 3.3V supply
36	XTALI	I	Master crystal oscillator input

Pin	Symbol	I/O	Description
37	XTALO	O	Master crystal oscillator input
38	VSSOSC	VSS OSC	OSC supply
39	STDA	O	SPI serial port A transmit data/GPIO(output only)
40	SRDA	I	SPI serial port A receive data/GPIO(input only)
41	SCKA	I/O	SPI serial port A clock/GPIO
42	TESTMODE	I	For internal use only/tie to ground
43	NMI	I	Non-maskable interrupt/PLL bypass lead strap
44	VDD	VDD core	VDD digital core supply
45	VSS	VSS core	VSS digital core supply
46	ARXD2	I	AFE interface receive data 2
47	VDDPST	VDD I/O	VDD digital I/O core supply
48	VSSPST	VSS I/O	VSS digital I/O supply
49	ARXD3	I	AFE interface receive data 3-6
50	ARXD4	I	
51	ARXD5	I	
52	ARXD6	I	
53	VDD	VDD core	VDD digital core supply
54	VSS	VSS core	VSS digital core supply
55	ARXD7	I	AFE interface receive data 7-8
56	ARXD8	I	
57	ACK0	I	AFE interface clock 0
58	ARXD9	I	AFE interface receive data 9-15
59	ARXD10	I	
60	ARXD11	I	
61	ARXD12	I	
62	ARXD13	I	
63	ARXD14	I	
64	ARXD15	I	
65	ATXD15	O	AFE interface transmit data 4-15
66	ATXD14	O	
67	ATXD13	O	
68	ATXD12	O	
69	ATXD11	O	
70	ATXD10	O	
71	ATXD9	O	
72	ATXD8	O	
73	ATXD7	O	
74	ATXD6	O	
75	ATXD5	O	
76	ATXD4	O	
77	VSS	VSS core	VSS digital core supply
78	VDD	VDD core	VDD digital core supply
79	ATXD3	O	AFE interface transmit data 3-2
80	ATXD2	O	
81	SCKB	I/O	SPI serial port B clock
82	STDB	O	SPI serial port B transmit data/GPIO(output only)
83	SRDB	I	SPI serial port B receive data/GPIO(input only)
84	SC2B	I/O	SPI serial port B control 2/GPIO
85	VSSPST	VSS I/O	VSS I/O supply
86	VDDPST	VDD I/O	VDD I/O supply
87	TMS	IPU	ONCE/JTAG test mode select
88	DEN	I	ONCE/JTAG debug enable
89	TDI	I	ONCE/JTAG serial test data in
90	VSS	VSS core	VSS digital core supply
91	VDD	VDD core	VDD digital core supply

Pin	Symbol	I/O	Description
92	TDO	O	ONCE/JTAG serial test data out
93	TCK	I	ONCE/JTAG test clock
94	TRSRN	IPU	ONCE/JTAG reset
95	EX_A11/GPIO0	I/O	Ext. memory address 11/GPIO
96	EX_A16/GPIO1	I/O	Ext. memory address 16/GPIO
97	VCCPLL1	VCC PLL1	1.2v VCC supply for PLL1
98	VSSPLL1	VSS PLL2	VSS for PLL1
99	EX_A17/GPIO2	I/O	Ext. memory address 17/GPIO
100	EX_AA	I/O	Ext. memory address attribute 0-3/GPIO
101	EX_AA	I/O	
102	EX_AA	I/O	
103	EX_AA	I/O	
104	RESET	I	System reset signal active low
105	VSS	VSS core	VSS digital core supply
106	VDD	VDD core	VDD digital core supply
107	HP_DY	I/O	Host port slave ready
108	HP_CS	I/O	Host port chip select
109	HP_RDWRn	I/O	Host port read/write
110	HP_DS	I/O	Host port data strobe
111	EX_D0/8	I/O	Ext memory data 8/Host port data 0/GPIO
112	EX_D1/9	I/O	Ext memory data 9/Host port data 1/GPIO
113	EX_D2/10	I/O	Ext memory data 10/Host port data 2/GPIO
114	VSSPST	VSS I/O	VSS I/O supply
115	VDDPST	VDD I/O	VDD I/O supply
116	EX_D3/11	I/O	Ext memory data 11/Host port data 3/GPIO
117	EX_D4/12	I/O	Ext memory data 12/Host port data 4/GPIO
118	EX_D5/13	I/O	Ext memory data 13/Host port data 5/GPIO
119	VSS	VSS core	VSS digital core supply
120	VDD	VDD core	VDD digital core supply
121	EX_D6/14	I/O	Ext memory data 14/Host port data 6/GPIO
122	EX_D7/	15	Ext memory data 15/Host port data 7/GPIO
123	IRQA	I	External interrupt A/Test mode 0 lead strap
124	IRQB	I	External interrupt B/Test mode 1 lead strap
125	IRQC	I	External interrupt C/Test mode 2 lead strap
126	IRQD	I	External interrupt D/Test mode 3 lead strap
127	VCCPLL2	VCC PLL2	1.0v VCC supply for PLL2
128	VSSPLL2	VSS PLL2	VSS supply for PLL2

Table 6.1: Pin assignment MT2311

6.1.2 Description of Interface pins

Package:		MII/SMII/RGMII		MII/RGMII/GMII		
No.	I/O	MII/SMII	MII/RGMII	MII	RGMII	GMII
1	I/O	stxclk (l)	-	-	-	GMRXD7 (O)
2	I/O	stxsync (l)	-	-	-	GMRXD6 (O)
3	I/O	stxdat1 (l)	-	-	-	GMRXD5 (O)
4	I/O	stxdat0 (l)	-	-	-	GMRXD4 (O)
5	O	CRS	CRS	CRS	CRS	CRS
6	O	COL	COL	COL	COL	COL
7	O	MRXD3	RGMRXD3	MRXD3	RGMRXD3	GMRXD3
8	O	MRXD2	RGMRXD2	MRXD2	RGMRXD2	GMRXD2
9	O	MRXD1	RGMRXD1	MRXD1	RGMRXD1	GMRXD1
10	O	MRXD0	RGMRXD0	MRXD0	RGMRXD0	GMRXD0

Package:		MII/SMII/RGMII		MII/RGMII/GMII		
No.	I/O	MII/SMII	MII/RGMII	MII	RGMII	GMII
11	O	MRXDV	RGMRXCTL	MRXDV	RGMRXCTL	GMRXDV
12	I/O	MRXCLK(I)	RGMRXCLK(O)	MRXCLK(I)	RGMRXCLK(O)	MRXCLK(O)
13	O	MRXERR	MRXERR	MRXERR	MRXERR	MRXERR
14	I	MTXERR	MTXERR	MTXERR	MTXERR	MTXERR
15	I/O	MTXCLK(I/O)	RGMTXCLK(I)	MTXCLK(I/O)	RGMTXCLK(I)	MTXCLK (I)
16	I	MTXEN	RGMTXCTL	MTXEN	RGMTXCTL	MTXEN
19	I	MTXD0	RGMTXD0	MTXD0	RGMTXD0	MTXD0
20	I	MTXD1	RGMTXD1	MTXD1	RGMTXD1	MTXD1
23	I	MTXD2	RGMTXD2	MTXD2	RGMTXD2	MTXD2
26	I	MTXD3	RGMTXD3	MTXD3	RGMTXD3	MTXD3
29	I/O	srxdat0 (O)	-	-	-	GMTXD4 (I)
30	I/O	srxdat1 (O)	-	-	-	GMTXD5 (I)
31	I/O	srxclk (O)	-	-	-	GMTXD6 (I)
32	I/O	srxsync (O)	-	-	-	GMTXD7 (I)

Table 6.2: Description of Interface pins MT2311

6.1.3 Pin assignment

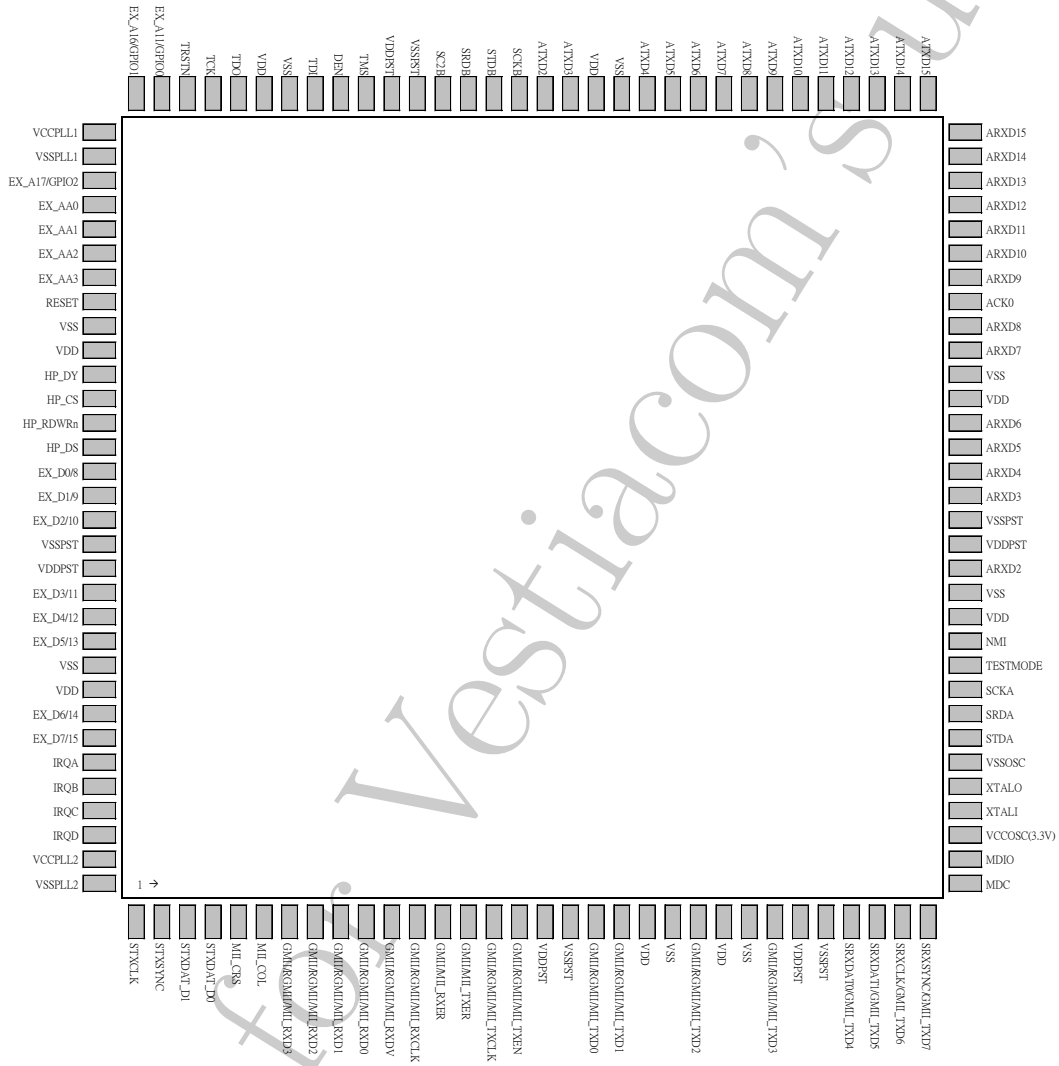

Figure 6.1: Pin diagram for MT2311

Chapter 7

Interface timing

7.1 Timing Characteristics for MT2311

This section presents the detailed timing characteristics for the MT2311 in figure 7.1 through figure 7.11 with values of the timing parameters tabulated below each waveform diagram. Detailed timing diagrams for the MT2311 device are provided in this section, with values for the timing intervals given in tables below the waveform drawings. All output times are measured with a 25 pF load capacitance for max conditions and 5 pF load capacitance for min conditions, unless noted otherwise. Timing parameters are measured at voltage levels of $(V_{IH} + V_{IL})/2$ and $(V_{OH} + V_{OL})/2$, for input and output signals, respectively. All input transition times, 10/90%, used for timing measurements are 1.0 ns for max conditions and 0.2 ns for min conditions.

7.1.1 Host Port Interface timing

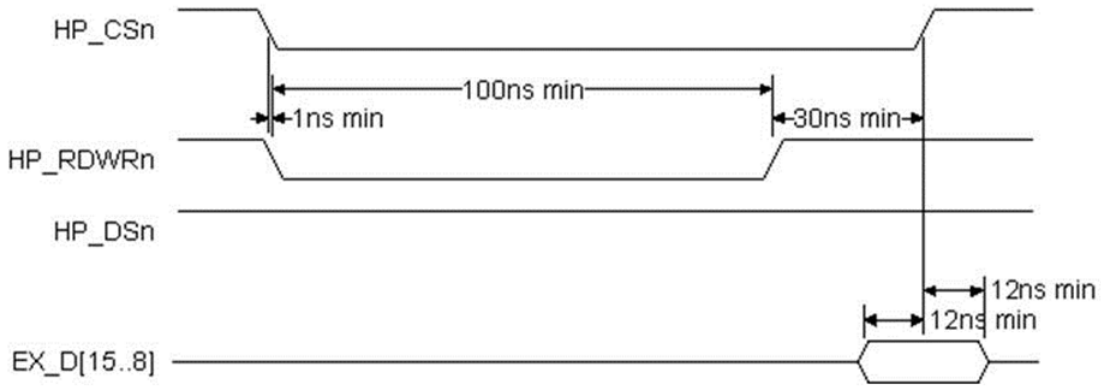

Figure 7.1: Host port read cycle timing.

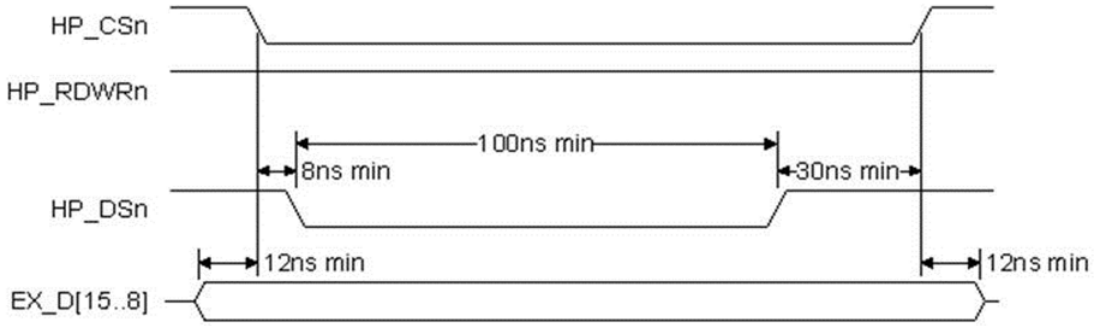

Figure 7.2: Host port write cycle timing.

7.1.2 Serial Port Interface timing

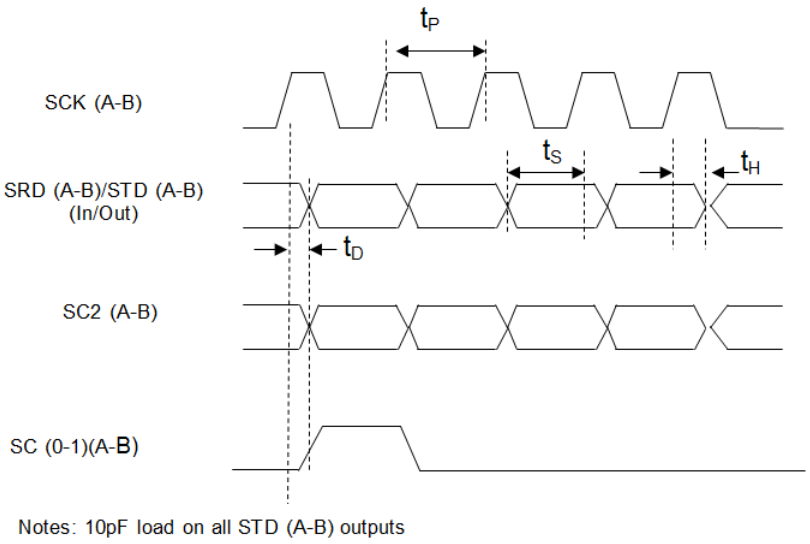

Figure 7.3: Serial Port A-B interface timing.

Parameter	Symbol	Min	Typ	Max	Unit
SCK(A-B) frequency	$1/t_P$	0.036	-	37.5	MHz
SCK(A-B) duty cycle	t_P	30	-	30 000	ns
SRD(A-B)/STD(A-B) delay from SCK↑	t_D	30	-	100	ns
SRD(A-B)/STD(A-B) setup from SCK↑	t_S	15	-	-	ns
SRD(A-B)/STD(A-B) hold from SCK↑	t_H	0.0	-	-	ns
SC(0-2)(A-B) delay from SCK↑	t_D	10	-	100	ns

Table 7.1: Serial port A-B interface timing.

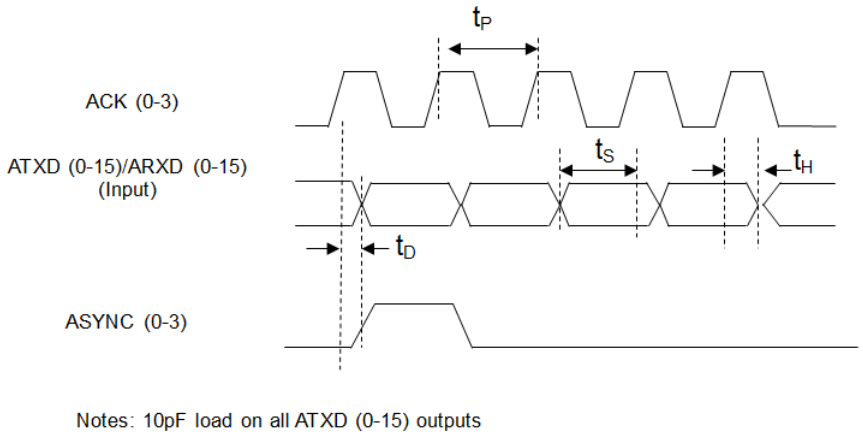

Figure 7.4: Serial Port 0-3 interface timing.

Parameter	Symbol	Min	Typ	Max	Unit
SCK(0-3) frequency	$1/t_P$	27	-	33.3	MHz
SCK(0-3) duty cycle	t_P	30	-	35	ns
SRD(0-15)/STD(0-15) delay from SCK↑	t_D	10	-	100	ns
SRD(0-15)/STD(0-15) setup from SCK↑	t_S	15	-	-	ns
SRD(0-15)/STD(0-15) hold from SCK↑	t_H	0.0	-	-	ns

Table 7.2: Serial port 0-3 interface timing.

7.1.3 SMII timing

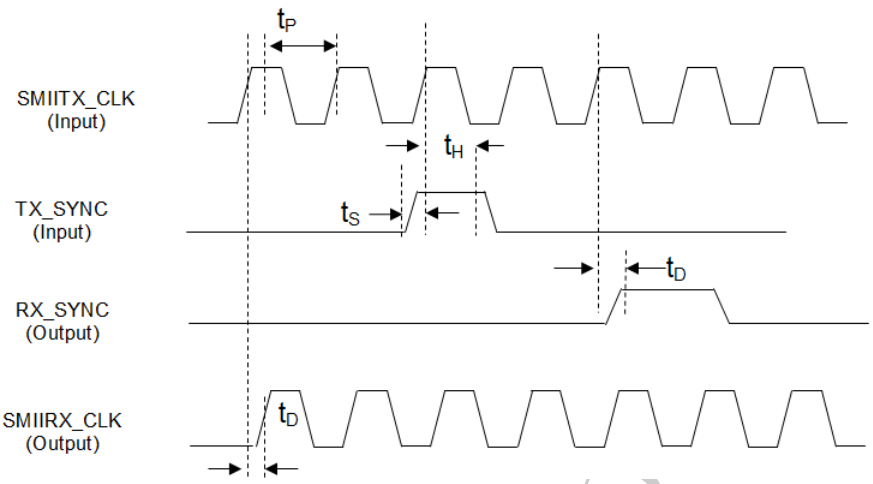

Figure 7.5: SMII Sync In/Out Timing.

Parameter	Symbol	Min	Typ	Max	Unit
SMIITX_CLK and SMIIRX_CLK period	t_P	-	8.0	-	ns
SMIIT_CLK and SMIIRX_CLK duty cycle	-	40	-	60	%
TX_SYNC setup time to SMIITX_CLK ↑	t_S	1.5	-	-	ns
TX_SYNC hold time from SMIITX_CLK ↑	t_H	1.0	-	-	ns
RX_SYNC/SMIIRX_CLK delay from SMIITX_CLK	t_D	1.5	-	4.5	ns

Table 7.3: SMII sync timing parameters.

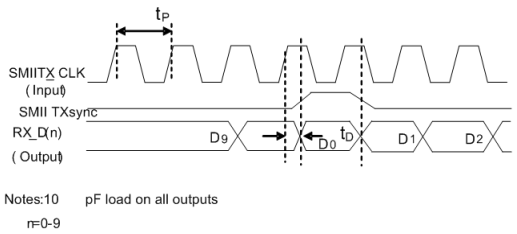

Figure 7.6: SMII Receiver interface timing.

Parameter	Symbol	Min	Typ	Max	Unit
RX_D(n) delay from SMIITX_CLK↑	t_D	1.5	-	4.5	ns

Table 7.4: SMII receiver timing parameters.

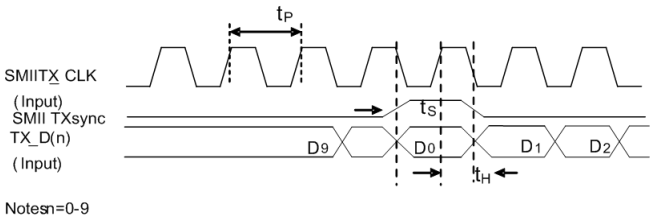

Figure 7.7: SMII transceiver interface timing.

Parameter	Symbol	Min	Typ	Max	Unit
TX(n) setup to SMIITX_CLK↑	t_S	1.5	-	-	ns
TX(n) hold from SMIITX_CLK↑	t_H	1.0	-	-	ns

Table 7.5: SMII receiver timing parameters.

7.1.4 MII timing

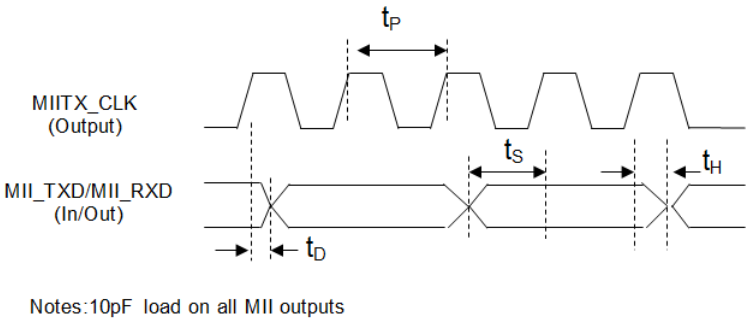

Figure 7.8: MII interface timing.

Parameter	Symbol	Min	Typ	Max	Unit
MII_CLK frequency	$1/t$	16.66	-	25	MHz
MII_CLK duty cycle	t_P	40	-	60	ns
MII_TXD/MII_RXD delay from MII CLK↑	t_D	10	-	100	ns
MII_TXD/MII_RXD setup to MII CLK↑	t_S	15	-	-	ns
MII_TXD/MII_RXD hold from MII CLK↑	t_D	0.0	-	-	ns

Table 7.6: MII timing parameters.

7.1.5 RGMII timing

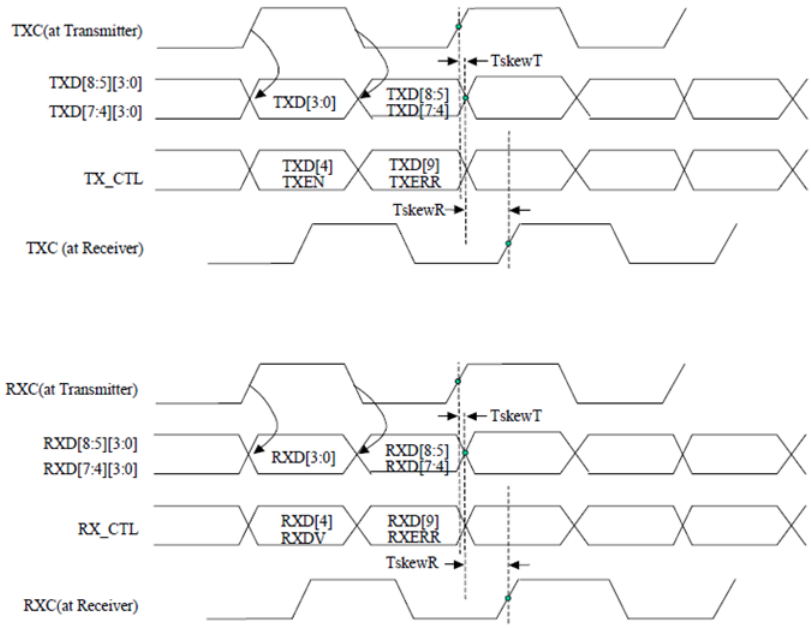

Figure 7.9: RGMII interface timing.

Parameter	Symbol	Min	Typ	Max	Unit
Data to clk output skew (at Tx)	T_{skewT}	-500	0	500	ps
Data to clk input skew (at Rx)	T_{skewR}	1	1.8	2.6	ns
Data to clk output setup (at Tx -integrated delay)	T_{holdT}	1.2	2.0	-	ns
Data to clk ouput hold (at Tx -integrated delay)	T_{holdT}	1.0	2.0	-	ns
Data to clk input setup (at Rx -integrated delay)	T_{setupR}	1.0	2.0	-	ns
Data to clk input hold (at Rx -integrated delay)	T_{holdR}	1.0	2.0	-	ns
Clk cycle duration	T_{cyc}	7.2	8	8.8	ns
Duty cycle for gigabit	$Duty_G$	45	50	55	%
Duty cycle for 10/100T	$Duty_T$	40	50	60	%
Rise / fall time (20-80%)	T_{cyc}	-	-	0.75	ns

Table 7.7: RGMII timing parameters.

7.1.6 AFE timing

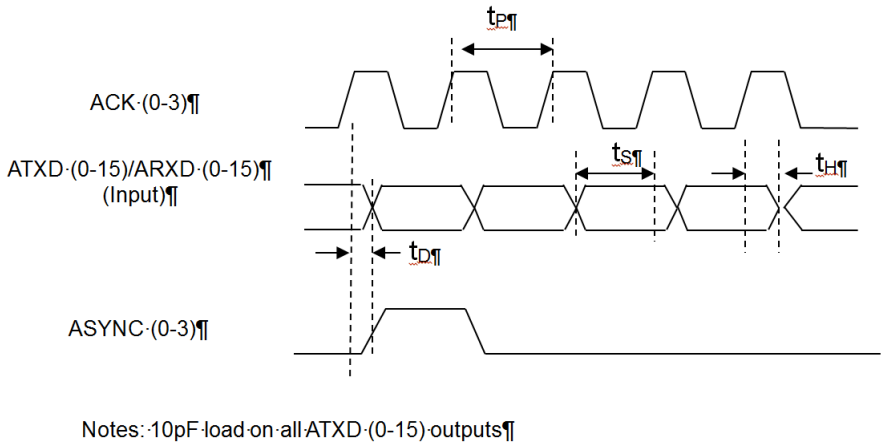

Figure 7.10: AFE interface timing.

Parameter	Symbol	Min	Typ	Max	Unit
ACCLK(0-3) frequency	$1/t$	-	35.328	-	MHz
ACCLK(0-3) duty cycle	t_P	-	28.03	-	ns
ATXD(0-15)/ARXD(0-15) delay from ACLK↑	t_D	10	-	100	ns
ATXD(0-15)/ARXD(0-15) setup to ACLK↑	t_S	15	-	-	ns
ATXD(0-15)/ARXD(0-15) hold from ACLK↑	t_H	0.0	-	-	ns

Table 7.8: AFE timing parameters.

7.1.7 Boundary scan timing

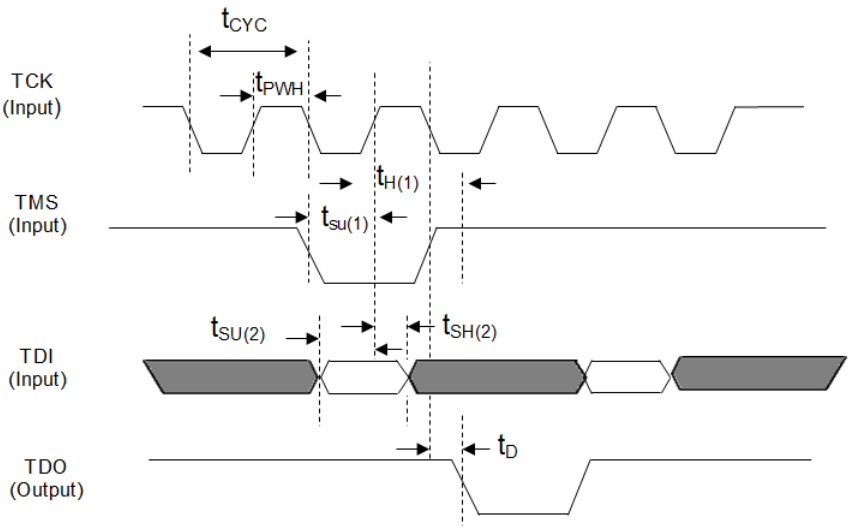

Figure 7.11: Boundary scan timing.

Parameter	Symbol	Min	Max	Unit
TCK clock cycle time	t_{CYC}	50	-	ns
TCK clock duty cycle	t_{PWH}/t_{CYC}	40	60	%
TMS setup time before TCK↑	$t_{SU(1)}$	4.0	-	ns
TMS hold time after TCK↑	$t_{H(1)}$	1.0	-	ns
TDI setup time before TCK↑	$t_{SU(2)}$	6.0	-	ns
TDI hold time after TCK↑	$t_{H(2)}$	1.0	-	ns
TDO delay after TCK↑	t_D	-	15	ns

Table 7.9: Boundary scan timing parameters.

Chapter 8

Package

8.1 Package Information for MT2311

The MT2311 device is packaged in a 14mm×14mm (3.20 mm), 128-lead thin-profile quad flat package (LQFP) suitable for surface mounting, as shown in Figure 8.1.

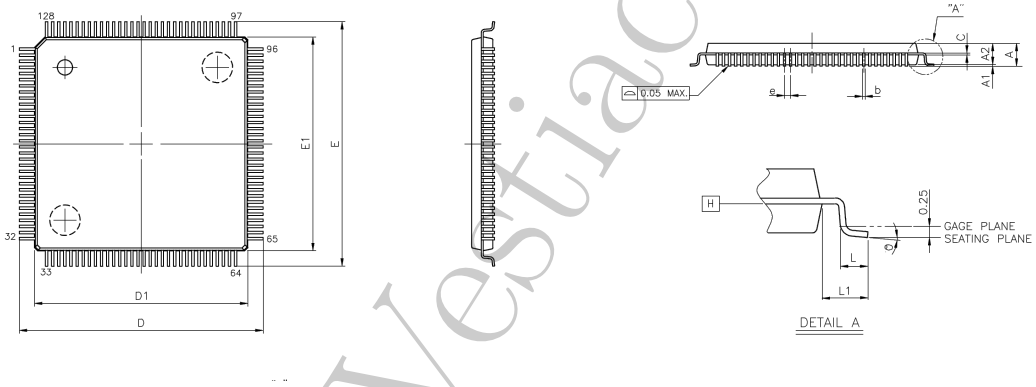

Figure 8.1: Package diagram for MT2311

Symbol	Dimension (mm)			Dimension (MIL)		
	MIN	NOM.	MAX	MIN	NOM	MAX
A	-	-	1.60	-	-	62.99
A1	0.05	-	0.15	1.97	-	5.91
A2	1.35	1.40	1.45	53.15	55.12	57.09
b	0.13	0.16	0.23	5.12	6.30	9.06
c	0.09	-	0.20	3.54	-	7.87
D	16.00 BSC			629.9 BSC		
D1	14.00 BSC			551.2 BSC		
E	16.00 BSC			629.9 BSC		
E1	14.00 BSC			551.2 BSC		
e	0.40 BSC			15.7 BSC		
L	0.45	0.60	0.75	17.72	23.62	29.53
L1	1.00 REF			39.37 REF		
○	0°	3.5°	7°	-	-	-

Table 8.1: Package variations

1. DATUM PLANE IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

Chapter 9

Ordering information

9.1 Ordering Information for MT2311

Part Number:
MT2311GL-A1: 1 port VDSL2 DMT chip with 128-LQFP package.

Prefix	Part No.	RoHS	Package type	Version
MT	2311	G: Green product N: Pb product	N:QFN P:QFP L:LQFP C:CHIP B:BGA	A3

Table 9.1: MT2311 part number explanation

