METANOIA

MT2201
&
MT3201

# Layout Guide

Rev. 1.0
2007/7/31

# Contents

# Introduction:

This document is intended to assist customers in designing a product that would optimize the CPE system performance using Metanoia DMT and AFE products. In addition, it will help comply with EMI and ESD standards. The goal is to minimize digital and common mode noise, and to provide shielding between internal circuitry and the external environment. These design practices apply to the entire system design to achieve the best overall performance.

# General Rules:

- Proper placement of components to avoid long loop traces
- Use bulk capacitor between Power and GND planes
- Use 0.1uF de-coupling capacitors to reduce high frequency noise
- Keep de-coupling capacitors as close as possible to DMT and AFE power pins
- Use of ferrite core on DC power cord to help with EMI
- Provide termination on clock lines and high speed digital signals
- Route all signals of digital bus the same lengths
- Provide impedance matching on high speed signal traces to prevent reflection
- Isolating DC-DC converter by proper shielding and GND isolation
- Route high speed signals above a continuous unbroken ground plane
- Keep all AFE analog traces as short as possible

# Power and Ground Planes:

- Maintain one MAIN GND plane, and do not split it into analog and digital ground.
- Fill copper in unused area of signal planes and connect copper to ground plane with vias
- Stagger vias to avoid creating long gaps in the planes caused by the via void

## Analog VCC Planes

Place and route the analog components within the Analog VCC plane

- **Line Driver 5V/ DAC and ADC 2.5V Planes** – Make sure the power planes are at least 4X size of AFE to provide sufficient power to AFE
- Place vias as close as possible to AFE power pins when routing to power planes
- Keep dual LD power pin traces identical to power planes (VIAS). See Fig 1, pins highlighted in red.

## Digital VCC Planes

Place and route the digital components within the Digital VCC plane

## System Ground Plane

The system ground plane should be an unbroken plane and the size of the board

- **AFE GND** - Fig 1. Place GND VIAS in a symmetrical 4x4 matrix to isolate any AC current coupling between the DAC and ADC of the AFE.

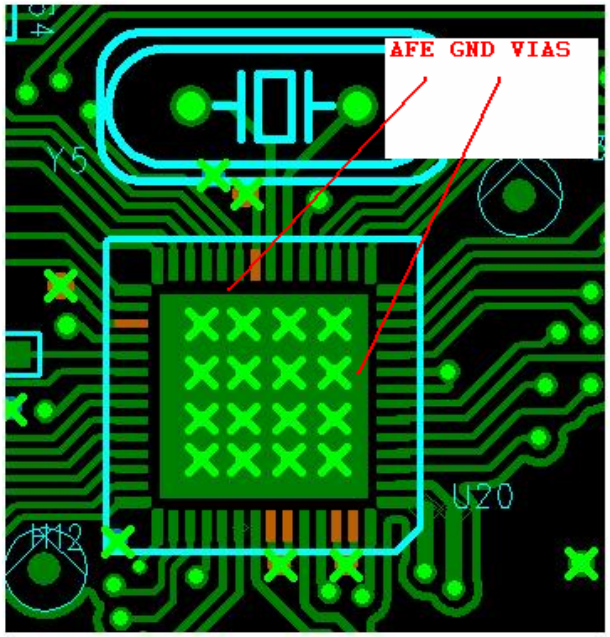


*Fig. 1. AFE GND*

## Chassis Ground Plane

The chassis ground plane should be multi-point connected to the external chassis. Place a trench around the signal ground plane to separate system ground from chassis ground. This will help with EMI and ESD.

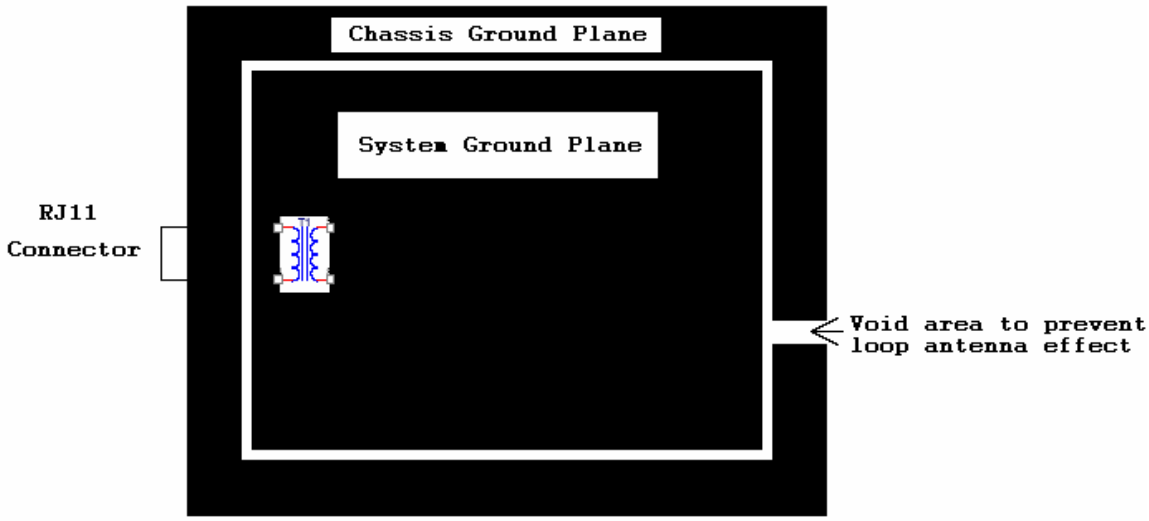


*Fig.2 Ground plane placement*

# Magnetic Noise Zone:

- Void power and ground planes directly under the magnetics
- Chassis ground should extend from the magnetics to the RJ11connector
- Do not route any digital signals between AFE and RJ11 connector.

# Clock Layout :

- Clock traces should be shortest as possible
- Use CLK buffer when driving multiple loads
- If CLK traces is longer than 2in then use it should be terminated
- If possible, surround CLK trace by ground traces to minimize EMI
- Keep CLK trace away from other signal traces

# Special Note on MT3201 (AFE) Layout

There are 7 parts need to notice for AFE layout, as show in picture as below Fig.3：

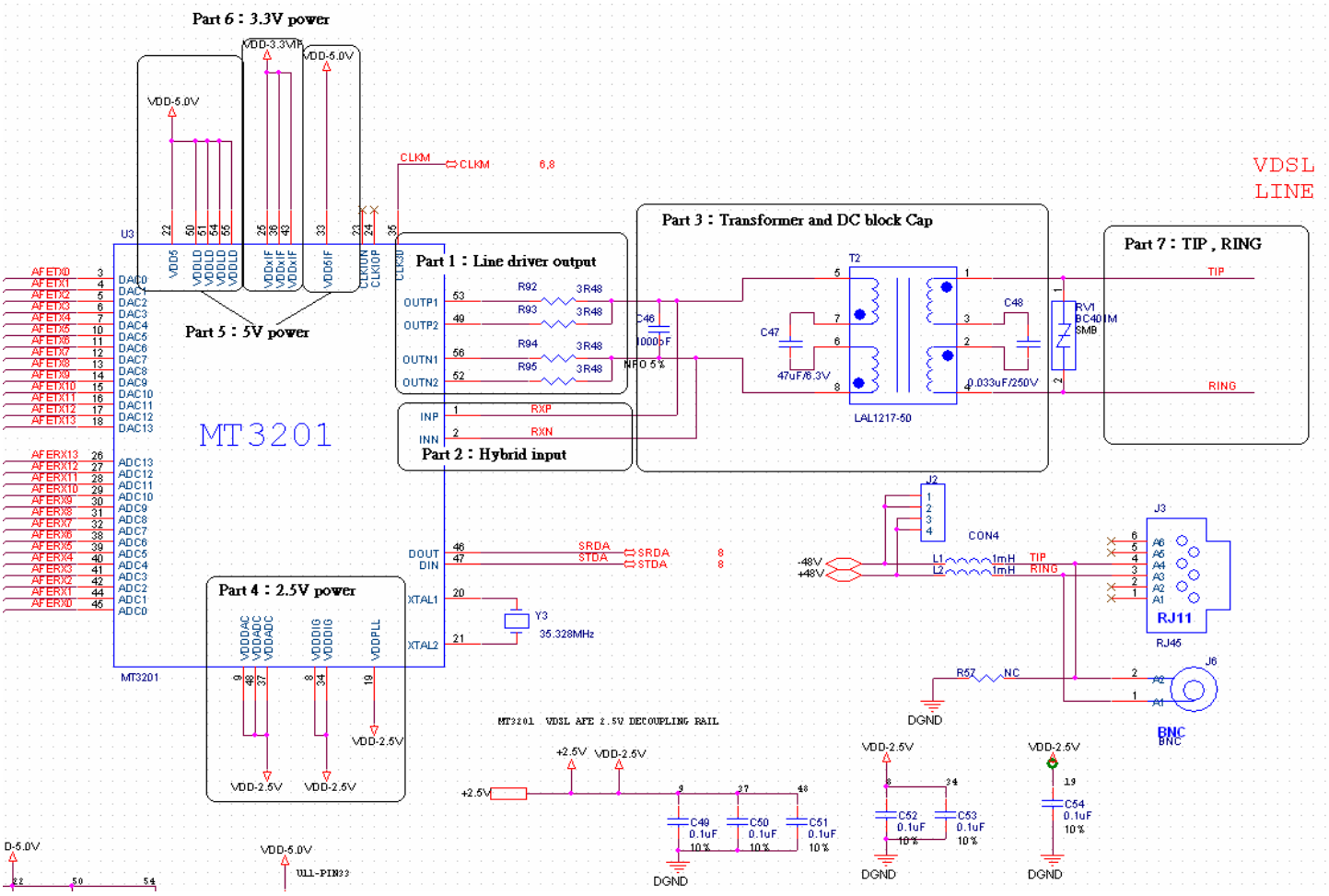


*Fig.3 Reference schematic for DMT and AFE connections*

## Part 1：Line driver output

(1) MT3021 line drivers output pin(49,52,53,56) need the same length, and should be shortest routing, and need 10mil width .
(2) Pin 53 and 56 connected to match resistor(R92,R94) on top layer as show in Fig.4.

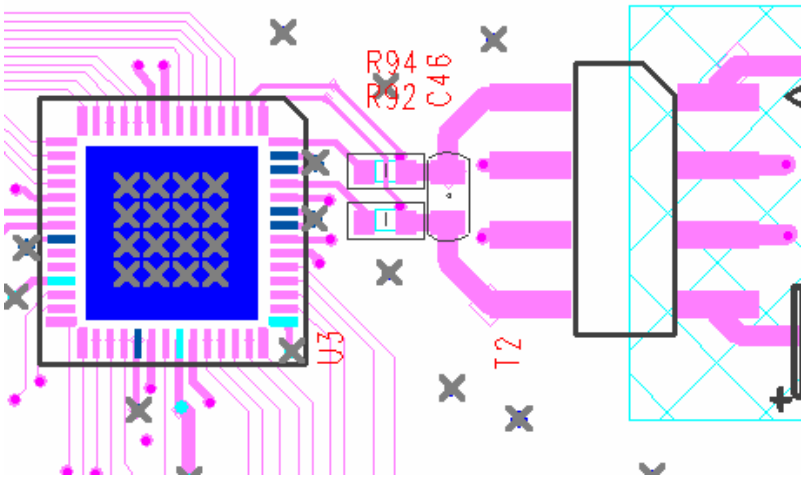


*Fig.4 MT3201 layout (front layer)*

(3) Pin 49 and 52 connected to match resistor(R93,R95) on bottom layer(see Fig.5).

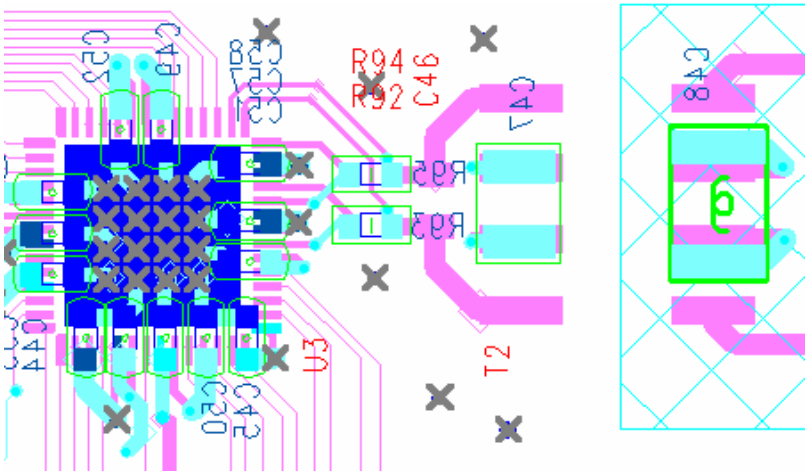


*Fig.5 MT3201 layout (bottom layer)*

## Part 2：Hybrid input

(1) MT3021 Hybrid output pin(1,2)need the same length, and should be shortest routing, and need 10mil width, as show in Fig.4.

## Part 3：Transformer and DC block cap

(1) The trace width need 20mil or above, and need shortest routing. as show in Fig.5.

## Part 4：2.5V power plane

(1) MT3201 need 3 power source and each need have power plane to supply AFE.
(2) We recommend 2.5V power plane on bottom layer and circle with AFE GND pad consistently, as show in Fig.6

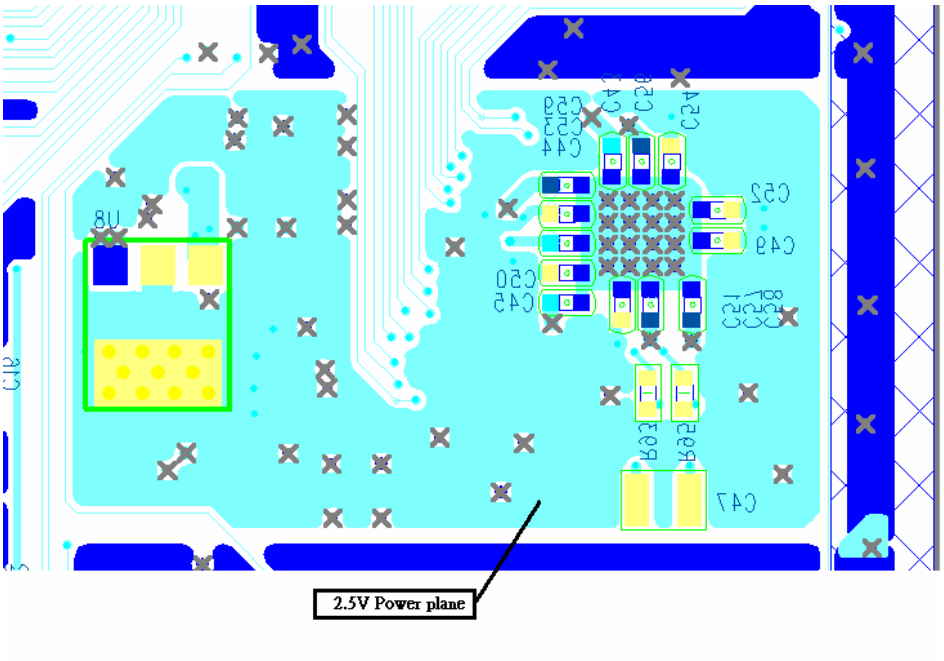


*Fig.6 AFE layout (bottom layer)*

## Part 5：5V power plane

(1) We recommend 5V power plane layer 3 and circle with AFE GND pad consistently, as show in fig.7

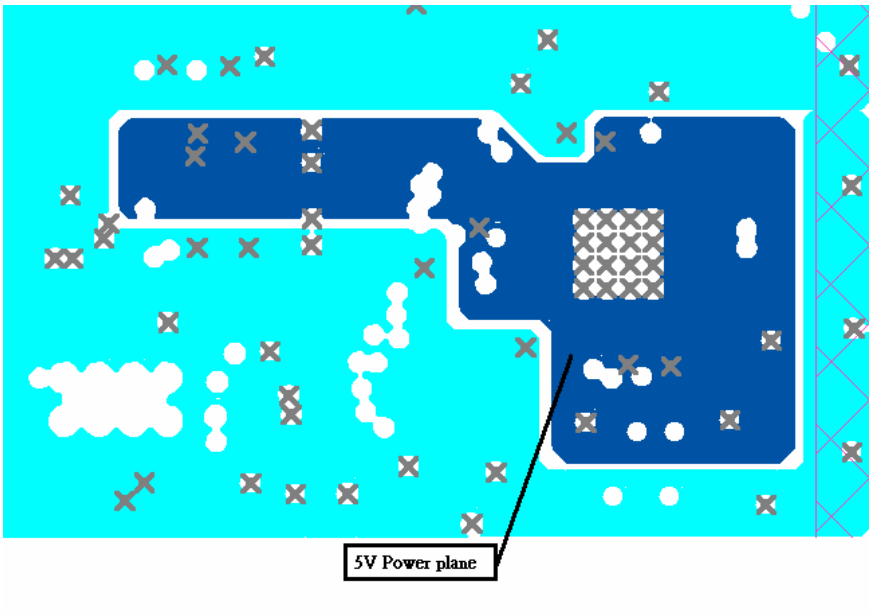


*Fig.7 AFE layout (layer 3)*

## Part 6：3.3V power plane

(1) 3.3V power do not need power plane, only need draw 12mil trace connect to 3.3V power source.

## Part 7：TIP and RING trace

TIP and RING trace recommend **parallel trace** and for certification issue both trace need keep 3mm distance from main board GND plane or other digital trace.