Falcon Device

Single VDSL DMT Chip

MT2201

Data Sheet

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Single VDSL DMT Chip

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PRODUCT REVIEW

General Description

The MT2201 is part of the Metanoia VDSL chipset solution named Falcon. The Falcon is a single chip programmable Discrete Multi-Tone (DMT) Digital Subscriber Loop (DSL) digital modulator/ demodulator processor units for broadband access. The Device supports all committee T1E1.4 and ITU-T SG15Q4 DSL discrete multi-tone based specifications, as well as IEEE 802.3 10PASS-TS.

Key Features

- Single chip configurable DMT data pump supporting one 100Mbps/50Mbps DS/US
- Up to 2048 DMT carriers downstream, Up to 2048 DMT carriers upstream
- Total DMT carriers U/D can utilize all 4096, Four DMT passbands in each direction
- Conformance to T1E1, ITU-T standards for VDSL, and current IEEE 802.3ah draft for 10PASS-TS (EFM)
- Configurable bandplan, conforms to NA, EUR and Swedish Bandplans subject to the 2048/3072 and 8-band/4-passband constraints
- Trellis coding support for up to 1024 DMT bins in any mode supporting VDSL
- Two or Four subscriber channels may be bonded into one logical channel
- Simultaneous fast and slow path operation (dual latency) on any channel
- Programmable Upstream Bandsplit DMT VDSL
- Support for 4 DMT DSL Analog Front Ends
- ATM Forum UTOPIA-2 - 4 PHY channels
- IEEE 802.3 MAC MII/SMII support for one, two or four Media Access Controllers
- Internal RAM for software stored in external flash or managed through MAC interface
- PHY software and management through IEEE 802.3 MDIO serial or a bi-directional octal interface
- Optimized to support low latency applications as required for voice
- 4 KHz and 8 KHz symbol rates allow variable bandwidth per bin
- VDSL rate over 100 Mbps on short loop with possible reach of 3,000 meters DS
- 128-lead and 208-lead thin quad flat package (LQFP)

Applications

- IP digital Subscriber Loop Access Multiplexer solution
- Multi-Service Access Platforms (MSAP)
- Customer Premise/Located Equipment for Internet Access and VoIP

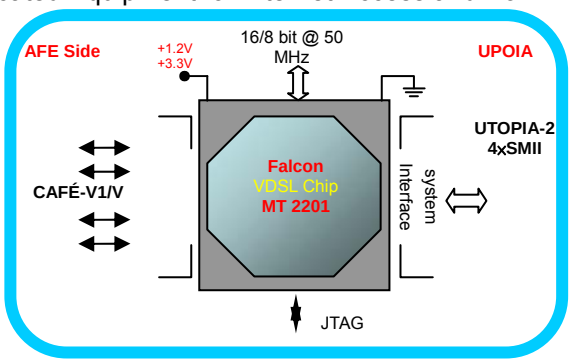

Figure 1 APPLICATION

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1 General Description

1-1 MT2201 Key Features

The Falcon supports the following features.

General Device Level

- Single chip configurable DMT processor
- Up to 2048 DMT carriers downstream
- Up to 2048 DMT carriers upstream
- Total DMT carriers U/D are limited to 4096
- Four DMT passbands in each direction
- Conformance to T1E1, ITU-T standards for VDSL
- Conformance to current IEEE 802.3ah draft for 10PASS-TS (EFM)
- Configurable bandplan, conforms to North America, European and Swedish
- Bandplans subject to the 2048/2048/3072 and 8-band /4-passband constraints
- Trellis coding support for up to 1024 DMT bins in any mode including VDSL
- Up to four autonomous DMT DSL Channels
- Two or Four subscriber channels may be bonded into one logical channel
- Simultaneous fast and slow path operation (dual latency) on any channel
- Programmable Upstream Bandsplit for DMT VDSL
- Support for one VDSL Analog Front End
- ATM Forum UTOPIA L2 bus for one, two or four PHY channels
- IEEE 802.3 SMII/MII support for one, two or four Media Access Controllers
- Internal RAM for software stored in external flash or managed through MAC interface
- PHY software and management through IEEE 802.3 MDIO serial or a bi-directional octal interface
- Optimized to support low latency applications, as required for voice
- 4 KHz and 8 KHz symbol rates allow variable bandwidth per bin
- VDSL rate over 100 Mbps on short loop with possible reach of 3,000 meters DS
- Advanced power management
- 128-lead and 208-lead LQFP package

1-1 MT2201 Application

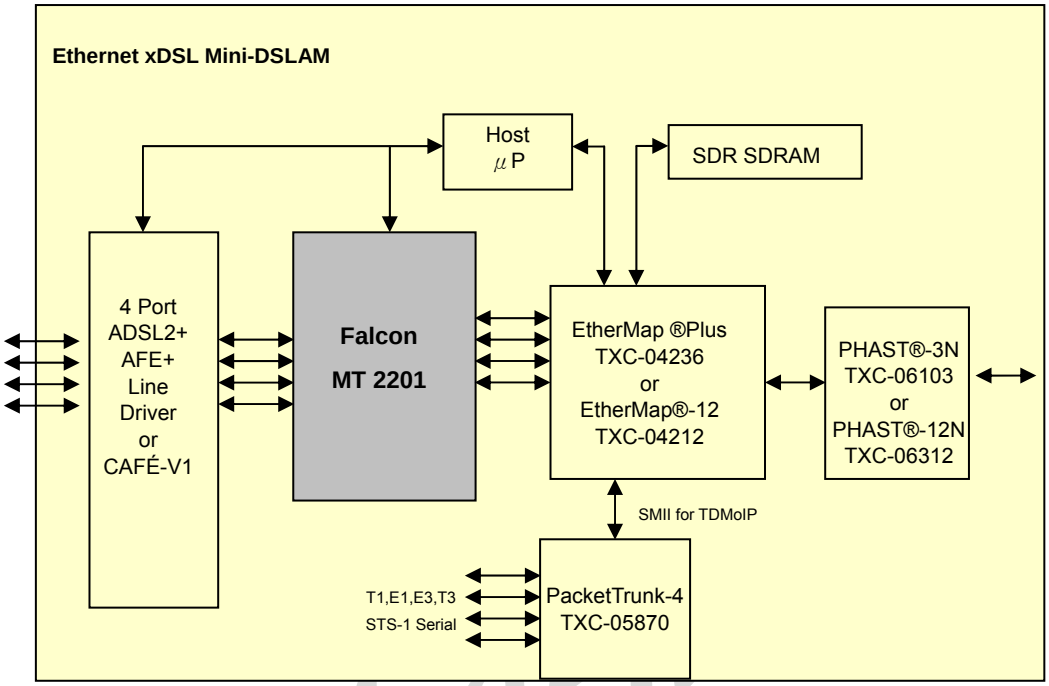

Figure 2 MTU/MDU IP DSLAM/ORD

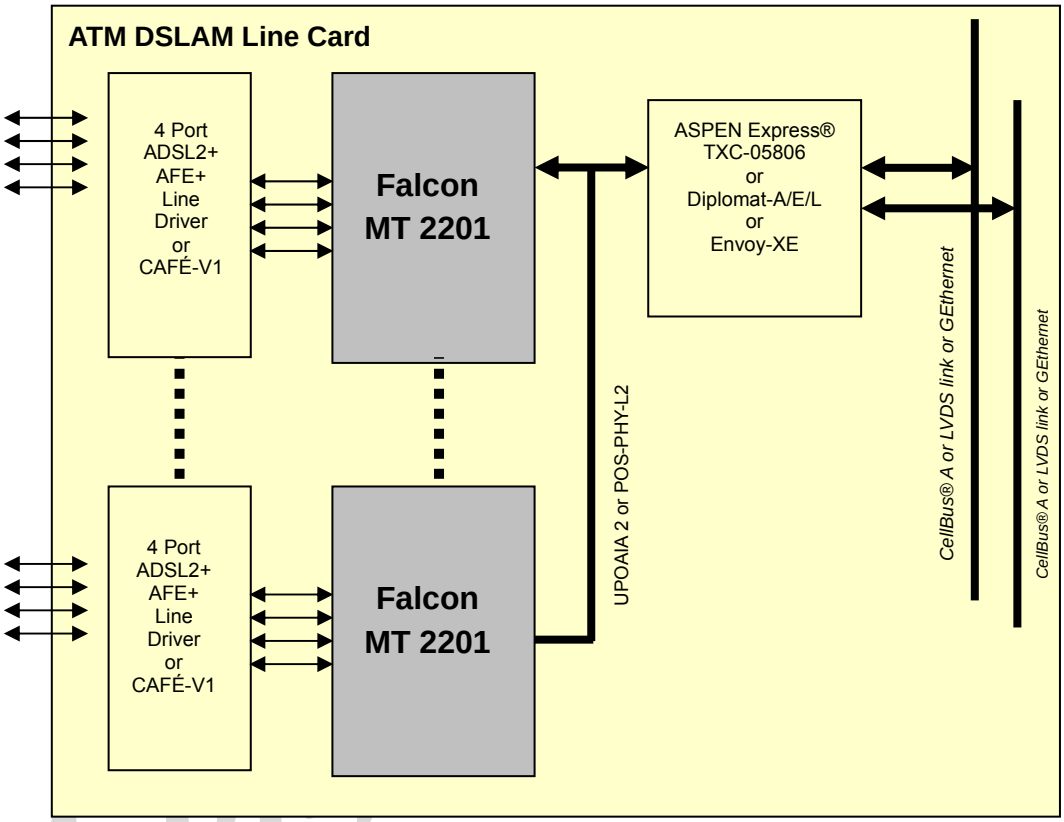

Figure 3 IP DSLAM

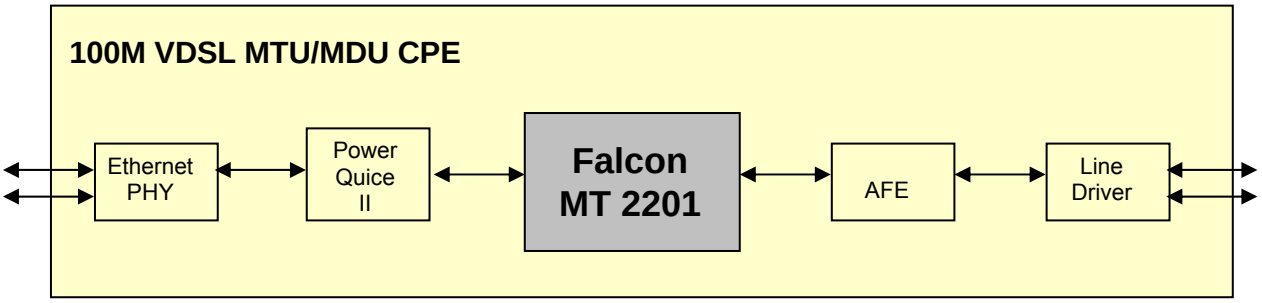

Figure 4 VDSL Modem

2 Device Description

2-1 Block Diagram

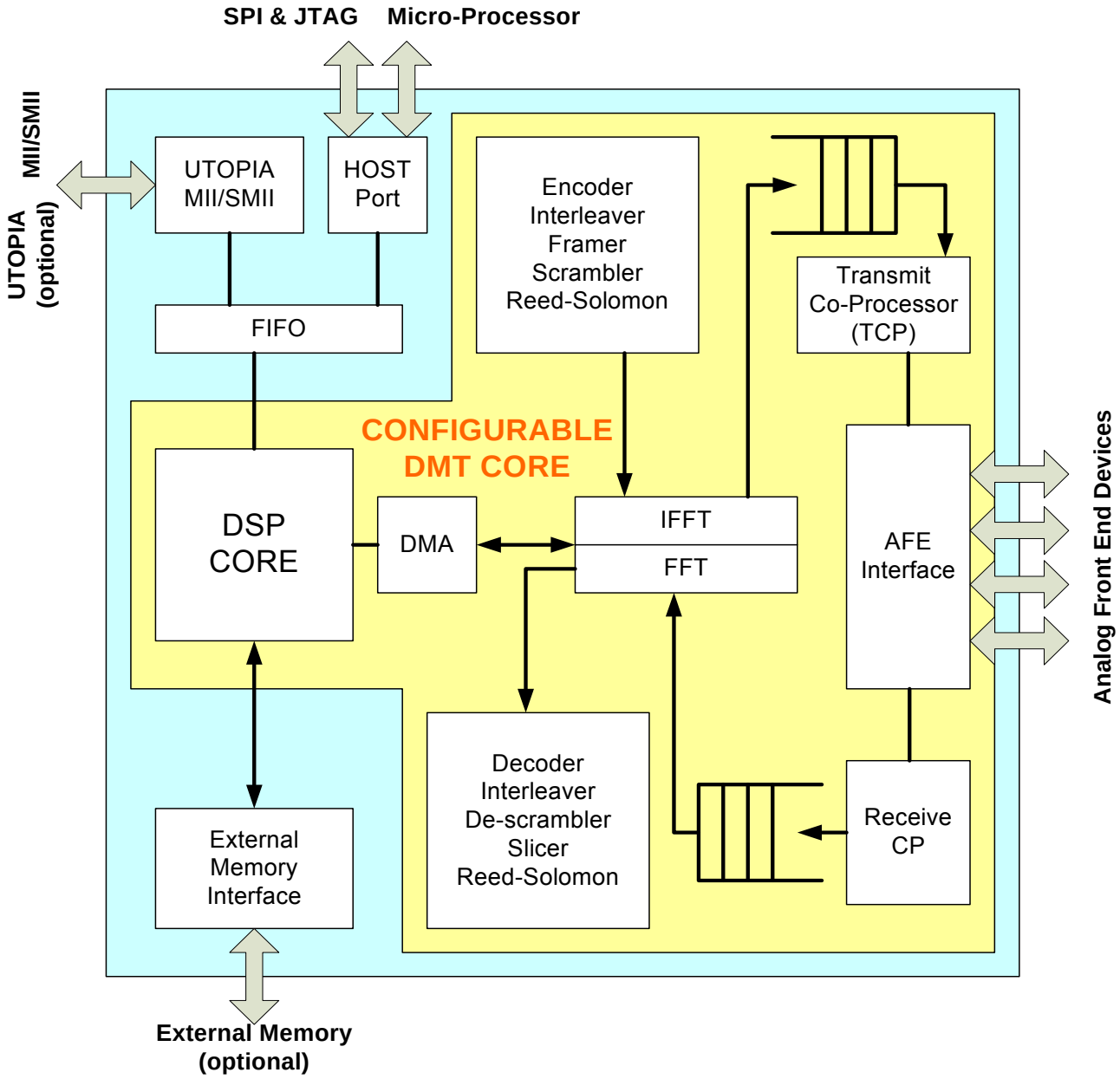

Figure 5 DAC block diagram

2-2 Block Diagram Description

The top-level architecture presented here is an area and power efficient implementation of a DMT data pump. To meet the high-speed calculation and dataflow requirements of a DMT VDSL engine the design was partitioned into a single DSP with multiple hardware coprocessor blocks. The main idea is to use the DSP for higher-level functions and control while performing most DMT calculations and data movement in the hardware blocks.

The Falcon ASIC performs all of the digital functions of a DMT based VTU-O or VTU-R physical interface. This includes all digital processing below the á and â interfaces in the VDSL reference model. It can also perform DMT calculations for up to four ADSL channels. The device is designed to be inserted into a system as an ATM or 10/100 Ethernet PHY and thus supports the PHY side of the UTOPIA L2 and Ethernet MII/SMII interfaces. A parallel host interface is also provided so that the ASIC can interface with other devices that perform higher layer functions.

The top-level block diagram for the Falcon chip is shown in Figure 5. The DSP core employed is compatible with a Motorola 56300 and thus contains an X, Y, and P memory space. All of the memory required for VDSL or four channel ADSL operations is provided on chip but an optional off chip memory can be used to support advanced features. The hardware coprocessors include an Encoder, Decoder, FFT coprocessor, TEQ coprocessor, and an AFE interface control processor. These processors perform all DMT operations from framing to cyclic extension. The coprocessors are flexible enough to handle current and future DSL configurations but do not require a lot of attention from the DSP.

Each hardware block has a set of registers mapped in the X or Y peripheral address space of the DSP A peripheral bus interface is used for transferring control information between the DSP and the hardware blocks. The local memory within each hardware block is also indirectly mapped into the peripheral address space via a memory port. This mapping gives the DSP the ability to setup DMA transfers of data to and from the distributed memories. Since a DMA interface is present on each block, DMA transfers can occur between any combination of hardware blocks, external memory, and the DSP. Between 1 and 16 wait states will be inserted per transfer when external memory is accessed using DMA. The number of wait states depends on the speed of the external memory. The external memory interface is provided for test, debug, and system expansion. External memory will not be required for normal VDSL DMT calculations.

Due to the high bandwidth requirements at various stages of the transmitter and receiver the DSP is not used for data movement. Instead each hardware block transfers data to the next under DSP control. These transfers are self-managing, controlled by DSP initialized parameters. Hardware flags are used to synchronize timing between processes. The data transfers occur on dedicated interfaces between each hardware block and the next logical block in the path. Since these interfaces are point-to-point, they are much simpler than those used for the bi-directional peripheral and DMA buses. The point-to-point buses are designed to efficiently support the dataflow requirements for Showtime operation. Since the requirements are different during training the point-to-point buses are configurable. Each hardware block can perform a

pass through from its input to output bus allowing the point-to-point buses to form a ring structure.

The hardware blocks can be triggered to begin performing calculations by the DSP or by a signal from another hardware block. Since the FFT/IFFT coprocessor has the most critical timing in the system it is used as the central timer. This processor takes approximately one half of a symbol period to process a FFT or IFFT. The end of FFT processing marks the beginning of the next sample period. At this time all hardware blocks are idle except for the continuous time domain blocks (FIFOS, TCP and AFE interface). The DSP uses this time marker to setup hardware blocks for the next symbol. The FFT coprocessor provides start symbols to the Encoder and Decoder. The Decoder is signaled to begin processing as soon as the FFT output has been written to the Decoder input FIFO. Similarly, the Encoder is signaled after the IFFT input data has been read from the Encoder output FIFO. Optionally, the DSP can control this timing directly and the hardware timing signals will be ignored. In either case, the Encoder and Decoder each have almost a full symbol period in which to perform their calculations.

2-3 Transmit Path Operation

The data to be transmitted to the remote modem arrives on the UTOPIA, MII, or Host interfaces, and is deposited into a FIFO. Since the UTOPIA and Ethernet interfaces aren't normally used simultaneously a single input FIFO is shared by both interfaces.

Once the data is deposited into the DSP memory it is available for processing or to be sent directly to the encoder via DMA. Using DSP memory in this fashion provides additional flexibility and avoids the need for a large input FIFO. In a single VDSL channel case DSP may not need to process the incoming data. However, in the case of multiple ADSL2/2+ or VDSL channels, the DSP must parse the data into separate packets for each logical path. In most situations, the DSP can simply configure the DMA channels to perform the required data separation.

The encoder performs framing, CRC generation, scrambling, interleaving, bit extraction, constellation encoding, and scaling as defined in the VDSL and ADSL2/2+ specifications. The encoder functions are divided between two hardware modules that share a common DMA, peripheral bus, and local memory: the SRS (Scrambler and Reed-Solomon) and the ICE (Interleaver and Constellation Encoder) module. As much as possible, the encoder avoids hard coding any of the intelligence required for these operations. The hardware is designed to be reasonably generic and programmable by the DSP. This approach provides flexibility for future specification changes and allows for easier reuse of the hardware for training and other non-Showtime functions. The Scrambler/Reed-Solomon (SRS) block fetches data from DSP memory via DMA and performs framing, CRC generation, scrambling, and Reed-Solomon encoding and then deposits the data in the Interleave memory. The hardware is flexible enough to support all current interleave modes and future changes. The Interleaver/ Constellation Encoder (ICE) block fetches data from the interleave memory and directly from the SRS to perform bit extraction, constellation encoding, rotation, and tone scaling. The complex addressing used for performing the interleave function is normally done by the SRS block as it fills the interleave memory. However, for maximum flexibility the ICE block contains a fully

programmable memory interface as well. This programmable interface provides the flexibility needed for generating training symbols such as O/R-P-TRAINING, O/R-P-rotator is provided to assist in generating training symbols. In multi-channel ADSL2/2+ mode, the SRS and ICE functions must be shared between up to four channels. Each processor completes an entire symbol of processing for one channel before moving to the next. The memory and other resources available for supporting VDSL are enough to support four ADSL2/2+ channels.

After constellation encoding the ICE block performs tone re-ordering and deposits the constellation points into the output FIFO (IFFT input ram). The FFT block is shared between transmit and receive paths. It performs an 8192 point real to complex FFT or complex to real IFFT. The output of the IFFT must be transferred to the TX FIFO. In the case of multiple ADSL2/2+ channels, the FIFO is logically partitioned into multiple FIFOs with individual input/output pointers. This organization allows the FFT coprocessor to fill the FIFO in the same manner as VDSL. The AFE side of the FIFO must read the data out from alternate channels on each system clock and send the data to the appropriate off chip AFE.
The AFE interface block is designed to interface the chip to a VDSL AFE or up to four ADSL2/2+ AFEs. The block is designed to be flexible enough to support existing and future AFEs. Up to 16 bits of data can be driven onto the TX leads and an additional 16 bits received on the RX leads on each 35.328Mhz sample clock. The leads can also be reconfigured as two 16 bit bi-directional buses, four 4 bit unidirectional TX and RX buses, or as serial interfaces. The serial and nibble wide interfaces are provided to support the data interfaces of multiple ADSL2/2+ AFEs simultaneously. In addition to the data buses a dedicated serial interface is provided for use in controlling each AFE. This interface is flexible enough to support many devices.

2-4 Receive Path Operation

The RX path data flow is largely the reverse of the TX. Like the TX path, the RX receives one 16-bit sample per 35.328 MHz clock from the AFE interface in VDSL mode. This data is filtered by the TEQ filter before being stored in the RX FIFO. The TEQ is a FIR that is calculated by the TCP (time domain co-processor) block. In VDSL Showtime operation, the TCP performs TEQ calculations in a serial fashion and writes its data to the RX FIFO. However, for multi-channel ADSL2/2+ modes the TCP must perform calculations for up to four channels. Since ADSL2/2+ sample rates are much lower than VDSL, the TCP does not need additional processing capabilities. It does need additional memory for the TEQ delay lines and coefficients.

Like the TX FIFO, the RX FIFO read and write pointers are controllable by DSP for use in symbol alignment. The FIFO can also be programmed to discard the cyclic prefix and can be logically partitioned into four FIFOs for multi-channel mode. After symbol sync is achieved, the RX FIFO can generate a symbol rate timing. This signal defines the symbol boundary and can be used to trigger the FFT operation. When symbol sync occurs the DSP adjusts the FIFO pointers to discard the required number of samples. The sync operation must always be accomplished with a symbol period extension so that the FFT/IFFT and other coprocessors have time to complete their operations. The TX FIFO must contain enough data to continue to supply the AFE during this extension (up to one symbol).

When the FFT block is available for performing an FFT, a symbol of data is burst transferred into the block. Similar to the TX, the single ported RX FIFO causes the burst to loose cycles while the TCP is writing the FIFO. The FFT block takes advantage of the idle butterfly hardware to perform output scaling during this transfer. The FFT signals the FCP and/or DSP when the output is ready. The FCP performs the FEQ filtering (including filter training), slicing, Viterbi decoding (ADSL or VDSL), SNR calculations, and framing. To save processing time and hardware requirements the FCP only operates on the active bins for the RX direction. The FCP block performs reverse tone ordering as it reads the data out of the FFT Output buffer. To facilitate training symbol recovery, the FCP also has pseudo-random number generator and tone rotator.

The FCP contains a specialized complex data processor that is capable of performing all FEQ, SNR, and slicing operations. The processor contains it s own program space that is written by the DSP. When the FCP has re-assembled the bit stream, it writes the data into the de-interleave memory. The de-interleaver complexity occurs in the DRS module but the FCP also has the ability to perform complex transfers to memory and the DMA bus. The de-interleave memory is shared with the DSP in the same fashion as the interleave memory. Simultaneous accesses by the DSP and hardware will result in hardware wait states. The FCP signals the DRS and/or DSP when enough data is available for de-interleaving to begin.

De-interleaving, Reed-Solomon decoding, CRC check, and de-scrambling are performed by the DRS block. The de-interleave function is performed by the addressing logic as data is fetched for Reed-Solomon decoding. Unlike the Reed-Solomon encoder, the decoder needs to have access to a full code word of data in case it needs to make corrections. Therefore, the Reed-Solomon decoder has a local 255 byte buffer to hold the maximum sized Reed-Solomon code word. After any corrections are made the data is de-scrambled, CRC checks are performed at superframe boundaries, VOC and other the fast bytes are extracted and stored in registers for DSP access. The de-framing logic has the same degree of programmability as the framer in the SRS block. The final output of the block is DMA transferred to DSP memory or directly to the Utopia/MII/SMII interface FIFO.

2-5 Analog Front End (AFE) Interface

The AFE Bus interface is designed to support several VDSL and ADSL2/2+ AFE interfaces. The AFE interface provides analog connectivity between the Analog Front End IC and time domain coprocessors (RCP and TCP) within the Falcon device. The Falcon device can be interfaced to multiple Analog Front Ends. The list below provides reference for different vendors and applications.

	AFE	Application
Fujitsu	Mb86626	2×single/dual ADSL (CO,RT)
	Mb86628	2 channel ADSL (CO)
Metanoia	CAFÉ-V2	Dual channel VDSL (CO)
	CAFÉ-V1	Single channel VDSL (CO, RT)

Table 1 AFEs and Their Vendors Already Supported by Falcon

The following signals are sent from the AFE to the Falcon device:

ADC [15:0] - 16-bits of receive data (clocked on either edge of clock)

DAC [15:0] - 16-bits of transmit data (clock on either edge of clock)

CLK0, CLK1, CLK2, CLK3 - AFE clocks (one per AFE interface)

SYNC0, SYNC1, SYNC2, SYNC3 - AFE synchronization for multi-channel operation

The RX data received from the AFE is 1/2/4/8/16-bits wide. Depending on the programmed configuration mode, the AFE interface module decodes the combination of clock and sync to determine if valid data is available. The interface packs shorter format data into a 16-bit word register at the input of a two sample fall-through stack (one per channel) for processing by the RCP (receive time coprocessor) module. Samples are passed on a P2P (point-to-point) bus to the RCP channel selected by priority encoding with the deepest stack serviced first.

The TX path is largely the inverse of the RX. Data is fetched from the output of a 4-deep circular queue (one per channel) and then transmitted on the TX interface 1/2/4/8/16-bits at a time. As a sample is removed from the queue, a request is made to re-supply the queue with a new sample being entered into the TCP (transmit time coprocessor) module. As a sample exits the TCP the sample is added to the queue. As long as a sample is produced soon enough the queue always has data available to transmit.

The 16-bit data paths may be configured as 16-bits parallel, byte-serial, nibble-serial, or bit-serial interfaces to match a particular AFE device. Each sync pulse and clock is associated with a particular ADC and DAC I/O leads for the specified mode of operation.

16-bit parallel:	ADC[15:0], DAC[15:0], CLK0, SYNC0
byte-serial:	ADC[7:0], DAC[7:0], CLK0, SYNC0 ADC[15:8], DAC[15:8], CLK2, SYNC2
nibble-serial:	ADC[3:0], DAC[3:0], CLK0, SYNC0 ADC[7:4], DAC[7:4], CLK1, SYNC1 ADC[11:8], DAC[11:8], CLK2, SYNC2 ADC[15:12], DAC[15:12], CLK3, SYNC3
bit-serial (use LS bit) or dibit-serial:	ADC[1:0], DAC[1:0], CLK0, SYNC0 ADC[5:4], DAC[5:4], CLK1, SYNC1 ADC[11:8], DAC[11:8], CLK2, SYNC2 ADC[13:12], DAC[13:12], CLK3, SYNC3

Table 2 Analog Front End (AFE) Configurations

The word count mask specifies the 2^n count value of a circular word counter. This is generally set to the number of data samples between sync pulses. An exception is the Fujitsu MB86626 which has 8 data samples between sync pulses but repeats sample order after 4, hence the word count mask = 3 in this case.

For the 16-bit parallel interface, setting the word count mask to anything other than zero creates a multi-channel mode, e.g., word count mask = 1 interleaves samples of channel 0 and channel 1 with the sync0 pulse determining the channel assignment. Setting word count mask = 3 specifies a 4-channel mode. With word count mask = 0 the sync pulse is ignored and the interface is clamped at channel 0. The nibble and byte-serial modes transmit least significant portion of the word first in time. The bit and dibit-serial modes transmit most significant portion of the word first in time. This matches the individual specifications of the AFE devices supported.

Individual word count offsets for both the ADC and DAC allow the sync pulse position to have an arbitrary alignment relative to the channel data. They essentially rotate the word count to match the channel number or word position of the data being transferred by the interface.

The AFE block is equipped with a low-power gated clock mode. Setting the soft reset bit of the CTL register will gate off the clock for the module and reset all logic. This capability is useful for reducing power consumption when Falcon is not operating.

The AFE module uses a gated and non-gated version of the DSP clock. The gated version is provided for low power mode and drives all logic except for the CTL register. The non-gated clock is used to drive the CTL register. The CTL register must always be active so that it can enable the rest of the logic on command from the DSP. The AFE interface uses four clocks: CLK0, CLK1, CLK2, and CLK3. These clocks are asynchronous to the system clock; however, the minimum period (28.3 ns) is longer than the system clock (7 ns). Four snapshot registers capture different portions of the ADC input on each of the selected external clock edges. This guarantees proper operation for clock frequencies up to 35 MHz. Each external clock is double delayed and differentiated for both positive and negative edge. Double delayed input data is captured on the selected pos/neg edge. Output data is supplied on the selected pos/neg edge. Sync pulses are always captured on the negative edge since all supported converters provide sync pulses synchronous with the positive edge of their respective clocks. The module also includes a hard and soft reset. A CTL bit controls soft reset and doubles as the clock gating signal. Independent channel enables hold the interface in a defined state for each channel when reset.
AFE Interface is controlled by a 24-bit control register which can be controlled and modified via API command.

Bit	Symbol	Description
23-20	AFE_WCNT_MASK	This is a mask for the word counter. It generates a circular word count for the number of serial words (or bits in serial mode) between sync pulses.
19-16	AFE_WCNT_AOFF	This offsets the ADC word count prior to masking by the word count mask above. It essentially rotates the count to the proper alignment to match the
15-12	AFE_WCNT_DOFF	This offsets the DAC word count prior to masking by the word count mask above. It essentially rotates the count to the proper alignment to match the
11	AFE_ADC_2X	Enables double rate serial input. (serial mode only)
10	AFE_DAC_2X	Enables double rate serial output. (serial mode only)
9-8	AFE_WSIZE	Defines the word size of the interface 0 = 16-bit parallel interface 1 = Fujitsu byte-serial interface 2 = Alcatel nibble-serial interface 3 = STMicro serial interface
6	AFE_SYNC_POL	Defines the polarity of the sync pulse. The sync pulse is always sampled on the negative edge of the clock. 0 = positive pulse 1 = negative pulse
5	AFE_ADC_POL	Defines the edge on which the ADC input is sampled. 0 = positive edge 1 = negative edge
4	AFE_DAC_POL	Defines the edge on which the DAC sample is clocked 0 = positive edge 1 = negative edge
3	AFE_CLK3	Enables AFE#3 clock 0 = Disabled 1 = Enabled
2	AFE_CLK2	Enables AFE#2 clock 0 = Disabled 1 = Enabled
1	AFE_CLK1	Enables AFE#1 clock 0 = Disabled 1 = Enabled
0	AFE_CLK0	Enables AFE#0 clock 0 = Disabled 1 = Enabled

Table 3 AFEFR as Shown in the Following Table

2-6 Ethernet Interfaces

The Media Independent Interface (MII) provides Ethernet connectivity between 10/100 Media Access Control (MAC) and Physical Layer (PHY) devices. To support EFM flow control, the MAC/PHY can be configured for half-duplex operation, i.e., as if the PHY were connected to a multi-drop Ethernet coax. This module implements the nibble wide data interfaces and serial control interface defined in the IEEE STD 802.3 clauses 22, 45, 61, 62. It performs the time critical lower level functions of the MII interface. The DSP handles higher-level functions in software.

The module is made up of a transmit path, a receive path, and a control section. To avoid confusion with the Ethernet specification, transmit and receive paths are defined with respect to the Ethernet MAC and the modem itself. Since this interface implements the PHY side of the MII the transmit (tx) path is the input and the receive (rx) path is the output.

Direct input/output FIFO connections avoid DSP assisted data transfers. Extended Management Data register set is visible to DSP and external MAC. Simple interrupt driven software interface saves DSP MIPs. A low power, gated-clock mode is provided. The Figure 6 below shows a block diagram of this interface.

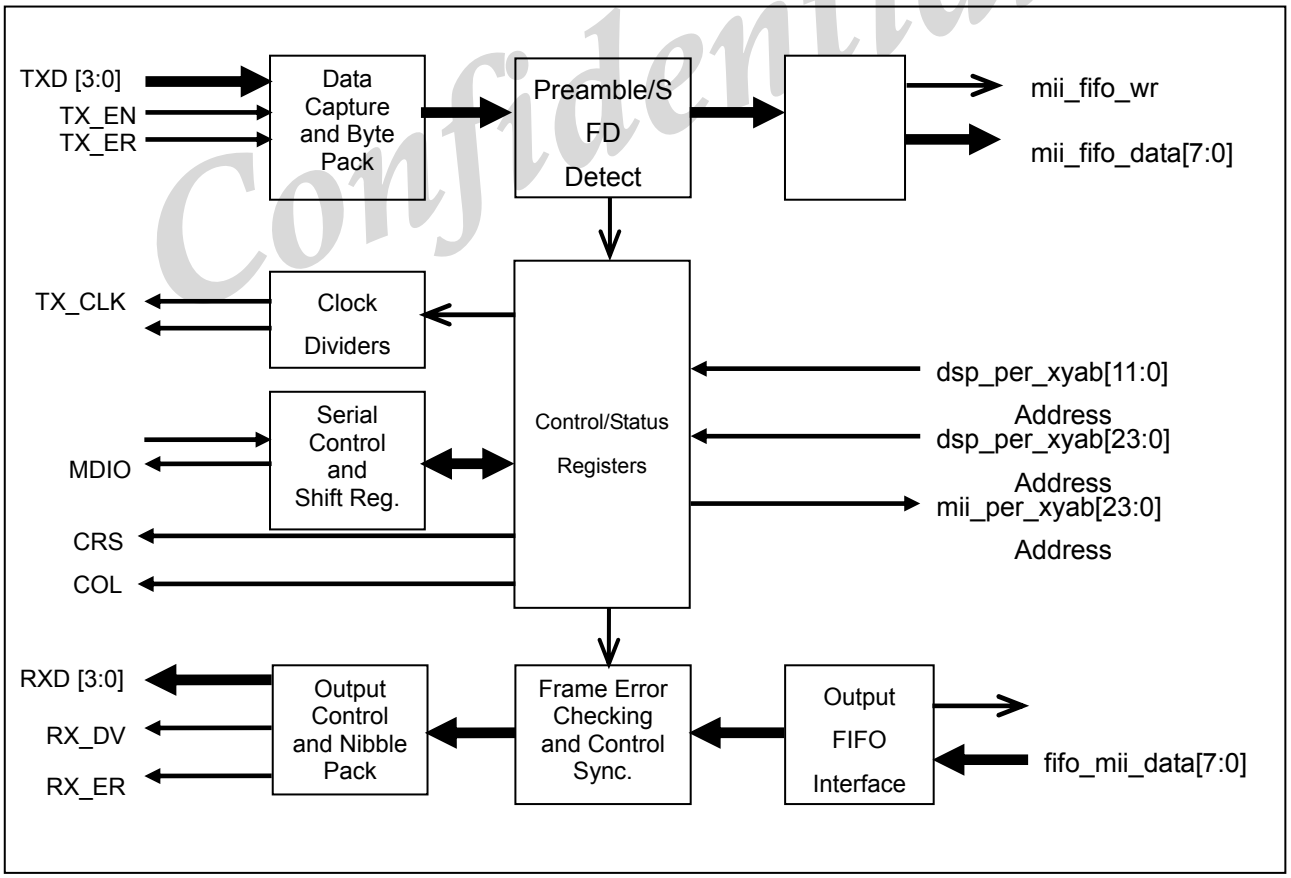

Figure 6 MII Interface Block

2-6-1 MII Operation

The data received from the Ethernet MAC on the TX interface is four bits wide. The MII module decodes the combination of UT_TXEN, UT_TXER, and UT_TXDx to determine if a valid nibble is currently on the interface. The nibble is valid if UT_TXEN is asserted even when UT_TXER is also asserted. The interface packs each pair of input nibbles into a byte (least significant nibble first in time) for use by the framing logic and FIFO interface. The number of nibbles in an Ethernet frame will normally be even so that all bytes are fully packed.

Leads	Description
UT_TXD[3:0]	Nibble transmit data (clocked on positive edge of TX_CLK)
UT_TXEN	Transmit framing (clocked on positive edge of TX_CLK)
UT_TXSOC/UT_TXER	Transmit coding error (clocked on positive edge of TX_CLK)
UT_RXD[3:0]	Nibble receive data (clocked on negative edge of RX_CLK)
UT_RXEN/UT_RXDV	Receive data valid (clocked on negative edge of RX_CLK)
UT_RXSOC/UT_RXER	Receive error (clocked on negative edge of RX_CLK)
UT_TXCLAV/UT_CRS	Carrier sense (asynchronous signal)
UT_RXCLA/UT_COL	Collision (asynchronous signal)
UT_TXCLK	25 MHz transmit clock, ±100ppm local crystal
UT_RXCLK	25 MHz receive clock, ±100ppm local or remote crystal

After the valid nibbles are packed into bytes the byte stream is checked for the Ethernet framing signals: the preamble and the Start Frame Delimiter (SFD). After UT_TXEN goes active, the MAC sends a preamble of seven bytes of 0x55 followed by one byte of 0xd5 followed by up to 1522 bytes of data. After frame detection the byte stream is sent to the aggregation function. The MAC de-asserting UT_TXEN indicates the end of an Ethernet frame.

The RX path is largely the inverse of the TX. Data is fetched from the aggregation function, and then transmitted on the RX interface one nibble at a time. The interface signaling for the RX path uses UT_RXDx, UT_RXDV, and UT_RXER. Similar to the UT_TXEN signal, the rate matching function asserts the UT_RXDV signal for the duration of a packet transfer. After UT_RXDV goes active, the PHY sends one byte of 0xd5 followed by up to 1522 bytes of data. UT_RXDV then goes inactive. While configured for half-duplex operation, this should not preclude receiving data at the same time as transmitting. Output bytes are sent over the nibble wide UT_RXD data bus least significant bits first in time while UT_RXDV is active. The DSP has control of the UT_RXER signal via a register bit and the MII module synchronizes this signal to the interface and frame timing as necessary. This indicates the PHY has detected a data error in the current frame. An error is to be propagated by the MAC into the current frame being sent.

The carrier sense signal (CRS) is inactive in the idle state. It goes active in the 320 ns preamble period following UT_TXEN. Normally it would indicate when the Ethernet is actively passing information, local or

another device. Since the MAC knows not to attempt to send a frame when another device is using the Ethernet, CRS is used to flow control the transmit data from the MAC. CRS is not returned to the inactive state until the PHY is prepared to accept another 1522 byte frame. Alternatively, the interface can use pause frames for flow control.

The collision signal (COL) is set when the PHY detects multiple devices transmitting at once. Typically this is used to get the MAC to retransmit a frame after a delay period while the PHY jams the Ethernet until detection of a collision causes both devices to drop carrier. Both back off and try again after a delay period. The 320 ns preamble gives the PHY time to detect a collision and report it.

UT_TXCLK and UT_RXCLK are asynchronous signals for a VDSL PHY. VDSL operates on its own time base. These clocks are only used as a means of communicating with the MAC. These clocks are tied to together and provided as a common input/output for MT2201.

The DSP can also control the RXD data bus via MII module register bits. This control allows the DSP to send the False Carrier Indication (UT_RXDV=0, UT_RXER=1, UT_RXD[0,3]=1110) to the external Ethernet MAC.

2-6-2 SMII Operation

The Serial Media Independent Interface (SMII) provides all functions equivalent to the MII interface without the overhead of the external wiring of the more parallel form of the interface. This section describes all the differences between SMII and MII interfaces for the signals, functionalities, and other specific information related to the SMII operation.

The data received from the Ethernet MAC on the TX interface is bit serial, eight bits of data and two status bits: TX_EN and TX_ER. Using TX_SYNC for frame alignment the SMII module converts the serial data (least significant bit first in time) to 10-bit parallel data. The TX_EN bit determines if a valid byte is currently available. The byte is valid if TX_EN is asserted even when TX_ER is also asserted. The framing logic passes valid bytes to the FIFO interface.

If TX_ER is asserted while TX_EN is also active the MAC is indicating that there is an error in the current Ethernet packet. The SMII module stores this error condition in the high bit of the next tag register. It can also generate an interrupt for this condition. The error is propagated into the current frame being sent. The second CRC byte (FCS in the encoder) is complemented to indicate an error frame. When the TX_EN bit is not active both TXD and TX_ER are ignored.

The valid byte stream process remains similar to the MII interface.

The RX path is largely the inverse of the TX. As with the MII module, the SMII module indicates the PHY has detected a data error in the idle status following an active frame. Status indicated by the eight data bits when

the link is idle (RX_DV = 0):

RXD0 - RX_ER from previous frame

RXD1 - always 1 = 100 Mbps

RXD2 - full-duplex operation programmable under software control

RXD3 - link active state of the interface (channel specific)

RXD4 - always 0 = jabber OK

RXD5 - always 1 = upper nibble valid

RXD6 - always 0 = false carrier not detected

RXD7 - always 1

The 125 MHz TX_CLK (for SMII) is supplied externally on the UT_TXEN lead (for MII) to prevent unusual amounts of clock skew.

Received data and control information are signaled in ten bit segments. In 100 MBit mode, each segment represents a new byte of data. As defined in the 802.3 EFM standard, there is no 10 Mbit support.

2-6-3 SOURCE Synchronous MII (SSMI)

The Source Synchronous Serial Media Independent Interface (SSMII) provides all functions equivalent to the SMII interface but using 6 signals for systems requiring trace delays longer than 1 ns. This section describes all the differences between SMII and MII interfaces for the signals, functionalities, and other specific information related to the SMII operation.

Leads	Description
TXD[3:0]	Four Serial transmit data (clocked on positive edge of TX_CLK)
TX_STNC/UT_TXSOC	Transmit sync (clocked on positive edge of TX_CLK)
TX_CLK/UT_TXEN	125 MHz transmit clock through remote crystal
RXD[3:0]	Four Serial received data (output on positive edge of TX_CLK)
RX_SYNC/UT_RXSOC	Received sync (regenerated on positive edge of TX_CLK)
RX_CLK/UT_RXEN	125 MHz regenerated, delayed clock of the TX_CLK

Received and Transmit data and control information are signaled in ten bit segments as for SMII. The 125 MHz TX_CLK (for SMII) is supplied externally on the UT_TXEN lead (for MII) to prevent unusual amounts of clock skew. RX_CLK is a buffered version of TX_CLK, hence delayed slightly when looped back to the MAC.

RX_SYNC is regenerated and clocked out synchronously with RXD.

2-6-4 Other Ethernet Related Operations

Falcon also has support for four SMII (4 leads) or SSMII (6 leads) interfaces. These four serial interfaces are used for the four ports in VDSL Low speed mode, or ADSL2/2+ mode or may be used as a fast path and slow path interface on up to two VDSL or ADSL2/2+ ports. The TC sub-layer uses a 65th sync byte for every 64 bytes transmitted to encapsulate the framed data. The TC sub-layer also includes a G(x) = 1 + x^39 + x^58 scrambler/descrambler combination. Protocol is incorporated for mapping the following data types: idle, in-frame, idle->in-frame, in-frame->idle, in-frame->idle->in-frame. For packets containing data a 32-bit CRC is appended. After coding the byte stream is written to the input FIFO. This FIFO is located outside of the MII module because it is shared with the UTOPIA interface.

The RX path is largely the inverse of the TX. Data is fetched from the output FIFO and passed through a decoder. Sync byte detection is performed in the receive path according to a well-defined state machine. The transmit path uses a 64-byte pipeline.

The serial control portion of the MII module implements the management data interface defined in the IEEE Std 802.3 specification. This interface supports dual standard clause 22 and clause 45 operations. Clause 22 is considered to be obsolete, but is included for backwards compatibility with older equipment. This standard defines a Management Data Input/Output (MDIO) interface between Station Management (STA) devices and the sub-layers that form the Physical Layer (PHY). The sub-layers are composed of individually manageable entities known as MDIO Manageable Devices (MMDs). The management data interface uses a data frame to transmit read or write commands to the PHY and to receive response data for reads. Control information is sent by STA in the initial portion of a management frame that determines the data transaction type to execute. The PHY can only return status or accept command as requested by the STA. Protocols must be defined to accomplish the reverse. Three fields control the type of transaction:

OP - the op-code (refer to clause 22/45 for definition)

PRTAD (PHYAD) - the port address (or clause 22 physical address)

DEVAD (REGAD) - the device address (or clause 22 register address)

The MII block is equipped with a low-power gated clock mode. Setting the soft reset bit of the CSR will gate off the clock for the module and reset all logic. This capability is useful for reducing power consumption when the Falcon device's host interface is through UTOPIA or the parallel port.

The MII module uses a gated and non-gated version of the DSP clock. The gated version is provided for low power mode and drives all logic except for the CSR register. The non-gated clock is used to drive the CSR register. The CSR must always be active so that it can enable the rest of the logic on command from the DSP

The MII interface uses two clocks: MDC and MII_CLK. The MDC clock is asynchronous to the system clock; however, its minimum period (400 ns) is much longer than the system clock (7ns). Therefore, the clock is sampled by the system clock for the purpose of capturing data on the MDIO lead and no MDC clock domain is needed.
The MII_CLK is 25 MHz and is also asynchronous to the system clock. Clause 22 specifies the synchronous rx signals be valid ±10 ns with respect to the rising edge of the rx clock. By clocking on the negative edge of a relatively square input clock we guarantee proper operation for clock frequencies up to 35 MHz. The MII_CLK is double delayed and differentiated for both positive and negative edge. Double delayed input data is captured on the positive edge. Output data is supplied on the negative edge. The module also includes a hard and soft reset. A CTL bit controls soft reset and doubles as the clock gating signal.

2-7 UTOPIA Interface

Falcon-UTOPIA Interface implements UTOPIA Level 2, AF-Phy-0039, with Cell rate decoupling feature.

Leads	Description
UT_TXCLK	UTOPIA Transmit clock
UT_RXCLK	UTOPIA Receive clock
UT_TXEN	Indicates UTOPIA Transmit data enable: Txenb
UT_TXSOC	UTOPIA Transmit start of cell: Txsoc
UT_TXD [3:0]	UTOPIA Transmit data bus input LSB txdata[3:0]
UT_TXCLAV	UTOPIA Transmit Cell Available: Txclav
UT_RXCLAV	UTOPIA Receive Cell Available: Rxclav
UT_RXEN	Indicates UTOPIA Receive data enable: Rxenb
UT_RXSOC	UTOPIA Receive start of cell: Rxsoc
UT_RXD [3:0]	UTOPIA Receive data bus output LSB rxdata[3:0]
UT_TXREF	UTOPIA Transmit Reference signal: Txref
UT_RXREF	UTOPIA Receive Reference signal: Rxref
UT_TXADD[4:0]	UTOPIA Transmit PHY Address
UT_RXADD[4:0]	UTOPIA Receive PHY Address
UT_TXD [7:4]	UTOPIA Transmit data bus input MSB txdata [7:4]
UT_RXD [7:4]	UTOPIA Receive data bus output MSB rxdata [7:4]

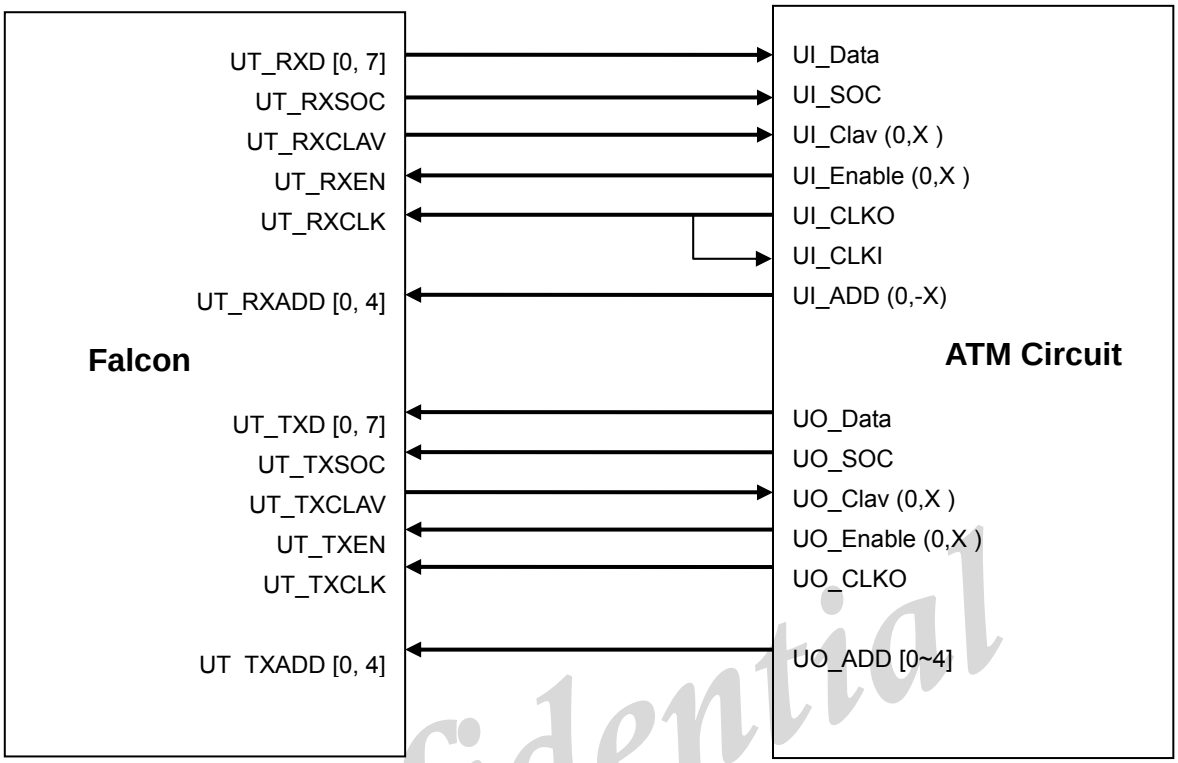

Figure 7 UTOPIA Connection between Falcon and ATM Layer Devices

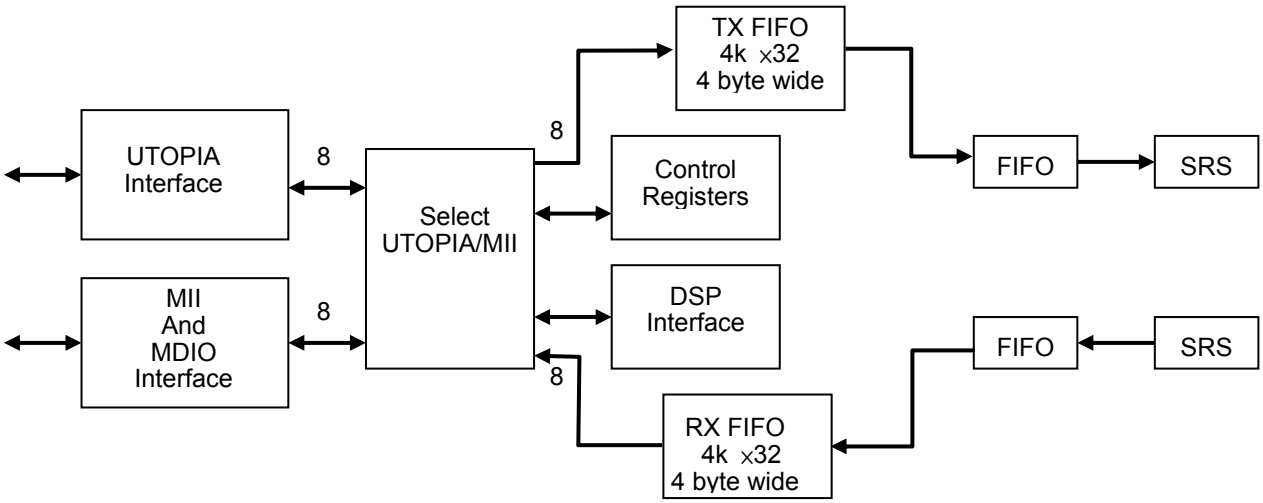

Figure 8 UTOPIA and Ethernet Submodule Interconnections

The ATM layer controls both the Transmit and Receive interface. The ATM layer provides an interface clock to the PHY layer for synchronizing all interface transfers.

The ATM transmit block generates all output signals on the rising edge of the TxClk. Signals TxData, TxSOC, and TxPrty are sampled on the rising edge of TxClk.

PHY layer indicates it can accept data using the TxClav signal, then the ATM layer drives data onto TxData and asserts (active low) TxEnb. The PHY layer controls the flow of data via the TxClav signal.

The ATM layer polls the TxClav status of a MPHY port by placing its address on TxAddr. The MPHY port (device) drives TxClav during each cycle following one with its address on the TxAddr lines. The ATM layer selects a MPHY port for transfer by placing the desired MPHY port address onto TxAddr, when TxEnb is de-asserted during the current clock cycle, and asserted during the next clock cycle.

The ATM receive block generates all output signals on the rising edge of the RxClk. Signals RxData, RxSOC, and RxPrty are sampled on the rising edge of RxClk. The PHY layer indicates it has valid data using the RxClav signal. Then the ATM layer asserts (active low) RxEnb to read this data from the PHY layer. The PHY layer controls the data flow via RxClav signal.

The ATM layer polls the RxClav status of a MPHY port by placing its address on RxAddr. The MPHY port (device) drives RxClav during each cycle following one with its address on the RxAddr lines. The ATM layer selects a MPHY port for transfer by placing the desired MPHY port address onto RxAddr, when RxEnb is disserted during the current clock cycle, and asserted during the next clock cycle.

2-8 Serial Port Interface

The Serial Port Interface (SPI) provides multiple ports that can be used for various purposes. An example is the use of the Serial Port 0-3 for interfacing the Falcon with some type of AFE All these ports are full-duplex serial ports with a lot of flexibility in their programming for communicating with a variety of serial devices.

All Serial Ports comprise independent transmitter and receiver sections and a common serial clock generator.

2-8-1 Serial Port Rates

The Serial Port interface maximum communication rate is 1/4 of the master clock. As the Falcon can operate up to 150 MHz (see “UTOPIA Interface” section), then the max rate is 37.5Mbit per second. All Serial Port Interfaces need four system clocks to operate on a single bit of data. The slowest rate is equal to the maximum frequency divided by 4096, meaning 36.6Kbit per second in case of a 150 MHz operation.

2-8-2 Serial Port Operation

Words transferred by the SCI are characterized by word length, shift direction, and word alignment. This section describes these characteristics and the programming associated with them.

2-8-3 Word Length

The Serial Port provides full control of the number of bits per word or the word length. The SCI transmit and receive data registers are 24-bits long, so 32-bits words cannot be transmitted or received. For 32-bit words, the first 24 bits contain valid data and the last bits are not defined.

2-8-4 Shift Direction

The Serial Port presents two options for shift direction: most significant bit (MSB) first or least significant bit (LSB) first. To select shift direction, set bit 6 in Control Register B, SHFD. If SHFD is set, the data is shifted into the receive shift register from the SRD lead and out of the transmit shift register to the STD lead with the LSB first. If SHFD is clear, the data is shifted into the receive shift register from the SRD lead and out of the transmit shift register to the STD lead with the MSB first.

2-8-5 Synchronization Signals

Because the Serial Port is a synchronous interface, it requires clock and frame sync signals to define when the data changes and when a new frame begins. In certain modes, the Serial Port also has the option of two flag signals to use for device selection.

2-8-6 Synchronous versus Asynchronous

The Serial Port includes both synchronous and asynchronous modes. In synchronous mode, the transmitters and receiver use the same clock and frame sync; in asynchronous mode, the transmitters and receiver use different clocks and frame syncs. The Serial Port data transfers are synchronized to a clock in both modes. The choice of synchronous versus asynchronous mode is determined by API command. Setting SYN puts the Serial Port is in synchronous mode; clearing SYN puts it in asynchronous mode.

In synchronous mode: SCK is an input or an output that both the transmitter and receiver use as the clock signal. SC2 is an input or an output that both the transmitter and receiver use as the frame sync signal. SC0 and SC1 can be used as flag signals.

2-8-7 In Asynchronous Mode

SCK is an input or an output that the transmitter uses as the clock signal.

SC2 is an input or an output that the transmitter uses as the frame sync signal.

SC0 is an input or an output that the receiver uses as the clock signal.

SC1 is an input or an output that the receiver uses as the frame sync signal.

The direction of the SC0, SC1, SC2, and SCK leads is determined by the SCD0, SCD1, SCD2, and SCKD bits, respectively, CRB [3:0]. If one of these bits is clear, the corresponding lead is an input. If one of these bits is set, the corresponding lead is an output.

2-8-8 Serial Clock

SCK's direction can be controlled via API command.

2-8-9 Frame Sync

The frame sync signal indicates when a new frame begins. In synchronous mode, the SC2 lead is the frame sync for the receiver and transmitter. In asynchronous mode, SC2 is the frame sync signal for the receiver and SC0 is the frame sync signal for transmitter 0.

Frame sync is generated only when data is ready to be transmitted, i.e., data is written to a transmit data register. This mode requires that the transmit frame sync be internal (output) and the receive frame sync be external (input) for proper operation. Transmit underruns are impossible in on-demand mode because there are no transmit time slots, thus transmit underruns are disabled.

2-8-10 Flags

When the Serial Port is in synchronous mode, the SC0 and SC1 leads are available for use as flags

2-8-11 SPI Protocol: Clock Stop Mode

A system conforming to this protocol has a master-slave configuration. SPI protocol is a 4-wire interface composed of serial data in (master in slave out), serial data out (master out slave in), shift clock (SCK), and an active (low) slave enable signal. Communication between the master and the slave is determined by the presence or absence of the master clock. Data transfer is initiated by the detection of the master clock and is terminated on absence of the master clock. The slave has to be enabled during this period of transfer. When the SPI is the master, the slave enable is derived from the master transmit frame sync pulse, SC2.

The clock stop mode of the Serial Port provides compatibility with the SPI protocol. The SPI supports two SPI transfer formats specified by the clock stop mode field (CKST) in Control Register B. The clock stop mode in conjunction with the CKP bit allows serial clocks to be stopped between transfers using one of four possible timing variations.

2-8-12 SPI Protocol: Start Bit Mode

Some devices require a start bit to indicate the arrival of a data frame. When configured in this mode (SBIT = 1 in Control Register B) an active low start bit precedes the data followed by an active high stop bit. No frame sync is required since the receiving device frames the data. The word length control (WL [4:0]) is adjusted to specify the number of bits.

2-9 Host Port Interface

The host port interface (HPI) is an eight/sixteen bit parallel interface with a DMA control. The HPI supports both master and slave operation. The HPI can interface with most of the Microprocessor and DSP available on the market with no external components

The Host Port implementation is a Master or Slave mode transferring a message length of up to 512 bytes per transaction.

Falcon employs a message interface API for command and response. The command and response message format uses HDLC-like framing, similar to the one used in G.997.1. Each command is followed by an acknowledge response typically within 1 ms. If a command is not acknowledged within 10 ms the command can be assumed to be not understood or some other error condition preventing the command can be assumed. Some commands will be acknowledged and then will be followed by a status frame sent from Falcon to the host at a later time.

2-10 Boundary Scan (JTAG) Operation

When boundary scan testing is not being performed, the boundary scan register is transparent, allowing the input and output signals at the device leads to pass to and from the device's internal logic. During boundary scan testing, the boundary scan register disables the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. Data is read out from internal test registers LSB first.

The following boundary scan test instructions are supported

-SAMPLE/PRELOAD
-BYPASS
-IDCODE
-EXTEST

EXTEST Test Instruction: One of the required boundary scan tests is the external boundary test (EXTEST) instruction. When this instruction is shifted in, the device is forced into an off-line test mode. While in this test mode, the test bus can shift data through the boundary scan registers to control the external input and output leads. The MT2201 is NOT held in Reset.

SAMPLE/PRELOAD Test Instruction: When the SAMPLE/PRELOAD instruction is shifted in, the device remains fully operational. While in this test mode, input data, and data destined for device outputs, can be captured and shifted out for inspection. The data is captured in response to control signals sent to the TAP controller.

BYPASS Test Instruction: There is no explicit decode for bypass instruction. It is always selected by default. Thus any invalid instruction opcode will map to the bypass instruction. When the BYPASS instruction is shifted in, the device remains fully operational. While in this test mode, a scan operation will transfer serial data from the TDI input, through an internal scan cell, to the TDO lead. The purpose of this instruction is to abbreviate the scan path through the circuits that are not being tested to only a single clock delay.

IDCODE Instruction: When the IDCODE instruction is shifted in, the device remains fully operational. The purpose of this instruction is to output the device ID code register on the TDO lead.

3 Pin Description

3-1 LQFP 128 Pin Description

Pin	Symbol	Pad Type	Description
1	TCK	I/O	ONCE/JTAG Test Clock
2	TRSTn	Ipu	ONCE/JTAG Reset
3	EX_D23	I/O	Ext Memory Data 23/Host Port Data 15/GPIO
4	EX_D22	I/O	Ext Memory Data 22/Host Port Data 14/GPIO
5	EX_D21	I/O	Ext Memory Data 21/Host Port Data 13/GPIO
6	EX_D20	I/O	Ext Memory Data 20/Host Port Data 12/GPIO
7	EX_D19	I/O	Ext memory data 19/Host port data 11/GPIO
8	EX_D18	I/O	Ext memory data 18/Host port data 10/GPIO
9	EX_D17	I/O	Ext memory data 17/Host port data 9/GPIO
10	EX_D16	I/O	Ext memory data 16/Host port data 8/GPIO
11	EX_D15	I/O	Ext memory data 15/Host port data 7/GPIO
12	EX_D14	I/O	Ext memory data 14/Host port data 6/GPIO
13	EX_D13	I/O	Ext memory data 13/Host port data 5/GPIO
14	EX_D12	I/O	Ext memory data 12/Host port data 4/GPIO
15	EX_D11	I/O	Ext memory data 11/Host port data 3/GPIO
16	EX_D10	I/O	Ext memory data 10/Host port data 2/GPIO
17	VDD_IO1	VDD_{IO}	VDD IO Supply
18	GND_IO1	VSS_{IO}	VSS IO Supply
19	EX_D9	I/O	Ext memory data 9/Host port data 1/GPIO
20	EX_D8	I/O	Ext memory data 8/Host port data 0/GPIO
21	VDD_D1	VDD_{CORE}	VDD Digital core supply
22	GND_D1	VSS_{CORE}	VSS Digital core supply
23	VDD_D2	VDD_{CORE}	VDD Digital core supply
24	GND_D2	VSS_{CORE}	VSS Digital core supply
25	EX_A11	I/O	Ext memory address 11/GPIO
26	VDD_IO2	VDD_{IO}	VDD IO Supply
27	GND_IO2	VSS_{IO}	VSS IO Supply
28	EX_A16	I/O	Ext memory address 16/GPIO
29	EX_A17	I/O	Ext memory address 17/GPIO
30	EX_AA3	I/O	Ext memory address attribute 3/GPIO
31	EX_AA2	I/O	Ext memory address attribute 2/GPIO
32	EX_AA1	I/O	Ext memory address attribute 1/GPIO
33	EX_AA0	I/O	Ext memory address attribute 0/GPIO
34	RESETn	I/O	Master Reset
35	HP_DY	I/O	Host port slave ready
36	HP_RDWRn	I/O	Host port read/write#
37	HP_CS	I/O	Host port chip select

Pin	Symbol	Pad Type	Description
38	HP_DS	I/O	Host port data strobe
39	TSTMODE	I	Test mode-scan mode enable
40	IRQA	I	External Interrupt A/Test mode 0 lead strap
41	IRQB	I	External Interrupt B/Test mode 1 lead strap
42	IRQC	I	External Interrupt C/Test mode 2 lead strap
43	IRQD	I	External Interrupt D/Test mode 3 lead strap
44	VDD_D3	VDD_{CORE}	VDD Digital core supply
45	GND_D3	VSS_{CORE}	VSS Digital core supply
46	NMI	I	Non-maskable interrupt/PLL Bypass lead strap
47	VDD_IO3	VDD_{IO}	VDDD IO Supply
48	GND_IO3	VSS_{IO}	VSS IO Supply
49	GND_PLL	VSS_{PLL}	VSS PLL Supply
50	VDD_PLL	VDD_{PLL}	VDD PLL Supply
51	XTALI	I	Master crystal oscillator input
52	XTALO	O	Master crystal oscillator output
53	VDD_D4	VDD_{CORE}	VDD Digital core supply
54	GND_D4	VSS_{CORE}	VSS Digital core supply
55	ACK0	I	AFE Interface clock 0
56	ATXD15	O	AFE Interface transmit data 15
57	ATXD14	O	AFE Interface transmit data 14
58	ATXD13	O	AFE Interface transmit data 13
59	ATXD12	O	AFE Interface transmit data 12
60	ATXD11	O	AFE Interface transmit data 11
61	ATXD10	O	AFE Interface transmit data 10
62	ATXD9	O	AFE Interface transmit data 9
63	ATXD8	O	AFE Interface transmit data 8
64	ATXD7	O	AFE Interface transmit data 7
65	ATXD6	O	AFE Interface transmit data 6
66	ATXD5	O	AFE Interface transmit data 5
67	ATXD4	O	AFE Interface transmit data 4
68	ATXD3	O	AFE Interface transmit data 3
69	ATXD2	O	AFE Interface transmit data 2
70	ARXD2	I	AFE Interface receive data 2
71	ARXD3	I	AFE Interface receive data 3
72	ARXD4	I	AFE Interface receive data 4
73	ARXD5	I	AFE Interface receive data 5
74	ARXD6	I	AFE Interface receive data 6
75	ARXD7	I	AFE Interface receive data 7
76	ARXD8	I	AFE Interface receive data 8
77	GND_D5	VSS_{CORE}	VSS Digital core supply

Pin	Symbol	Pad Type	Description
78	VDD_D5	VDD_{CORE}	VDD Digital core supply
79	ARXD9	I	AFE Interface receive data 9
80	ARXD10	I	AFE Interface receive data 10
81	ARXD11	I	AFE Interface receive data 11
82	ARXD12	I	AFE Interface receive data 12
83	ARXD13	I	AFE Interface receive data 13
84	ARXD14	I	AFE Interface receive data 14
85	GND_IO4	VSS_{IO}	VSS IO Supply
86	VDD_IO4	VDD_{IO}	VDDD IO Supply
87	ARXD15	I	AFE Interface receive data 15
88	ACK2	I	AFE Interface clock 2
89	ASYNC2	I	AFE Interface frame sync 2
90	GND_D6	VSS_{CORE}	VSS Digital core supply
91	VDD_D6	VDD_{CORE}	VDD Digital core supply
92	SRDA	I/O	SPI Serial port A receive data/GPIO
93	SCKA	I/O	SPI Serial port A clock
94	STDA	I/O	SPI serial port A transmit data/GPIO
95	SRDB	I/O	SPI serial port B receive data/GPIO
96	SCKB	I/O	SPI serial port B clock
97	STDB	I/O	SPI serial port B transmit data/GPIO
98	SC2B	I/O	SPI serial port B control 2/GPIO
99	MII_XTALI	I	MII crystal oscillator input
100	MII_XTALO	O	MII crystal oscillator output
101	UT_TXD0/ET XD0	I	UTOPIA/MII transmit data 0/SMII transmit data 0
102	UT_TXD1/ET XD1	I	UTOPIA/MII transmit data 1/SMII transmit data 1
103	UT_TXD2/ET XD2	I	UTOPIA/MII transmit data 2/SMII transmit data 2
104	UT_TXD3/ET XD3	I	UTOPIA/MII transmit data 3/SMII transmit data 3
105	GND_D7	VSS_{CORE}	VSS Digital core supply
106	VDD_D7	VDD_{CORE}	VDD Digital core supply
107	UT_TXEN/SMIITX_CLK	I	UTOPIA/MII transmit Enable/SMII TX CLK
108	UT_TXCLAV	O	UTOPIA TX cell Available/MII carrier sense
109	UT_TXSOC	I	UTOPIA TX start of Cell/MII TX error/SMII TX SYNC
110	UT_TXCLK/MIITX_CLK	I/O	UTOPIA TX clock (I)/MII TX clock (O)
111	UT_TXREF	I	UTOPIA TX timing reference/MII MDC
112	UT_RXEN/SMIIRX_CLK	I/O	UTOPIA RX enable (I)/MII RX data valid (O)/SMII RX CLK (I)
113	UT_RXCLAV	O	UTOPIA RX cell Available/MII Collision
114	GND_IO5	VSS_{IO}	VSS IO Supply
115	VDD_IO5	VDD_{IO}	VDD IO Supply
116	UT_RXSOC	O	UTOPIA RX start of Cell/MII RX error/SMII RX SYNC
117	UT_RXCLK/MIIRX_CLK	I/O	UTOPIA RX Clock (I)/MII RX Clock (O)

Pin	Symbol	Pad Type	Description
118	UT_RXREF	I/O	UTOPIA RX Timing Reference (O)/MII MDIO
119	GND_D8	VSS_{CORE}	VSS Digital Core Supply
120	VDD_D8	VDD_{CORE}	VDD Digital Core Supply
121	UT_RXD3/NET_RXD3	O	UTOPIA/MII Receive Date 3/SMII Receive Data 3
122	UT_RXD2/NET_RXD2	O	UTOPIA/MII Receive Date 2/SMII Receive Data 2
123	UT_RXD1/NET_RXD1	O	UTOPIA/MII Receive Date 1/SMII Receive Data 1
124	UT_RXD0/NET_RXD0	O	UTOPIA/MII Receive Date 0/SMII Receive Data 0
125	TMS	Ipu	ONCE/JTAG Test Mode Select
126	Scan_en	I	I for Internal Use Only/ Tie To Ground
127	TDI	I	ONCE/JTAG Serial Test Data In
128	TDO	O	ONCE/JTAG Serial Test Data Out

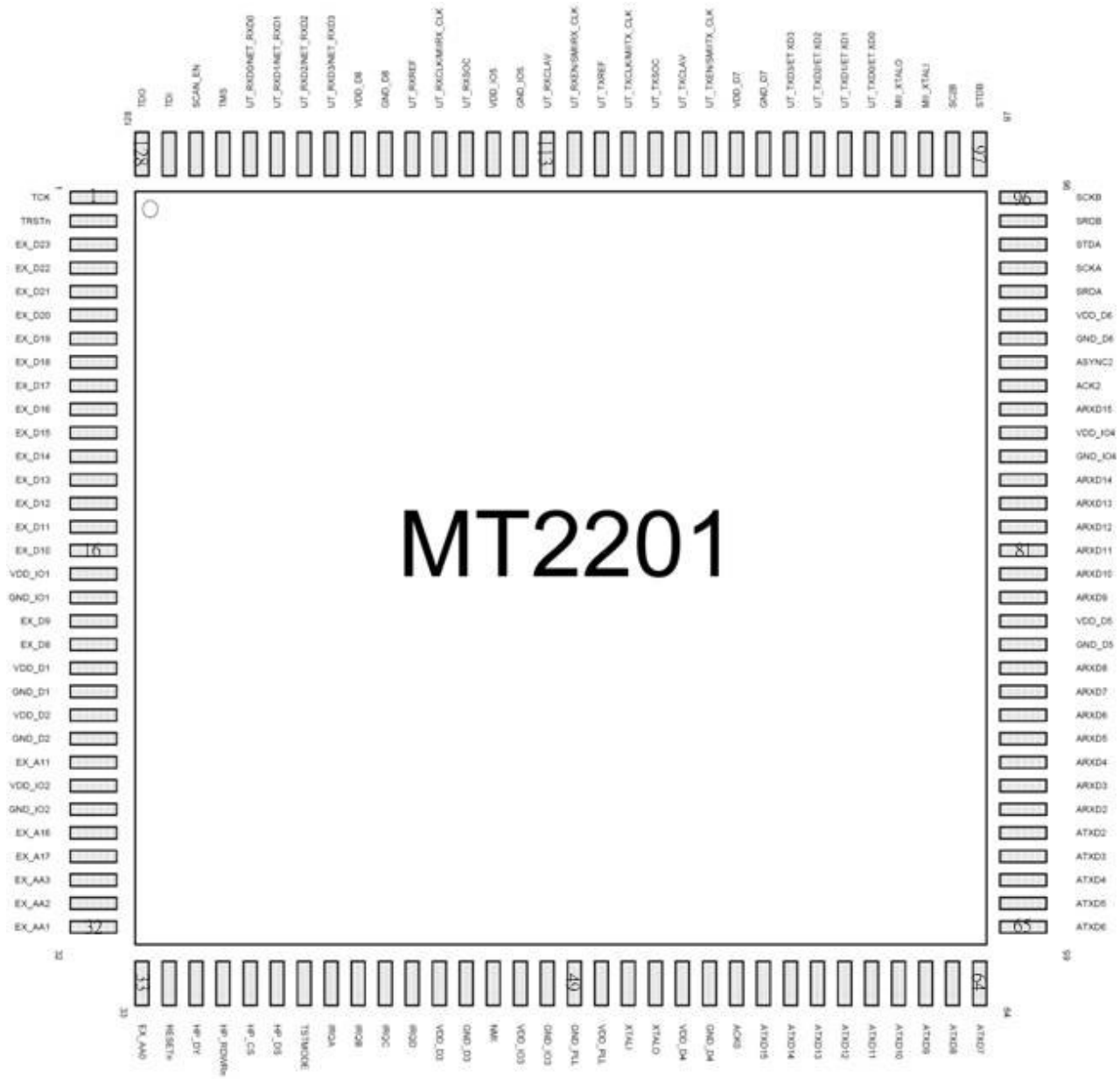

Figure 9 Pin Diagram

4 Technical Characteristics

4-1 Absolute Maximum Ratings and Environmental Limitations (REFERENCED to VSS)

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage (CMOS I/O)	$VDD_{IO/PLL}$	-0.3	3.9	V	Note 1,4
Supply voltage (Core)	VDD_{CORE}	-0.3	1.32	V	Note 1,4
DC input voltage	V_{IN}	-0.5	5.5	V	Note 1,4,5
Storage temperature range	T_S	-55	+150	℃	Note 1
Ambient operating	T_A	-40	+85	℃	0 ft/min linear airflow
Temperature	ME	5		Level	Per IPC/JEDEC
Moisture exposure level	RH	30	60	%	Note 2
Relative humidity, during assembly	RH	0	100	%	Non-condensing
ESD classification	ESD	2		kV	Note 3

Notes：

1. Operating conditions outside the min-max ranges specified may cause permanent device failure. Exposure to conditions near the min or max limits for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per JEDEC JESD22-A114-B.
4. Device core is 1.2V only.
5. Falcon is 5 V compatible in the sense that the output logic 1 (VOH) and output logic 0 (VOL) levels of the Falcon outputs have been specified at the same voltage levels that have been commonly recognized as logic 1 and logic 0 for the 5 V environment. Falcon can generally be expected to drive 5 V TTL compatible components. However, while Falcon outputs are able to meet the minimum input logic switching levels (VIH and VIL) of 5 V TTL compatible components, the output logic 1 output voltage of some 5 V components may exceed the maximum input voltage of Falcon. Depending on the technology and circuit implementation, the 5 V TTL compatible components may drive their outputs anywhere from 3 V to their VDD supply level. CAUTION: Before connecting a 5 V component to the Falcon, always check to be sure that the Maximum VOH of the 5 V device does not exceed the specified Maximum VIN listed in the table above.

4-2 Thermal Characteristics

Parameter	Min	Typ	Max	Unit	Conditions
Thermal resistance-junction to ambient		41.9		℃/W	0 ft/min linear airflow
Thermal resistance-junction to case		11.8		℃/W	0 ft/min linear airflow

4-3 Power Requirements

Parameter	Min	Typ	Max	Unit	Conditions
V_{DDIO}	2.67	3.3	3.96	V	
I_{DDIO}	20			mA	See Notes 1,2 and 3
P_{DDIO}	53.4			mW	See Notes 1,2,and 3
V_{DDPLL}	3.15	3.3	3.45	V	
I_{DDPLL}	1	1	1	mA	See Notes 1,2 and 3
P_{DDPLL}	3.2	3.3	3.5	mW	See Notes 1,2 and 3
V_{DDCORE}	1.12	1.2	1.31	V	
I_{DDCORE}	320	320	335	mA	See Notes 1,2 and 3
P_{DDCORE}	358.4	384.0	438.9	mW	See Notes 1,2 and 3
Total Power	450	450	550	mW	See Notes 1 and 2

Notes：

1 Typical values estimated with nominal voltages at 25° C.

2 All IDD and PDD values are dependent upon VDD.

3 Conditions: UTOPIA = 50 MHz, internal system clock = 150 MHz.

4-4 Input, Output and Input/Output Parameters

4-4-1 Input Parameters For LVTTL

Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	2.0			V	$3.14 \leqq V_{DD33} \leqq 3.46$
V_{IL}			0.8	V	$3.14 \leqq V_{DD33} \leqq 3.46$
Input leakage current	-10		10	μA	$V_{IN} = V_{DD33}$ or V_{SS}
Input capacitance		5		pF	

4-4-2 Input Parameters For LVTTLpu (internal pull-up resistor)

Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	2.0			V	$3.14 \leqq V_{DD33} \leqq 3.46$
V_{IL}			0.8	V	$3.14 \leqq V_{DD33} \leqq 3.46$
Input leakage current	-10		10	μA	V_{IN}= V_{DD33} or V_{SS}
Input capacitance		5		pF	

4-4-3 Output Parameters For CMOS 16mA

Parameter	Min	Typ	Max	Unit	Conditions
V_{OH}	2.4			V	1_{OH}=-16mA
V_{OL}		0.2	0.4	V	1_{OL}=16mA
I_{OL}			16.0	mA	
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
I_{OH}			-16.0	mA	
Leakage tristate	-10		10	μA	

4-4-4 Input/Output Parameters For LVTTL/CMOS 16mA

Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	2.0			V	$3.14 \leqq V_{DD33} \leqq 3.46$
V_{IL}			0.8	V	$3.14 \leqq V_{DD33} \leqq 3.46$
Input leakage current	-10		10	μA	V_{DD33}=3.46
Input capacitance		5		pF	
V_{OH}	2.4			V	1_{OH}=-16mA
V_{OL}		0.2	0.4	V	1_{OL}=16mA
I_{OL}			16.0	mA	
I_{OH}			-16.0	mA	

4-5 Timing Characteristics

This section presents the detailed timing characteristics for the Falcon in Figure 11 through Figure 22 with values of the timing parameters tabulated below each waveform diagram. Detailed timing diagrams for the Falcon device are provided in this section, with values for the timing intervals given in tables below the waveform drawings. All output times are measured with a 25 pF load capacitance for Max conditions and 5 pF load capacitance for Min conditions, unless noted otherwise. Timing parameters are measured at voltage levels of (VIH+VIL)/2 and (VOH+VOL)/2, for input and output signals, respectively. All input transition times, 10/90%, used for timing measurements are 1.0 ns for Max conditions and 0.2 ns for Min conditions.

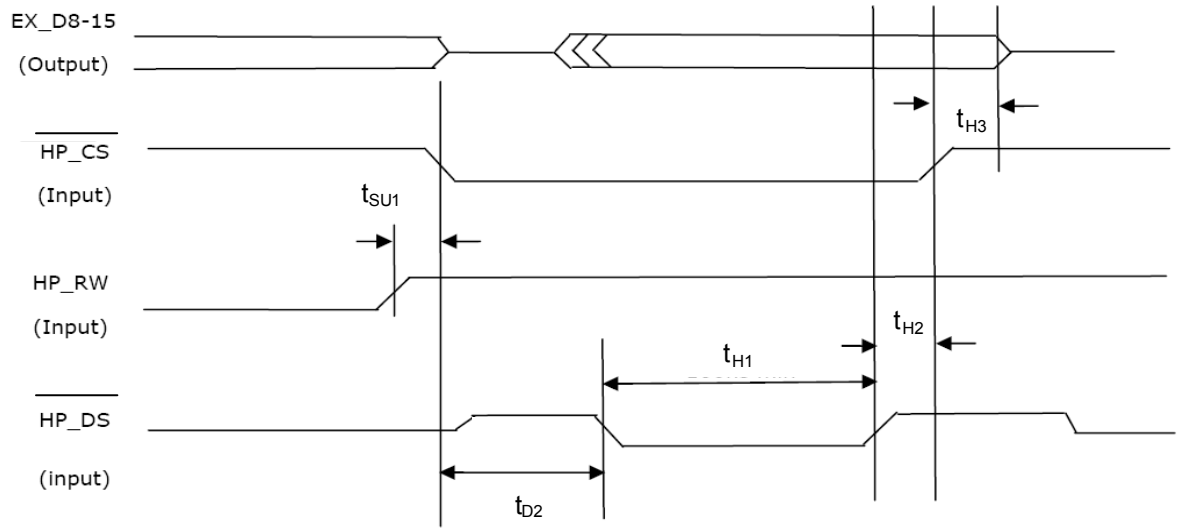

Figure 10 Host Port Read Cycle Timing

Parameter	Symbol	Min	Typ	Max	Unit
HP_RW setup to $\overline{HP\_CS}$ ↓	t_{SU1}	5.0			ns
EX_D(8-15) respond delay from $\overline{HP\_DS}$ ↓	t_{D2}	20.0			ns
$\overline{HP\_DS}$, hold time	t_{H1}	100.0			ns
$\overline{HP\_CS}$, hold from $\overline{HP\_DS}$ ↑	t_{H2}	20.0			ns
EX_D(8-15) hold from $\overline{HP\_CS}$ ↑	t_{H3}	20.0			ns

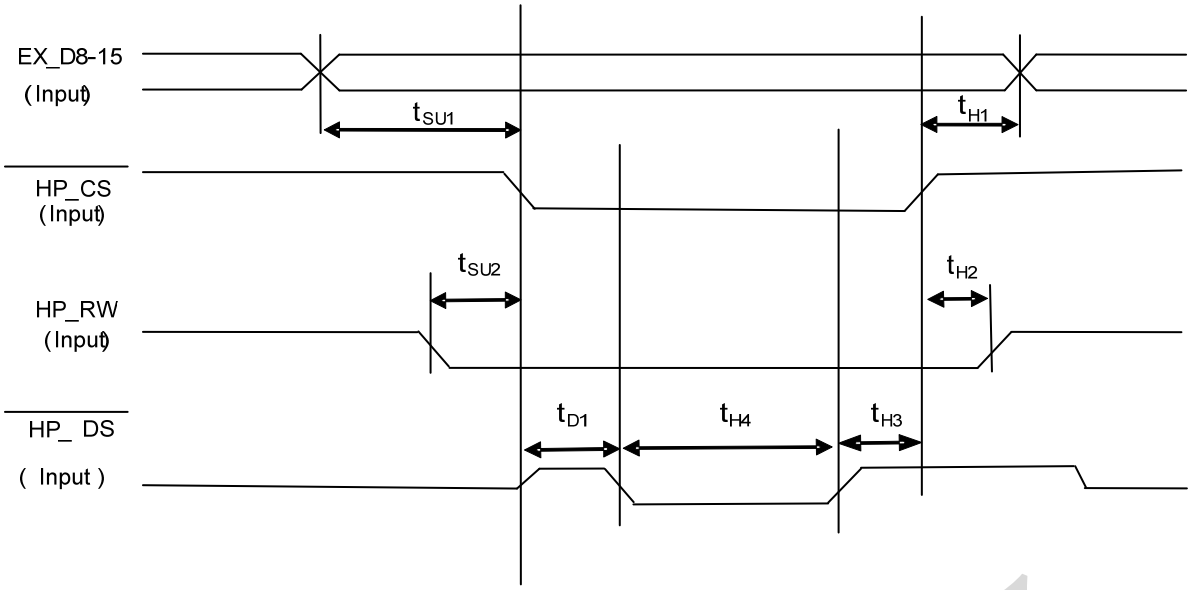

Figure 11 Host Port Write Cycle Timing

Parameter	Symbo	Min	Typ	Max	Unit
EX_D(8-15) setup to $\overline{\text{HP\_CS}}$ ↓	t_{SU1}	30.0			ns
EX_D(8-15) hold from $\overline{\text{HP\_CS}}$ ↑	t_{H1}	10.0			ns
$\overline{\text{HP\_DS}}$ delay from $\overline{\text{HP\_CS}}$ ↓	t_{D1}	20.0			ns
HP_RW setup to $\overline{\text{HP\_CS}}$ ↓	t_{SU2}	5.0			ns
HP_RW, hold from $\overline{\text{HP\_CS}}$ ↑	t_{H2}	5.0			ns
$\overline{\text{HP\_CS}}$, hold from $\overline{\text{HP\_DS}}$ ↑	t_{H3}	20.0			ns
$\overline{\text{HP\_DS}}$ hold time	t_{H4}	100.0			ns

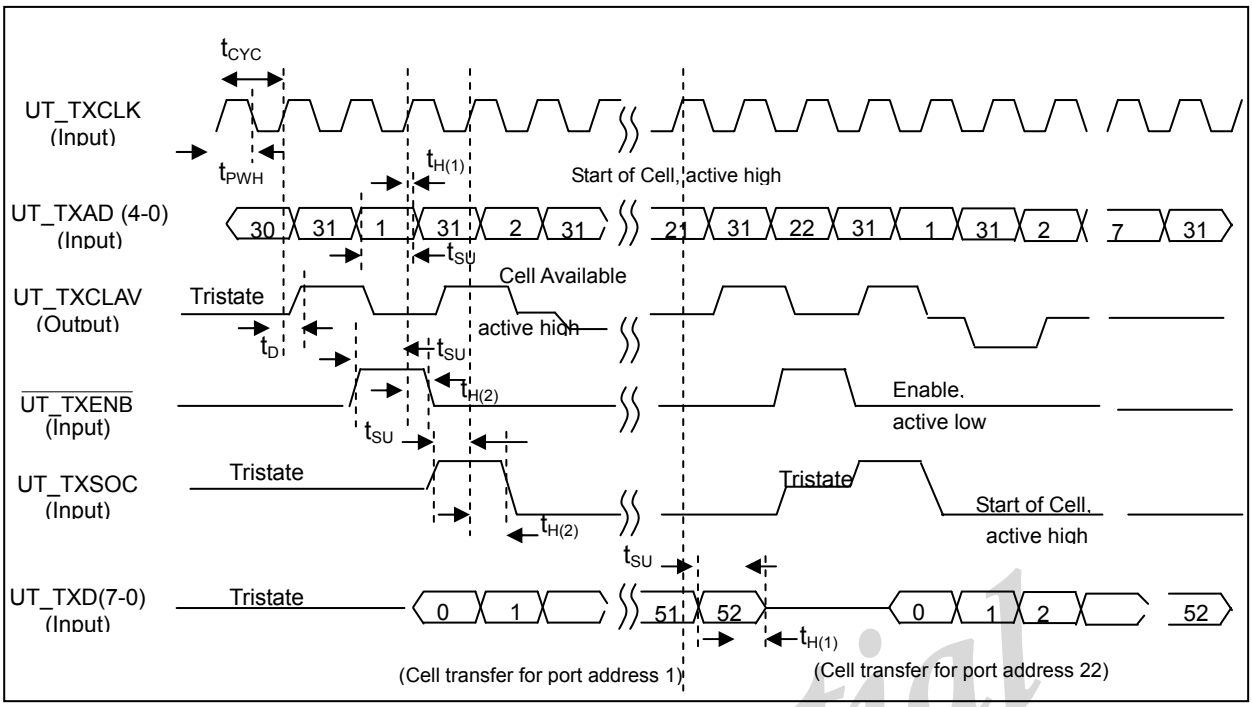

Figure 12 UTOPIA Transmit Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
UT_TXCLK clock period	t_{CYC}	20			ns
UT_TXCLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
UT_TXD(7-0), UT_TXSOC, UT_TXAD(4-0), $\overline{\text{UT\_TXENB}}$ setup time to UT_TXCLK↑	t_{SU}	4.0			ns
UT_TX D(7-0), UT_TXAD(4-0) hold time after UT_TXCLK↑	$t_{H(1)}$	1.0			ns
UT_TXSOC, $\overline{\text{UT\_TXENB}}$ hold time after UT_TXCLK↑	$t_{H(2)}$	1.0			ns
UT_TXCLAV delay from UT_TXCLK ↑	t_D	2.0		10.7	ns

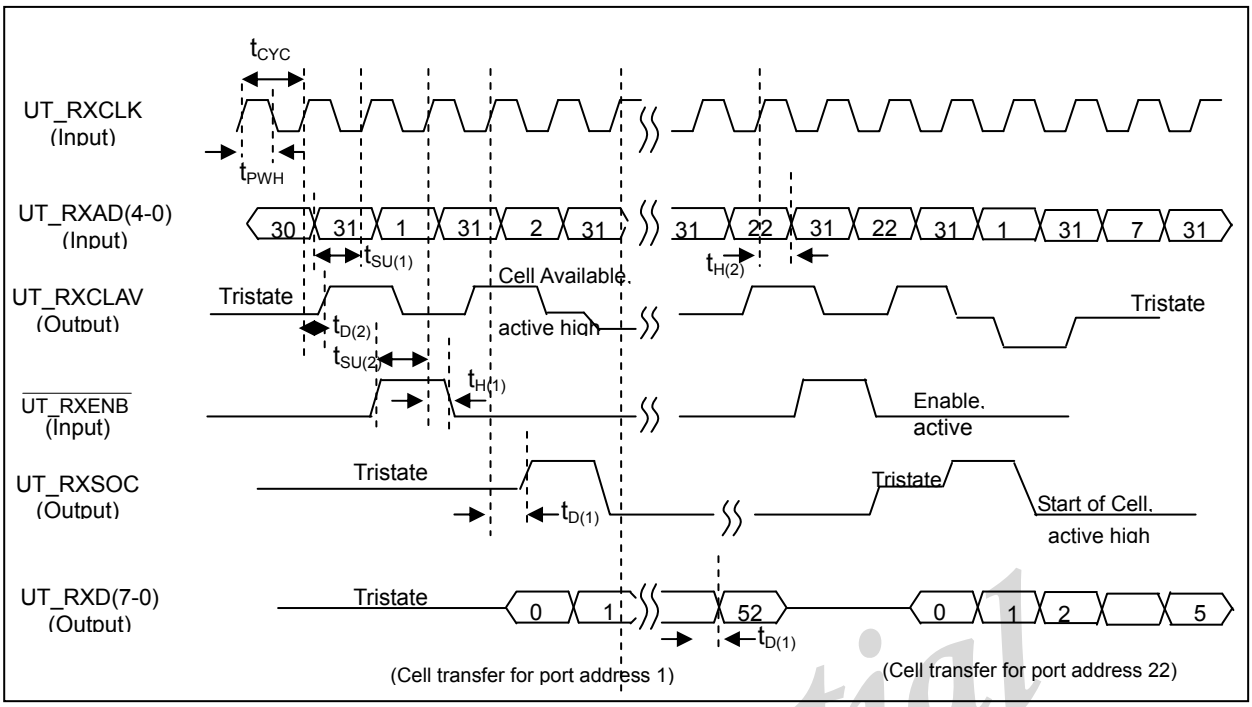

Figure 13 UTOPIA Receive Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
UT_RXCLK clock period	t_{CYC}	20			ns
UT_RXCLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
UT_RXAD(4-0), setup time to UT_RXCLK↑	$t_{SU(1)}$	4.0			ns
UT_RXD(7-0), UT_RXSOC delay from UT_RXCLK↑	$t_{D(1)}$	2.0		10.0	ns
$\overline{\text{UT\_RXENB}}$ hold time after UT_RXCLK↑	$t_{H(1)}$	1.0			ns
UT_RXAD(4-0) hold time after UT_RXCLK↑	$t_{H(2)}$	1.0			ns
$\overline{\text{UT\_RXENB}}$ setup time to UT_RXCLK↑	$t_{SU(2)}$	4.75			ns
UT_RXCLAV delay from UT_RXCLK ↑	$t_{D(2)}$	2.0		10.5	ns

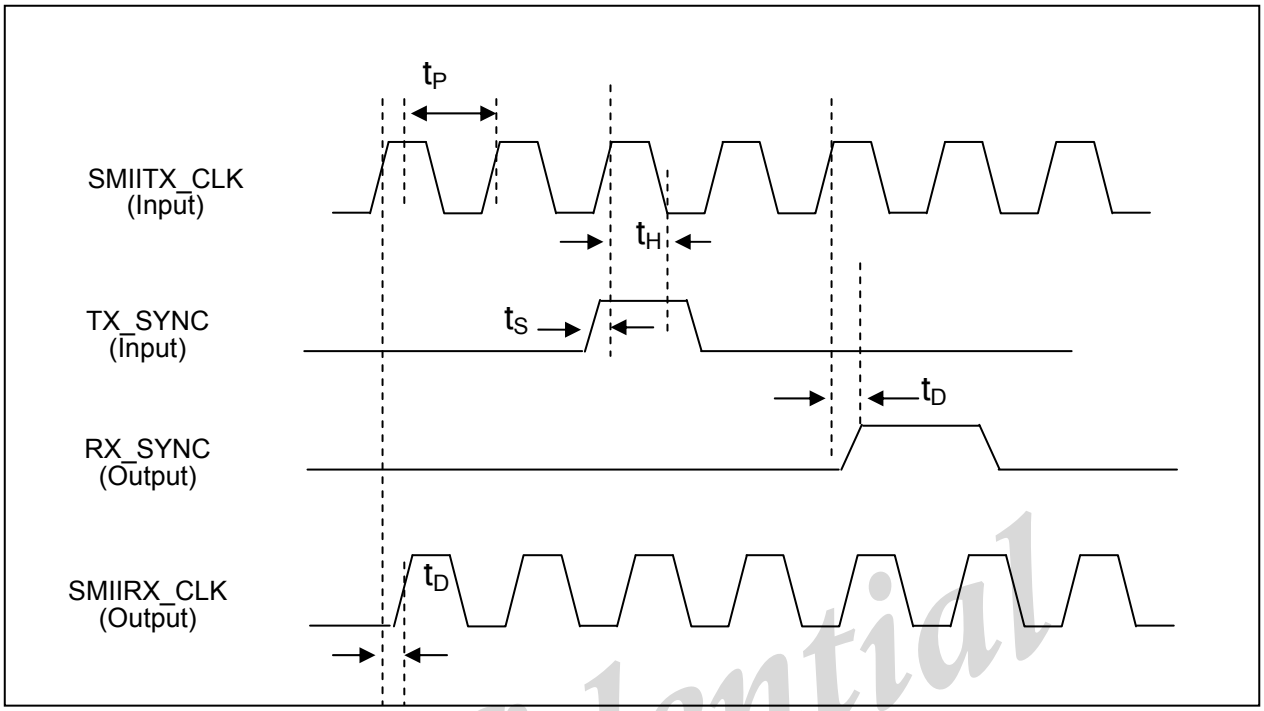

Figure 14 SMII Sync In/Out Timing

Parameter	Symbol	Min	Typ	Max	Unit
SMIITX_CLK and SMIIRX_CLK period	t_P		8.0		ns
SMIITX_CLK and SMIIRX_CLK duty cycle		40		60	%
TX_SYNC setup time to SMIITX_CLK↑	t_S	1.5			ns
TX_SYNC hold time from SMIITX_CLK↑	t_H	1.0			ns
RX_SYNC/SMIIRX_CLK delay from SMIITX_CLK↑	t_D	1.5		4.5	ns

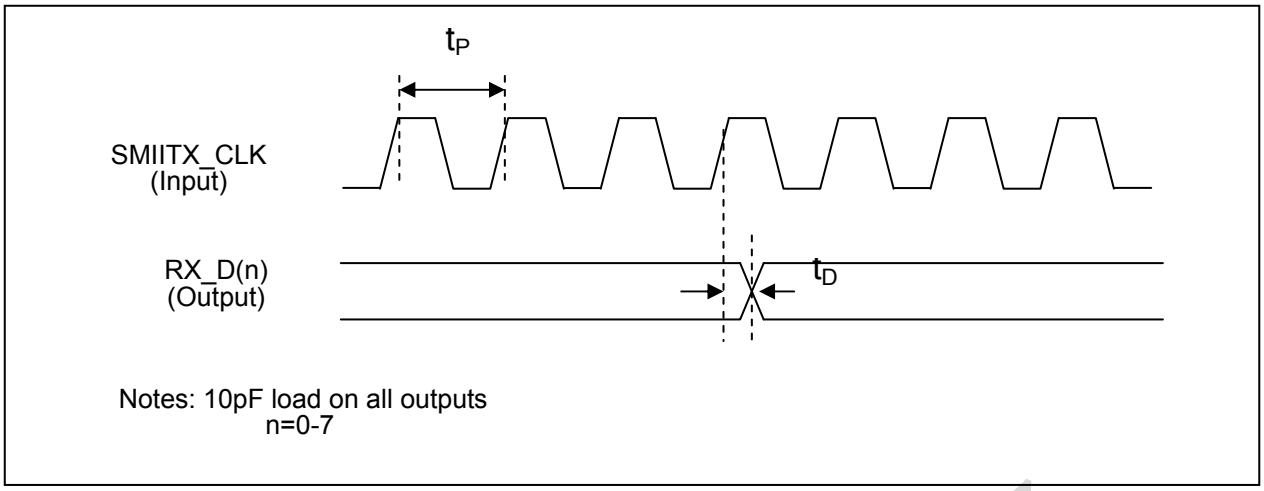

Figure 15 SMII Receive Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
RX_D(n) delay from SMIITX_CLK↑	t_D	1.5		4.5	ns

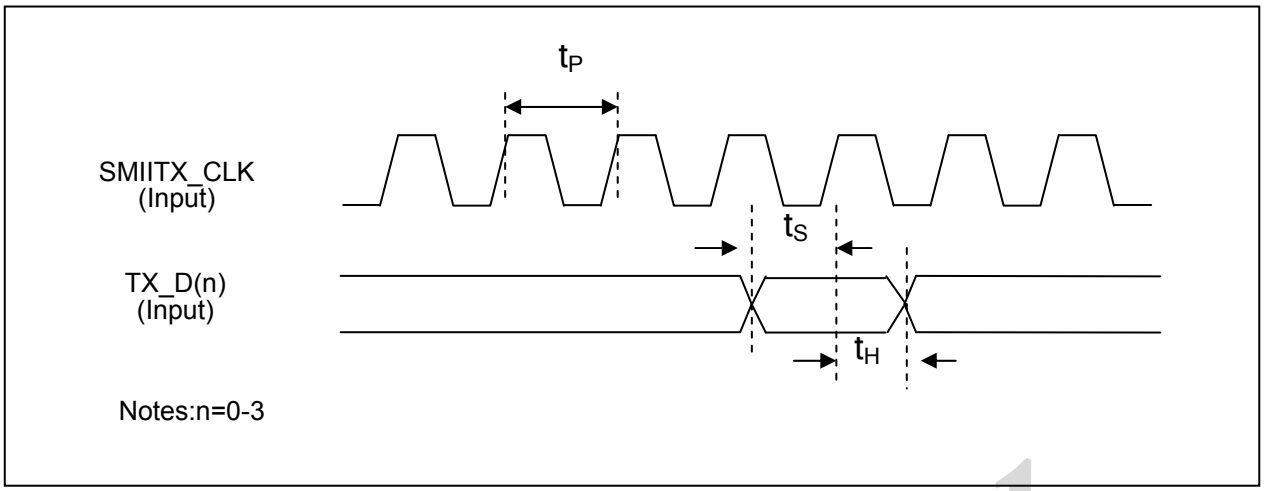

Figure 16 SMII Transmit Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
RX(n) setup to SMIITX_CLK↑	t_S	1.5			ns
RX(n) hold from SMIITX_CLK↑	t_H	1.0			ns

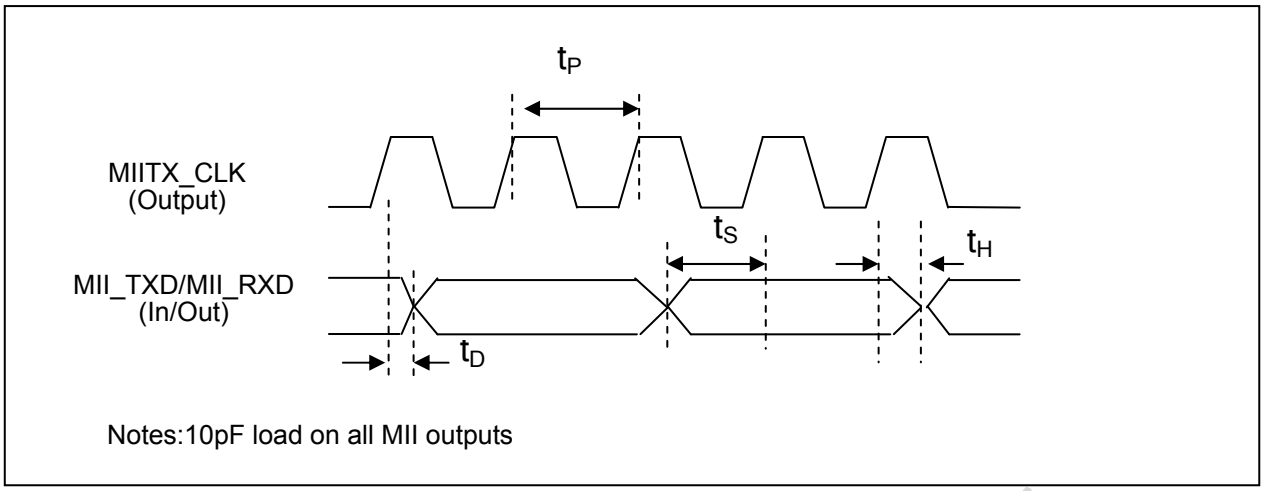

Figure 17 MII Interface Timing

	Symbol	Min	Typ	Max	Unit
MII_CLK frequency	$1/t_P$	16.66		25	MHz
MII_CLK duty cycle	t_P	40		60	ns
MII_TXD/MII_RXD delay from MII_CLK↑	t_D	10		100	ns
MII_TXD/MII_RXD setup to MII_CLK↑	t_S	15			ns
MII_TXD/MII_RXD hold from MII_CLK↑	t_H	0.0			ns

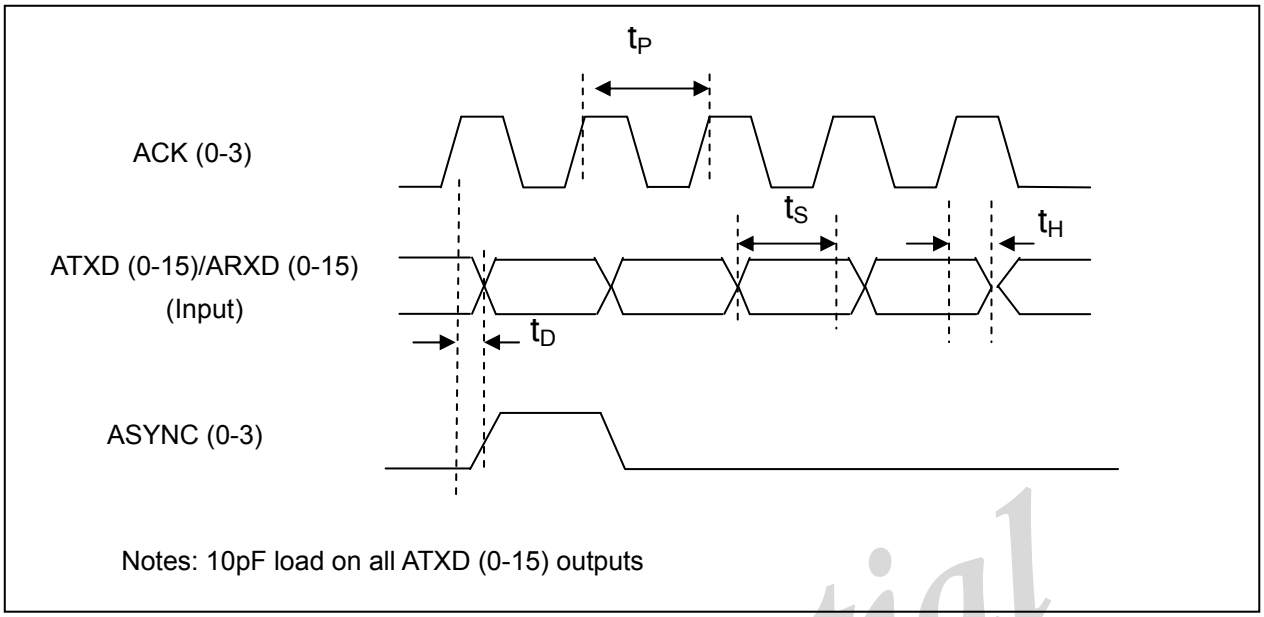

Figure 18 Analog Front End (AFE) Interface Timing

	Symbol	Min	Typ	Max	Unit
ACCLK(0-3) frequency	$1/t_P$		35.328		MHz
ACCLK(0-3) duty cycle	t_P		28.03		ns
ATXD(0-15)/ARXD(0-15) delay from ACLK↑	t_D	10		100	ns
ATXD(0-15)/ARXD(0-15) setup to ACLK↑	t_S	15			ns
ATXD(0-15)/ARXD(0-15) hold from ACLK↑	t_H	0.0			ns

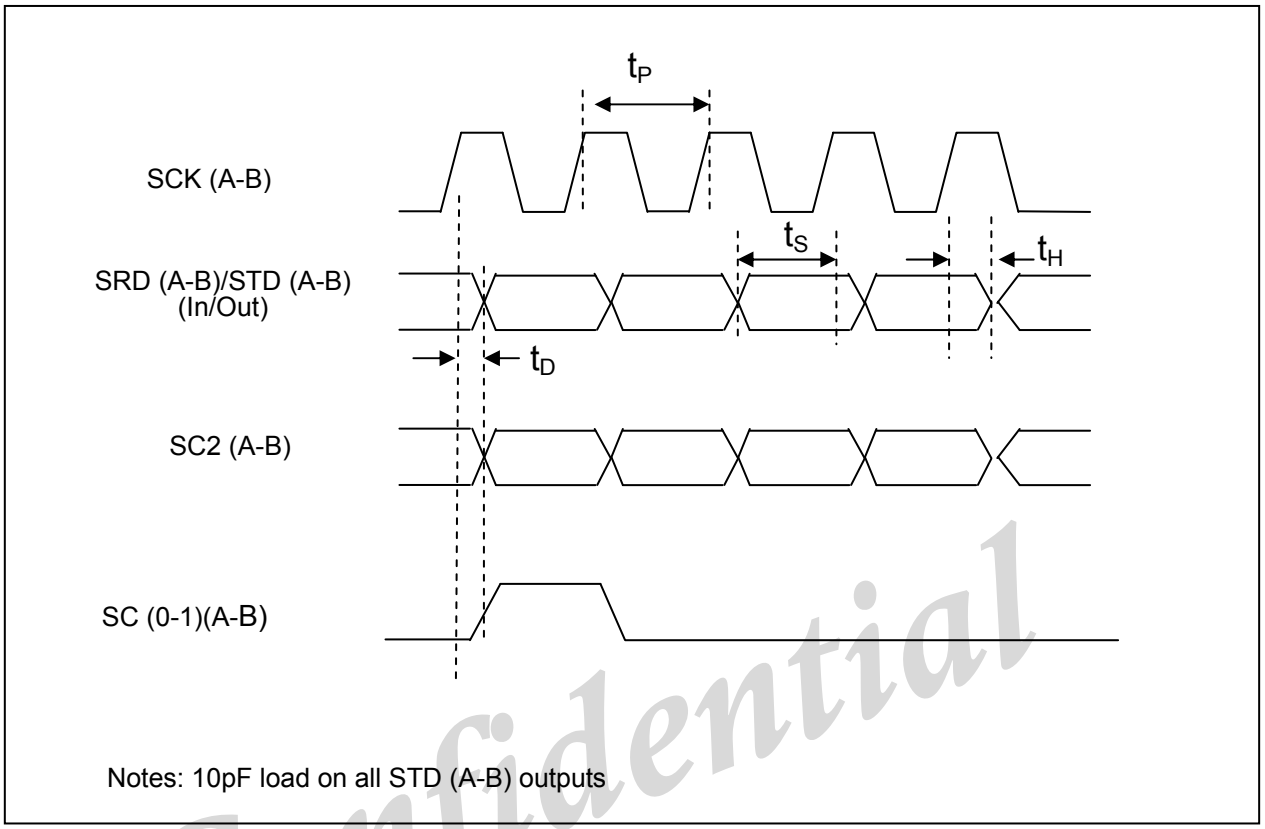

Figure 19 Serial Port A-B Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
SCK(A-B) frequency	$1/t_P$	0.036		37.5	MHz
SCK(A-B) duty cycle	t_P	30		30000	ns
SRD(A-B)/STD(A-B) delay from SCK↑	t_D	10		100	ns
SRD(A-B)/STD(A-B) setup to SCK↑	t_S	15			ns
SRD(A-B)/STD(A-B) hold from SCK↑	t_H	0.0			ns
SC(0-2)(A-B) delay from SCK↑	t_D	10		100	ns

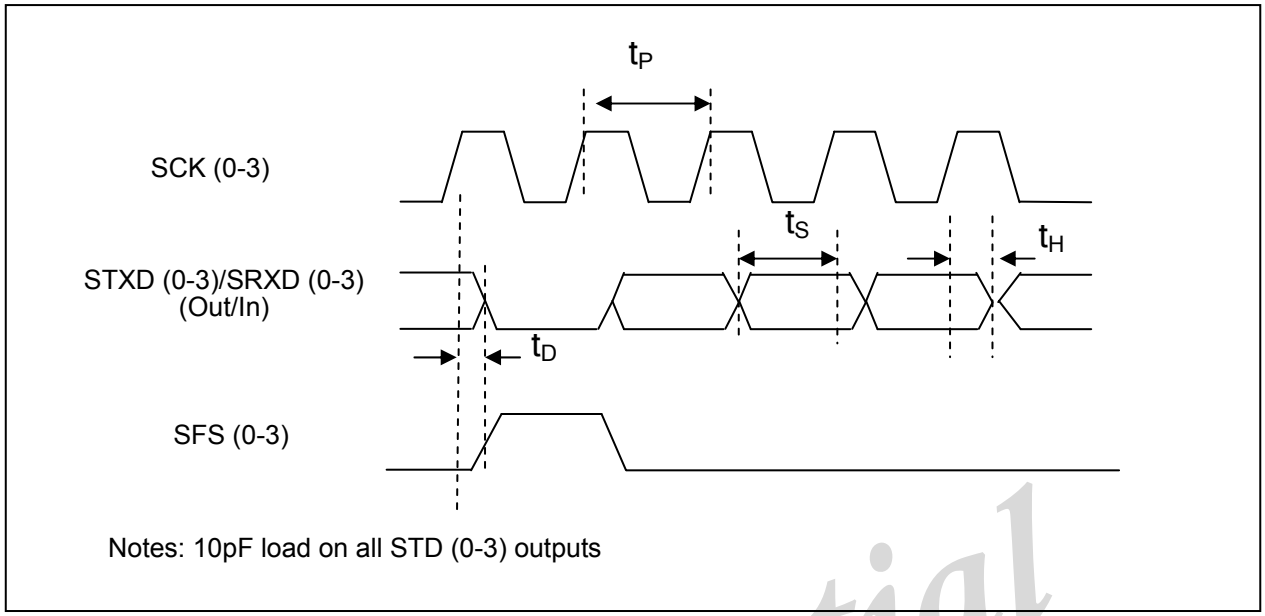

Figure 20 Serial Port 0-3 Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
SCK(0-3) frequency	$1/t_P$	27		33.3	MHz
SCK(0-3) duty cycle	t_P	30		35	ns
STXD(0-15)/SRXD(0-15) delay from SCK↑	t_D	10		100	ns
STXD(0-15)/SRXD(0-15) setup to SCK↑	t_S	15			ns
STXD(0-15)/SRXD(0-15) hold from SCK↑	t_H	0.0			ns

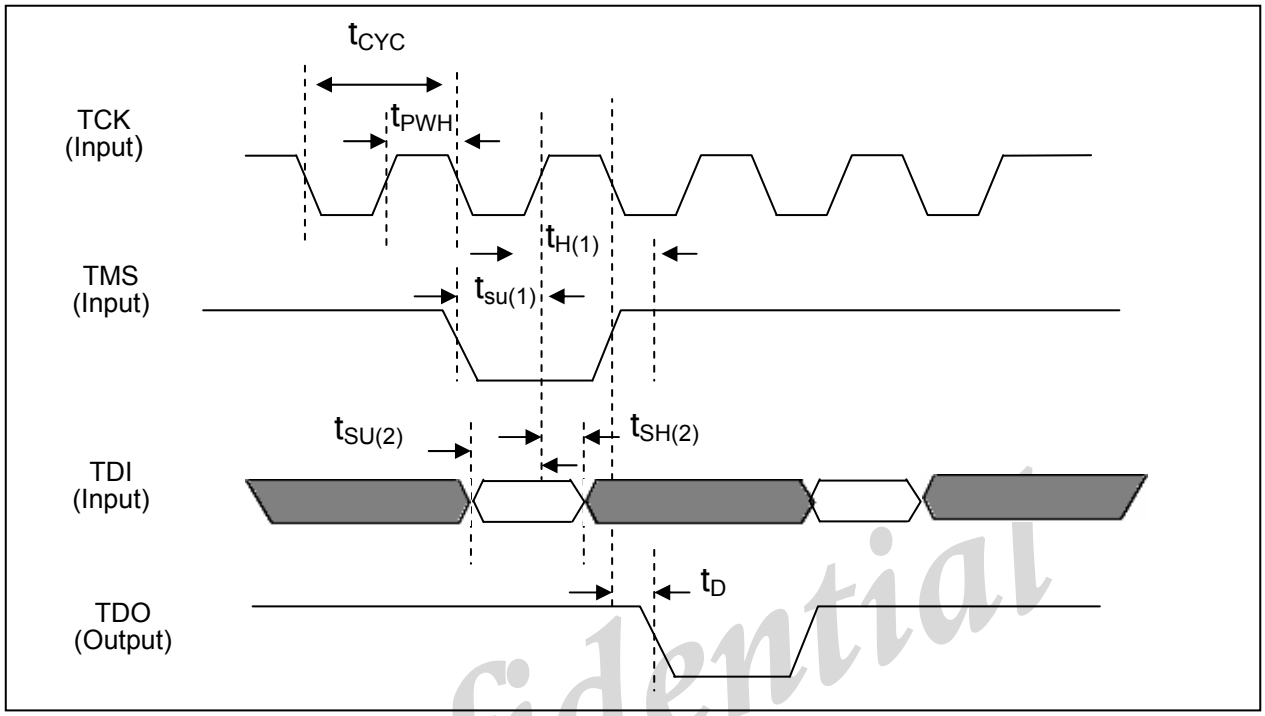

Figure 21 Boundary Scan Timing

Parameter	Symbol	Min	Max	Unit
TCK clock cycle time	t_{CYC}	50		ns
TCK clock duty cycle	t_{PWH}/ t_{CYC}	40	60	%
TMS setup time before TCK↑	$t_{SU(1)}$	4.0		ns
TMS hold time after TCK↑	$t_{H(1)}$	1.0		ns
TDI setup time before TCK↑	$t_{SU(2)}$	6.0		ns
TDI hold time after TCK↑	$t_{H(2)}$	1.0		ns
TDO delay after TCK↑	t_D		15.0	ns

5 Package Information

The Falcon device is packaged in a 14mm×14mm (3.20 mm), 128-lead thin-profile quad flat package (LQFP) suitable for surface mounting, as shown in Figure 22.

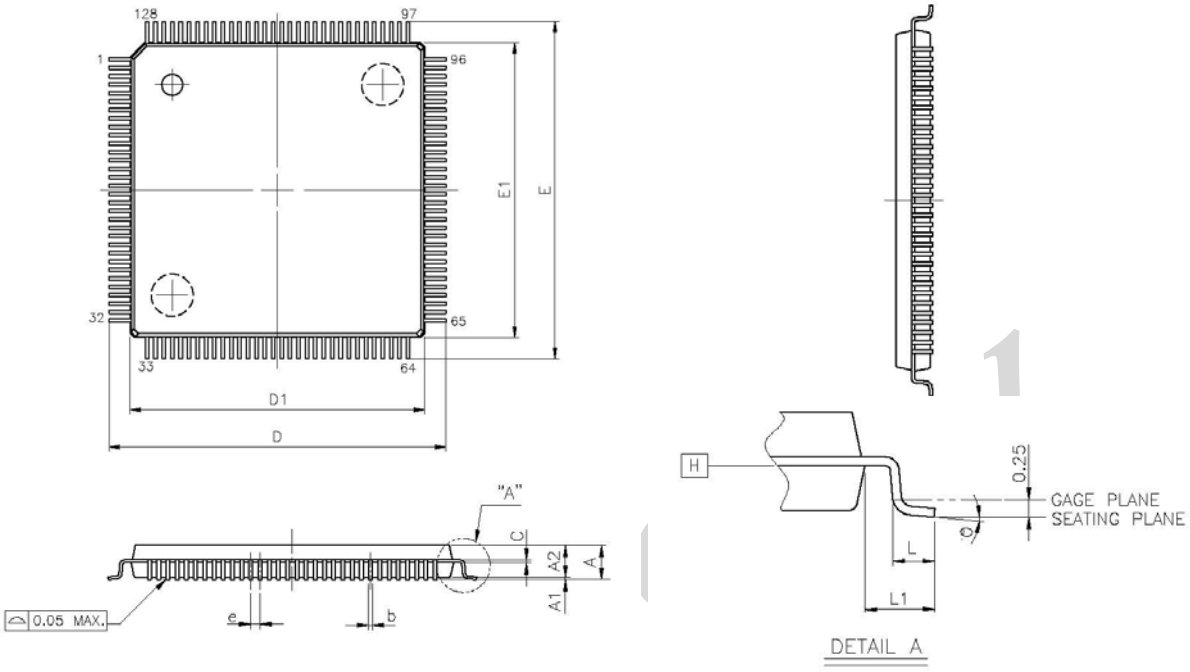

Figure 22 MT2201 LQFP Package Diagram

VARIATIONS (ALL DEMINSIONS SHOW IN MM)

SYMBOLS	Min	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.13	0.16	0.23
c	0.09	--	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Notes:

1. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

6 Ordering Information

Prefix	Part No. (4 numbers)	Package		-	Version
		RoHS or Not	Package Type		
MT	2201	G: **Green Product** N: **Pb Product**	N: **QFN** P:**QFP** L: **LQFP** C:**CHIP** B:**BGA**	-	B1

Part Number

- MT2201GL-B1: 1 port VDSL1 DMT chip with 128-LQFP package.