Falcon Device

Single VDSL Analog Front End Chip

MT3201

Data Sheet

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Metanoia Communications Inc.

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Single VDSL AFE

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PRODUCT PREVIEW

General Description

The MT3201 VDSL AFE provides all analog functions necessary for receiving and transmitting VDSL data according to ETSI and ANSI. The device includes in the transmit path a 14-bit DAC and a fully integrated line driver. The receive path consists of an integrated hybrid and a variable gain amplifier with up to 35 **dB** gain and a 14-bit ADC. As single port device it is intended to be used in customer premises equipment (CPE). The full 12MHz bandwidth support in downstream and upstream direction also allows the use in central office (CO).

Key Features

- Fully integrated VDSL Analog Front End (AFE) including line driver
- Realized in standard CMOS
- 5V/2.5V dual analog supply for high efficiency line driver
- Digital I/O supply variable from 1.2V up to 3.3V
- Low power consumption 950Mw/channel @14.5dBm line power
- I/O data stream at 35 MSPS
- 14 bit resolution / 12 bit accuracy DAC with low out of and noise fitting PSD masks
- Variable gain amplifier (VGA) with up to 35dB gain
- 14 bit resolution / 12 bit accuracy ADC with sophisticated Sigma-Delta architecture
- On-chip clean-up PLL
- Minimum of external components necessary
- Selectable power down modes
- 35.328MHz crystal reference oscillator
- Operation with 30MHz reference clock for QAM available
- All functions controllable through serial bus interface

Applications

The MT3201 Single Channel Analog Front End is optimized for CPE applications where the degree of integration enables a very dense PCB layout. 2, 3 and 4 band operating modes make the MT3201 suitable for MDU/MTU Applications as well.

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1. General Description

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1-1 MT3201 Key Features

- Fully integrated VDSL Analog Front End (AFE) including line driver
- Realized in standard CMOS
- 5V/2.5V dual analog supply for high efficiency line driver
- Digital I/O supply variable from 1.2V up to 3.3V
- Low power consumption 950mW/channel @ 14.5dBm line power
- Supports 2, 3 and 4 bands of operation (U0 optional)
- I/O data stream at 35 MSPS
- 14 bit resolution / 12 bit accuracy DAC with low out of band noise fitting PSD masks
- Line driver with SNDR of 75dB at 14.5dBm transmit power
- Variable gain amplifier (VGA) with up to 35dB gain
- 14 bit resolution / 12 bit accuracy ADC with sophisticated Sigma-Delta architecture
- On-chip clean-up PLL
- Minimum of external components necessary
- Selectable power down modes
- 35.328MHz crystal reference oscillator
- Operation with 30MHz reference clock for QAM available
- All functions controllable through serial bus interface

1-2 MT3201 Applications

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1-3 Application Block Diagram

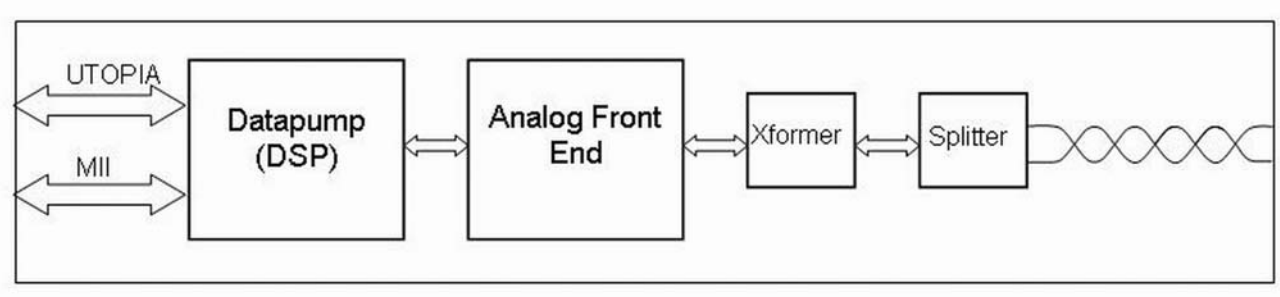

Figure 1 Typical CPE Application Block Diagram

2. Functional Description

2-1 Overview

The MT3201 incorporates a fully integrated AFE with line driver compliant to the ITU standard[1]. TX and RX paths can work fully independent but share common blocks like the PLL and the serial bus interface. The absence of nearly all external components and the low pin count in combination with the small package outline contributes to a very dense board layout.

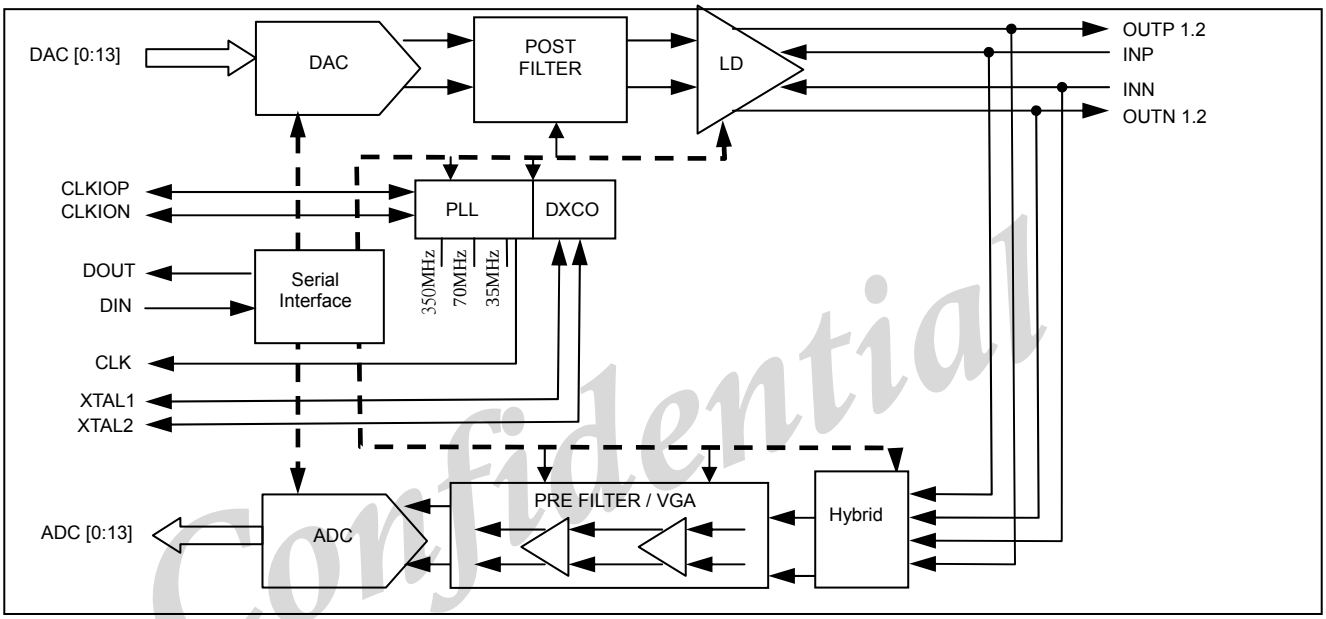

Figure 2 Block Diagram

[1] Band allocations e.g. frequency plans A, B, etc are supported but the separation of up- and downstream has to be performed by the DSP.

2-2 Transmit Path

2-2-1 Digital to Analog Converter (DAC)/TX Post Filter

The DAC consists of 3 blocks: a digital interpolation filter, a current steering DAC and a 4th order continuous-time post filter. The interpolation filter receives a 14-bit wide data stream in two's complement at 35.328MS/s. To attenuate images at 35,70 and 105MHz the filter has an up-sampled output of 140MS/s which feeds the current steering DAC. The 4th order continuous-time post filter following the DAC guarantees the required suppression of all out-of-band images and noise. The typical corner frequency of 18MHz is kept within a ±7% range by means of an automatic RC-time constant adjustment during power-up.

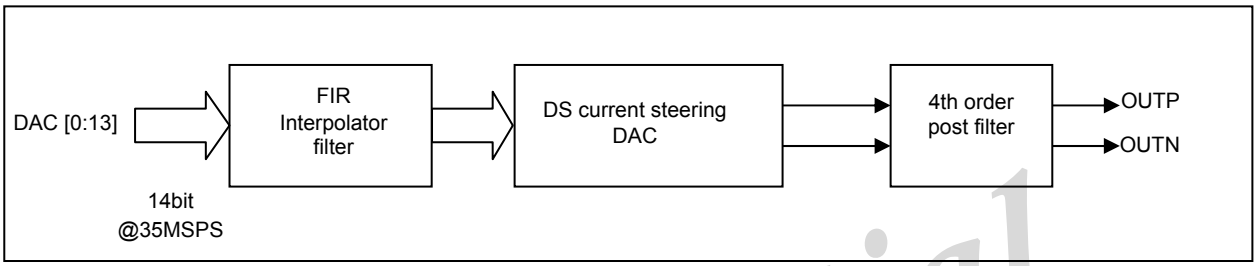

Figure 3 DAC Block Diagram

2-2-2 Power Back Off

To allow a power back off (PBO) from +14.5dBm down to 0.0dBm line power, a programmable attenuation is realized from 0dB down to -14.5dB in 0.5dB steps. To keep the DAC operating with the optimal S/N conditions, this attenuation is mainly realized in the post-filter block. If again finer attenuation steps are necessary, digital attenuation using the DSP can be used in conjunction with the analog attenuation.

2-2-3 Line Driver

The line driver takes its input signal from the DAC post filter. The fully integrated line driver reaches an extremely high linearity by means of a sophisticated compensation technique, whereby additional outputs and external circuitry are needed (see Figure4: Line driver/VGA/Hybrid equivalent circuit diagram and Figure 12: Test circuit). To minimize the power consumption, 40% of the output impedance is synthesized. This configuration allows a highly efficient line driver design with a single 5V supply only. The necessary amplifier feedback path is also used as the input of the receive path.

2-3 Receive Path

2-3-1 Variable Gain Amplifier and Hybrid

The VGA is used to adapt the dynamic range of the received signal to best fits the S/N and dynamic range requirements of the ADC. The combined VGA/Hybrid is also used to reduce NEXT and echo from the received signal. Bridged taps and non resistive behavior of the line impedance and the transformer will decrease the hybrid rejection.

A first order high pass filter located in the VGA attenuates the remaining signal of the first down-stream band D1. Hence, the hybrid performance can be optimized to reduce the remaining echo resulting in an improved overall rejection.

The VGA has a minimum gain setting of -6dB and a maximum of 35dB into 1 dB-steps between 12 and 35 dB. Below 12dB gain 2dB steps are possible.

2-3-2 Analog to Digital Converter

The 12-bit accurate Analog to Digital Converter is implemented as a continuous time Sigma-Delta modulator with subsequent decimation stages. The 12MHz analog bandwidth modulator uses a sampling frequency of 350MHz. the 6 bit output of the modulator passes through a SINC4/4 and a programmable 8th order IIR-filter. This filter delivers a 14-bit wide 35.328MSPS output steam in two's complement (see Figure 4).

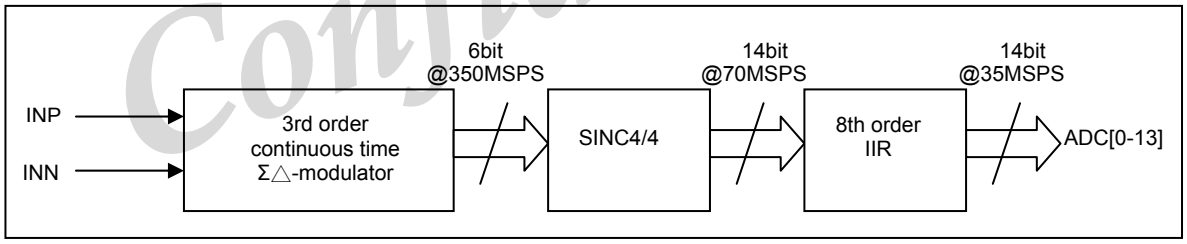

Figure 4 ADC Block Diagram

2-4 Common Blocks

2-4-1 Crystal Oscillator

The reference-oscillator requires a 30.240/35.328MHz crystal (type TBD) to be connected between pins XTAL1 and XTAL2. To compensate for the tolerances of the crystal, the oscillator allows a frequency adjustment by switching internal capacitors within a range from 6pf to 38pf in about 5fF-steps at both XTAL1/2 pins. The resulting frequency range of the adjustment ultimately depends on the crystal's equivalent circuit. Typical values are ±200ppm frequency range.

This adjustment can also be used to synchronize the modem timing with the system wide timing.

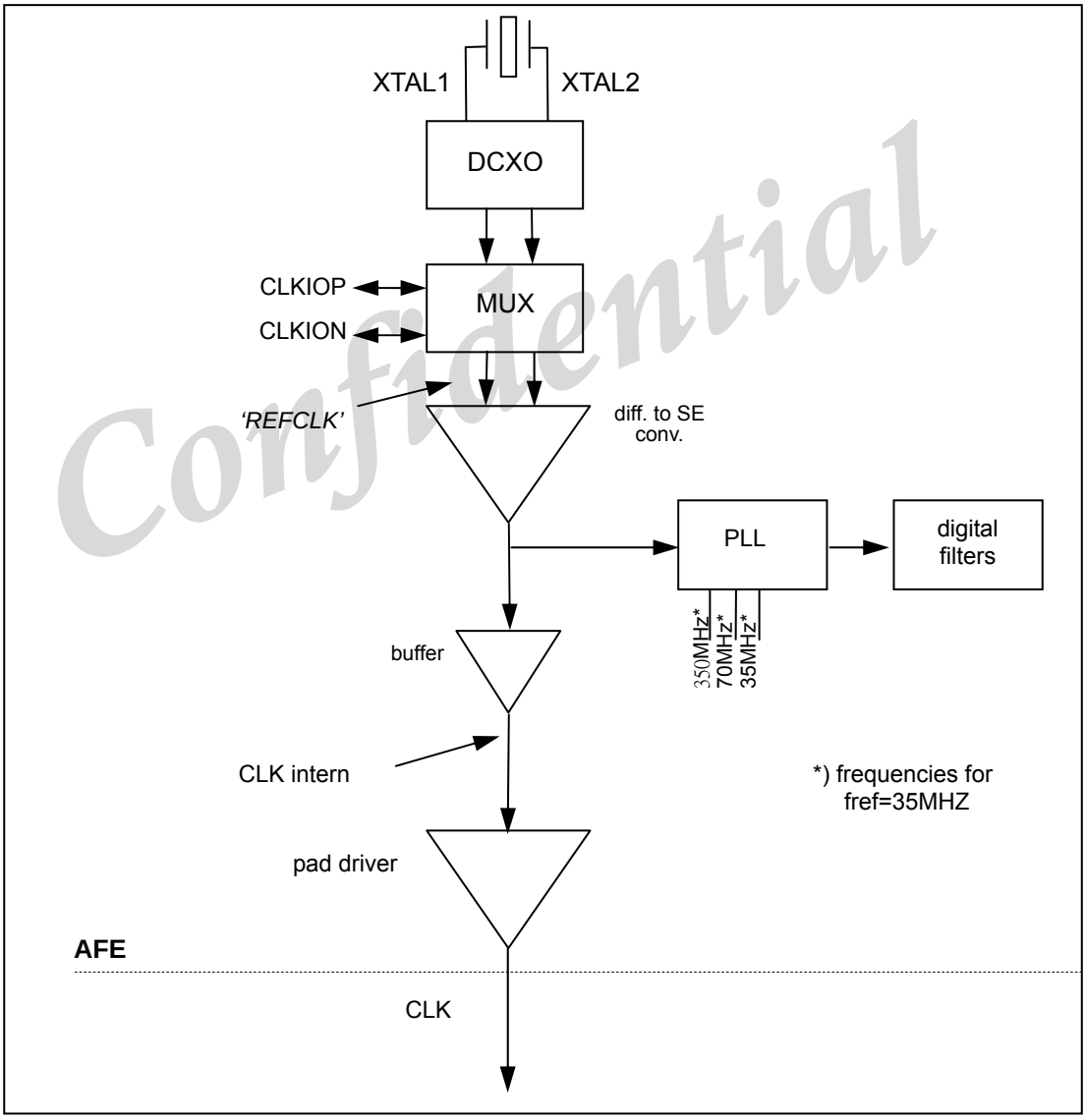

Figure 5 Oscillator/ PLL Block Diagram

2-4-1-1 PLL and Master/ Slave Selection

The AFE's on-chip crystal-oscillator can be used to supply the clock to the DSP referred to as master mode. The clock distribution to the DSP uses the single ended CLK. This signal is also reference clock for the serial control interface.

2-4-1-1-1 Master Mode Identification

The master mode is automatically chosen during power on. If the crystal oscillator starts operation the pad buffer tries to pull down the CLK pin at 35MHz periodically. If this is successful, the device considers being the clock master as the two master-conditions are true:

1. Crystal oscillator running: crystal present and
2. CLK pin is output: not connected to VDDxIF.

2-4-1-1-2 Slave Mode Identification

If the CLK pin is tied to VDDxIF the device puts itself into slave mode. The "slave" AFE will receive its clock from the DSP through CLKIOP/N as a differential signal. This scheme gives a high robustness against noise and jitter. In case there is only a single ended clock output available at the DSP, a connection as show in Figure 6: c) is also possible. Figure 6: a) and b) show master mode and differential slave connections, respectively.

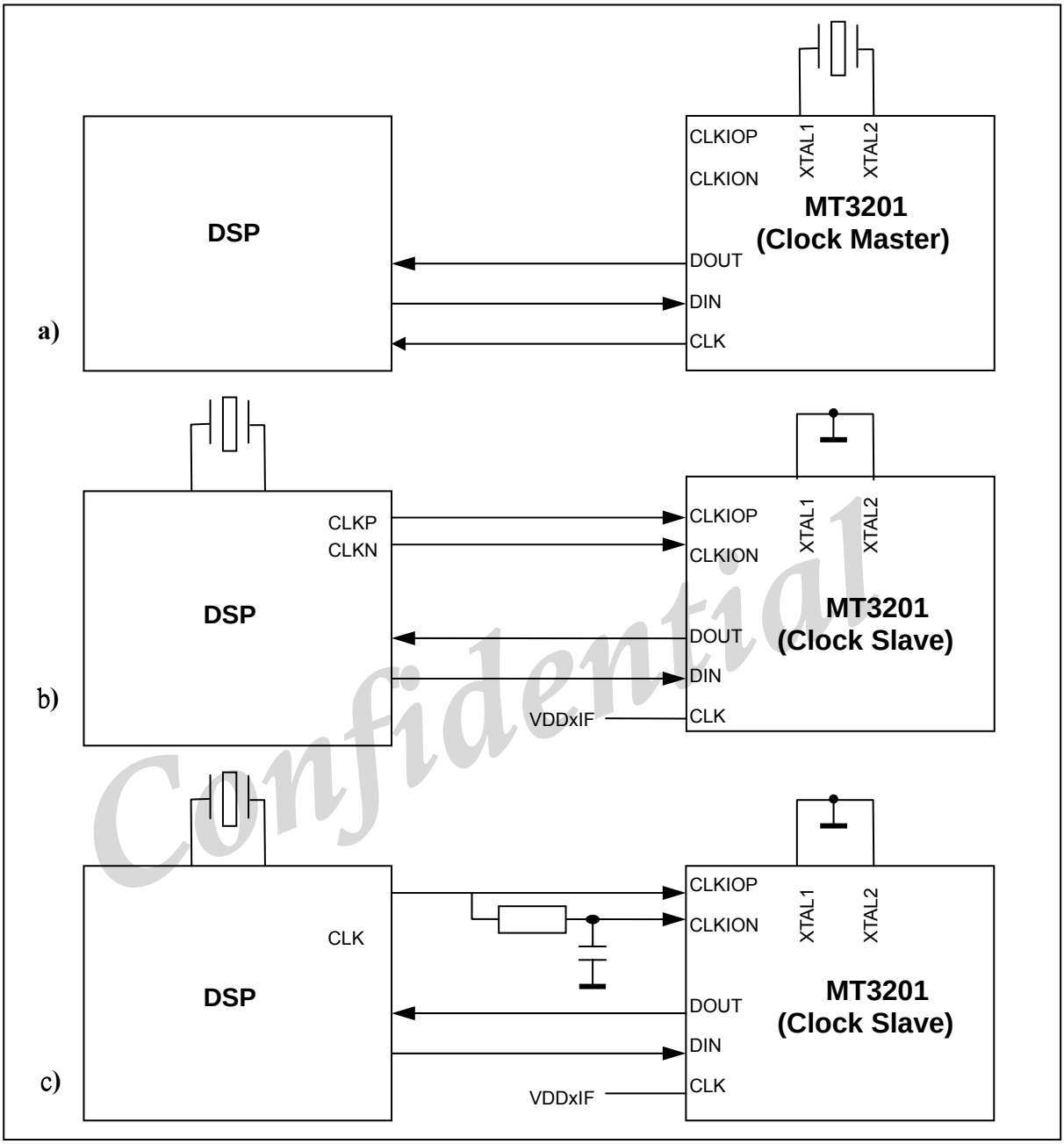

Figure 6 Clocking and Synchronization Scheme

2-4-2 TX and RX Data I/O

The TX and RX data between the DSP and the AFE is exchanged at a sample rate of 35.328MS/s. Synchronization is guaranteed by the system wide 35.328MHz clock (pin CLK or CLKIOP/N).

2-4-2-1 AFE Master Clock Mode

Necessary clock and data connections for the AFE-master mode are shown in the following figure.

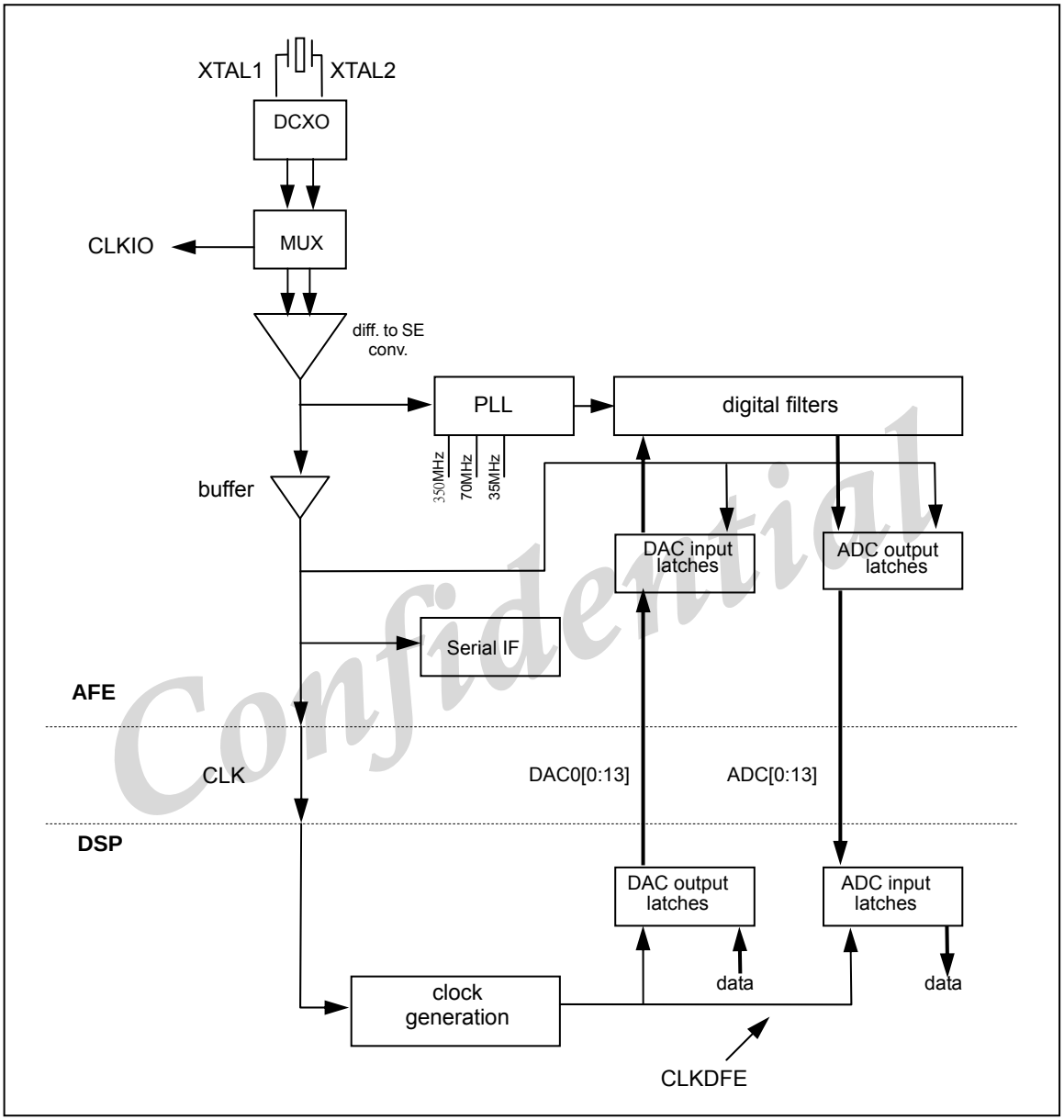

Figure 7 Data and Clock Connections between DSP and AFE – Master Mode

Additional timing diagrams are given in section 3-3.

2-4-2-2 AFE Slave Clock Mode

The necessary connections are shown in the following figure. Either a differential or single ended clock connection (CLKIO) between the DSP and the AFE guarantees synchronization.

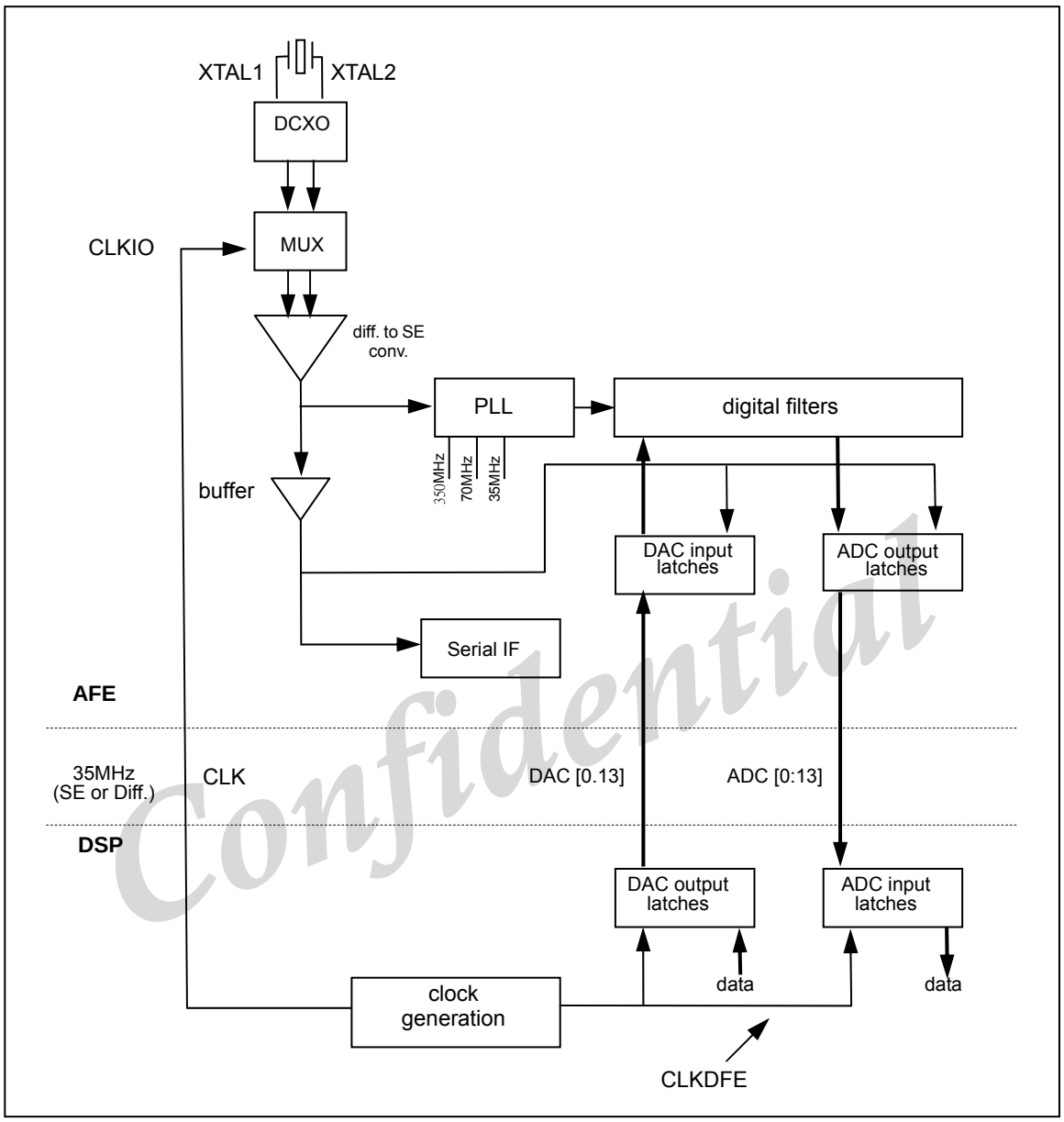

Figure 8 Data and Clock Connections between DSP and AFE – Slave Mode

2-4-3 Serial Control Interface

The serial control interface consists of the three connections CLK, DIN and DOUT. The CLK is the system wide 35.328MHz reference clock provided through the AFE. The DIN line carries information from the DSP to the AFE, whereas DOUT transfers information from the AFE to the DSP.

The protocol comprises of

1 startbit`0`

a data word of
12 bit data d11-d0 (in case of a 'Read' command the data won't be evaluated)

and register/ command bits

3 bit register address a2-a0
1 it R/W, Read=0, Write=1

The protocol is shown in Figure 9: Serial control interface protocol.

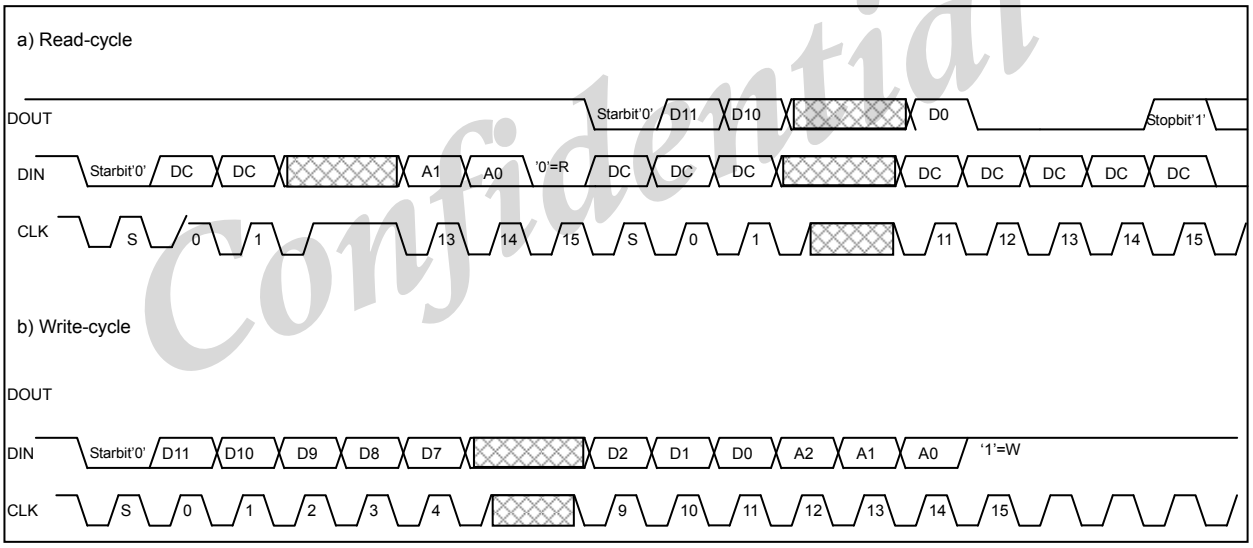

Figure 9 Serial Control Interface Protocol

If a "Read" command is initiated (as the DSP needs to read back the data from the AFE) one clock cycle later the AFE will transmit on a dedicated pin DOUT starting with a'0'startbit the 12 bit data word d11-d0 of the specified address a2-a0 followed by 3 '0'and a '1'stop bit.

The serial interface allow the programming of the different functions and blocks, e.g. power down and gain settings.

2-5 Programming

2-5-1 Chip Register Addresses

The default value of all register bits at power on is“0”. When register setting instructions given in this document make no mention of certain bits, they must be left or set to “0”.

Register#	Block (Function)
000 (0)	VGA
001 (1)	ADC/VGA
010 (2)	DCXO frequency adjustment
011 (3)	DAC/Post filter/Line driver
100 (4)	Bias/References
101 (5)	PLL/DCXO2
110 (6)	Reserved
111 (7)	Fuses (read only)

Register 6 contains bit setting for control during test. They are for internal use only and must be set to “0”.
Register 7 is a read-only register and is used to store trimmings during electrical wafer sort. The settings can be read later and used to adjust RC-time constants, bias and reference currents.
Underlined settings are recommended settings. If no indication is given the setting is according to application requirements.

2-5-2 Address 0 (VGA)

Function	11
Transformer Matching	
Disable	0
Enable	1

Function	10	9	8	7
VGA1 Gain				
-6dB	0	0	0	0
Not Allowed	0	0	0	1
0dB	0	0	1	0
Not Allowed	0	0	1	1
Not Allowed	0	1	0	0
Not Allowed	0	1	0	1
6dB	0	1	1	0
Not Allowed	0	1	1	1
12dB	1	0	0	0
13dB	1	0	0	1
18dB	1	0	1	0
19dB	1	0	1	1
Not Allowed	1	1	0	0
Not Allowed	1	1	0	1
24dB	1	1	1	0
25dB	1	1	1	1

Function	6	5
RX High Pass Filter		
Active High Pass Filter, fc=10KHz	0	0
Not Allowed	0	1
Active High Pass Filter, fc=3MHz	1	0
Active High Pass Filter, fc=6MHz	1	1

Function	4
RX Low Pass Filter	
Full Bandwidth (12MHz)	0
Activate 6MHz Low Pass Filter	1

Function	10*)	3	2	1	0
Hybrid Equivalent Line Impedance Setting					
60Ω	0	0	0	0	0
78Ω	0	0	0	0	1
78Ω	0	0	0	1	0
97Ω	0	0	0	1	1
75Ω	0	0	1	0	0
93Ω	0	0	1	0	1
93Ω	0	0	1	1	0
117Ω	0	0	1	1	1
75Ω	0	1	0	0	0
93Ω	0	1	0	0	1
93Ω	0	1	0	1	0
117Ω	0	1	0	1	1
89Ω	0	1	1	0	0
111Ω	0	1	1	0	1
111Ω	0	1	1	1	0
144Ω	0	1	1	1	1
60Ω	1	0	0	0	0
67Ω	1	0	0	0	1
78Ω	1	0	0	1	0
88Ω	1	0	0	1	1
100Ω	1	0	1	0	0
115Ω	1	0	1	0	1
134Ω	1	0	1	1	0
154Ω	1	0	1	1	1
Not Allowed	1	1	0	0	0
Not Allowed	1	1	0	0	1
Not Allowed	1	1	0	1	0
Not Allowed	1	1	0	1	1
Not Allowed	1	1	1	0	0
Not Allowed	1	1	1	0	1
Not Allowed	1	1	1	1	0
Not Allowed	1	1	1	1	1

***) Note**: Bit 10 also enables/disable the first gain stage VGA1

2-5-3 Address 1 (ADC/VGA2)

Function	11
ADC/VGA Power Down	
ADC/VGA Running	0
ADC/VGA Power down	1

Function	10	9	8
VGA Gain 2			
0dB	0	0	0
2dB	0	0	1
4dB	0	1	0
4dB	0	1	1
6B	1	0	0
8dB	1	0	1
10dB	1	1	0
10dB	1	1	1

2-5-4 Address 2 (DCXO Frequency Adjustment)

Function	11	10	9	…	2	1	0
Crystal Oscillator Frequency Adjustment							
0fF	0	0	0	…	0	0	0
5fF	0	0	0	…	0	0	1
10fF	0	0	0	…	0	1	0
…							
…							
…							
…							
20.470pF	1	1	1		1	1	0
20.475pF	1	1	1		1	1	1

2-5-5 Address 3 (DAC/Post Filter/Line Driver)

Function	11
DAC/Post Filter Power Down	
DAC/Post Filter Running	0
DAC/Post Filter Power Down	1

Function	10	9
Power Back Off (PBO), Coarse Steps		
0dB	0	0
-4dB	0	1
-8dB	1	0
-12dB	1	1

Function	8	7	6
Power Back Off(PBO), Fine Steps			
0dB	0	0	0
-0.5dB	0	0	1
-1dB	0	1	0
-1.5dB	0	1	1
-2dB	1	0	0
-2.5dB	1	0	1
-3dB	1	1	0
-3.5dB	1	1	1

Function	5
Line Driver (LD) Power Down	
LD Running	0
LD Power Down	1

Function	4	3
Output Impedance During Power Down		
Infinite	0	0
128 Ohm	0	1
128 Ohm	1	0
64 Ohm	1	1

Function	2
Failure Protection	
Over Temperature and Over Current-rotection Active	0
Over Temperature and Over Current-protection Disabled	1

Function	1	0
Line Driver Bias Adjustment		
Standard Current	0	0
Standard Current x 0.66	0	1
Output Stage Current x 0.5	1	0
Standard Current x 0.66 / Output Stage Current x 0.5	1	1

2-5-6 Address 4 (Bias/Reference)

Function	11	10	9	8
TX Voltage Adjustment				
Default	0	0	0	0
Setting ΔV= - 0.9%	0	0	0	1
Setting ΔV= - 1.8%	0	0	1	0
Setting ΔV= - 2.7%	0	0	1	1
Setting ΔV= - 3.6%	0	1	0	0
Setting ΔV= - 4.5%	0	1	0	1
Setting ΔV= - 5.4%	0	1	1	0
Setting ΔV= - 6.3%	0	1	1	1
Setting ΔV=+7.2%	1	0	0	0
Setting ΔV=+6.3%	1	0	0	1
Setting ΔV=+5.4%	1	0	1	0
Setting ΔV=+4.5%	1	0	1	1
Setting ΔV=+3.6%	1	1	0	0
Setting ΔV=+2.7%	1	1	0	1
Setting ΔV=+1.8%	1	1	1	0
Setting ΔV=+0.9%	1	1	1	1

Function	7	6
Bias Current Adjustment		
Default	0	0
+12.5%	0	1
-25%	1	0
-12.5%	1	1

Function	3	4	5
Shutdown Temperature			
181℃	1	0	0
175℃	1	0	1
169℃	1	1	0
163℃	1	1	1
147℃	0	0	0
139℃	0	0	1
125℃	0	1	0
113℃	0	1	1

Function	2
Reference Power Down	
References Running	0
References Power Down	1

Function	1	0
For Internal Use Only		
Must be '00'	0	0

2-5-7 Address 5 (PLL/DCXO 2)

Function	11	10
Crystal Drive Level (Depending on Crystal Type)		
Maximum	0	0
High medium	0	1
Low medium	1	0
Minimum	1	1

Function	9
Power Down	
PLL Running	0
PLL Power Down	1

Function	8
PLL Mode	
Automatic Startup Procedure Enabled	0
Manual Startup	1

Function	7
PLL Loop Filter Corner Frequency	
100KHz	0
1MHz	1

Function	6
Reference Frequency Selection	
Reference is 30.240MHz	0
Reference is 35.328MHz	1

Function	5
Freeze Tuning	
Tuning Running	0
Tuning Frozen	1

Function	4	3	2	1	0
Internal Use Only					
Must be'00000'	0	0	0	0	0

2-5-8 Address 6 (Reserved)

Function	11	10	9	8	7	6
Internal Use Only						
Must Be '000000'	0	0	0	0	0	0

Function	5	4	3	2	1	0
Internal Use Only						
Must be '000000'	0	0	0	0	0	0

2-5-9 Address 7 (Fuses, Read Only)

Function	11	10	9	8	7	6
Internal Use Only						
Must be '000000'	0	0	0	0	0	0

Function	5	4	3	2	1	0
Calibration Values- Read Only						
TBD	R	R	R	R	R	R

3. Parameters

3-1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD-A1}	Analog supply voltage DAC,LD				7	V
V_{DD-A2}	Analog supply voltage VGA,ADC,PLL				5	V
V_{DD-D}	Digital core supply voltage				5	V
V_{DD-IO}	I/O-supply voltage				5	V
T_{STG}	Storage Temperature		-65		125	℃
T_J	Junction Temperature		-40		125	℃
V_{ESD}	Electrostatic Discharge Voltage Capability	HBM Mil. Std.883			2	kV

3-2 Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD-A1}	Analog supply voltage DAC,LD		4.75	5	5.25	V
V_{DD-A2}	Analog supply voltage VGA,ADC,PLL		2.375	2.5	2.625	V
V_{DD-D}	Digital core supply voltage		2.375	2.5	2.625	V
$V_{DD-I/O}$	I/O-supply voltage		1.1		3.5	V
T_{AMB}	Ambient temperature		-40	25	85	℃

3-3 Thermal Resistance

Parameter	SYM	Condition	Min.	Typ.	Max.	Unit
Thermal resistance Junction to ambient	θja	4 layer PCB, 0m/s airfolw	-	26.26	-	℃/W
Thermal resistance Junction to case	θjc	4 layer PCB, 0m/s airfolw	-	1.94	-	℃/W

3-4 Electrical Characteristics

Standard conditions unless otherwise stated: V_{DD-A1}=5V, V_{DD-A2}=2.5V, V_{DD-D2}=2.5V, $V_{DD-I/O}$=1.2V, T_A=25℃, Crystal oscillator frequency 35.328MHz

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD-A1}	Analog supply voltage DAC,LD		4.75	5	5.25	V
V_{DD-A2}	Analog supply voltage VGA,ADC,PLL		2.375	2.5	2.625	V
V_{DD-D}	Digital core supply voltage		2.375	2.5	2.625	V
$V_{DD-I/O}$	I/O-supply voltage		1.1		3.5[2]	V
$P_{SUPPLY1}$	Power consumption	@14.5dBm line power, 14.5db Crest factor		950		mW
	Transmit path					
DR_{TX}	Input data rate			-	35.328	MS/s
Res_{TX}	Resolution		-	14	-	bits
$V_{outmaxTX}$	max. output voltage	@ 0dBfs, PBO=0dB, concept of synthesized impedance	7.2			V_{dpp}
$V_{outCMTX}$	Common mode output voltage			$V_{DD-A1}/2$		V
$I_{outmaxTX}$	max. output current		800			mA
PSD_{IBLTX}	Output noise in-band	line referred, 138kHz..12MHz		-128		dBm/Hz
PSD_{OBLTX}	Output noise out-of-band	line referred,> 12MHz		-128		dBm/Hz
$PSRR_{TX}$	Power supply ripple reject ration			TBD		dB
f_{lowTX}	Signal bandwidth lower corner frequency			10		kHz
f_{highTX}	Signal bandwidth upper corner		12			MHz
PBR_{TX}	Passband ripple			0.5		dB
THD_{TX-3}	Total harmonic distortion	f_{in}=1.7,2.4,4MHz @-3dBfs harmonics in band			-70	dBc
THD_{TX0}	Total harmonic distortion	f_{in}=1.7,2.4,4MHz @0dBfs harmonics in band			-70	dBc
IM_{TX}	Intermodulation	in band < 12MHz			-70	dBc
MBD_{TX}	Missing band depth			59		dB
GR_{PBO}	Power back off range		-14.5		0	dB
SS_{PBO}	PBO step size			0.5		dB
SS_{PBOADJ}	PBO accuracy		-0.5		0.5	dB

[2] The supply voltage for the digital I/O's can take any voltage between 1.1V and 3.5V

Electrical Characteristics cont.

Symbol	Receive path		Min.	Typ.	Max.	Unit
DR_{RX}	Output data rate			-	35.328	MS/s
Res_{RX}	Resolution		-	14	-	bits
$V_{inmaxRX}$	Max. input voltage	VGA gain=0dB		3.6		V_{dpp}
GR_{VGA}	VGA gain range		-6		35	dB
SS_{VGA}	VGA step size	Gain-6dB through +12dB Gain+12dB hrough+35dB		2 1		dB dB
SS_{VGAADJ}	VGA accuracy		-0.5		0.5	dB
$PSRR_{RX}$	Power supply ripple rejection ratio			TBD		dB
f_{lowRX}	Signal bandwidth lower corner frequency			10		kHz
f_{highRX}	Signal bandwidth upper corner frequency		12			MHz
PBR_{RX}	Passband ripple			1		dB
SNR_{RX}	Signal to noise ratio	fref=1MHz		72		dBc
THD_{RX-3}	Total harmonic distortion	f_{in}=4,6MHz @-3dBfs			-70	dBc
THD_{RX0}	Total harmonic distortion	f_{in}=4,6MHz @ 0dBfs		TBD		dBc
$SNDR_{RX}$	Signal to noise and distortion ratio			70		dB
PSD_{LRX}	Input noise	Line referred		-135		dBm/Hz
GD_{RX}	Group delay variation			TBD		µs
IM_{RX}	Intermodulation			TBD		dBc
MBD_{RX}	Missing band depth			58		dB
	Xtal Oscillator					
f_{0SC}	frequency	Xtal TBD		30.240/ 35.328		MHz
ΔC_{trim}	Capacitor trimming range	see section 2-4-1	6		38	pF
	Digital I/O's					
V_{IH}	Input 'high'		$V_{DD-I/O}$*0.8			V
V_{IL}	Input 'low'				$V_{DD-I/O}$*0.2	V
V_{OH}	Output 'high'		$V_{DD-I/O}$-0.1			V
V_{OL}	Output 'low'				0.1	V
C_{in}	Input capacitance				5	pF
C_{load}	Ioad capacitance	@ 60MHz signal			30	pF
	I/O Timing					
T_{CLK}	Clock period	CLK=1/f_{OSC}		28.306		ns
DC	Clock duty cycle	CLK30		50		%
T_R /T_F	Rise/fall time	20% to 80%		2.5		ns
$T_{invalidADC}$	Invalid time ADC, DOUT	see Figure 11	0		6	ns
$T_{setupdac}$	Setup time DAC		12			ns
$T_{holddac}$	Hold time DAC		0			ns

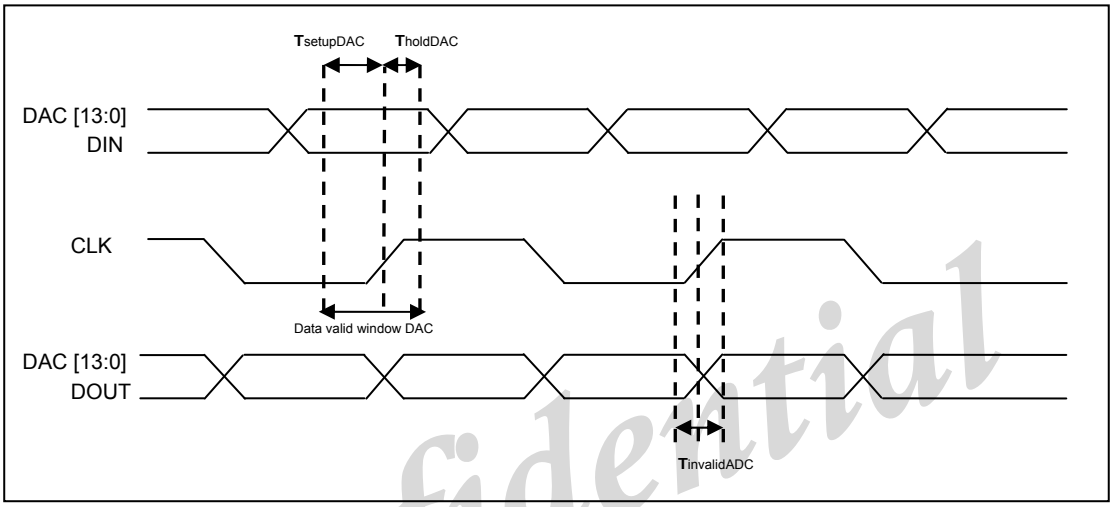

Figure 10 Data and Control Interface Timing

4. Pin Description

Pin	Symbol	I/O	Logic	Description
1	INP	AI		Positive hybrid/LD feedback input
2	INN	AI		Negative hybrid/LD feedback input
3	DAC0	DI		Data 0, Interpolator/DAC input
4	DAC1	DI		Data 1, Interpolator/DAC input
5	DAC2	DI		Data 2, Interpolator/DAC input
6	DAC3	DI		Data 3, Interpolator/DAC input
7	DAC4	DI		Data 4, Interpolator/DAC input
8	VDDDIG	Supply		Digital power supply , 2.5V
9	VDDDAC	Supply		Analog power supply DAC, 2.5V
10	DAC5	DI		Data 5, Interpolator/DAC input
11	DAC6	DI		Data 6, Interpolator/DAC input
12	DAC7	DI		Data 7, Interpolator/DAC input
13	DAC8	DI		Data 8, Interpolator/DAC input
14	DAC9	DI		Data 9, Interpolator/DAC input
15	DAC10	DI		Data 10, Interpolator/DAC input
16	DAC11	DI		Data 11, Interpolator/DAC input
17	DAC12	DI		Data 12, Interpolator/DAC input
18	DAC13	DI		Data 13, Interpolator/DAC input
19	VDDPLL	Supply		Analog power supply bandgap, DCXO/PLL, 2.5V
20	XTAL1	AI		Oscillator crystal pin 1
21	XTAL2	AI		Oscillator crystal pin 2
22	VDD5	Supply		Analog power supply bandgap, DAC , 5V
23	CLKION	AI/O		Clock synchronization input/output 2
24	CLKIOP	AI/O		Clock synchronization input/output 1
25	VDDxIF	Supply		Digital power supply data interface
26	ADC13	DO		Data 13, ADC/Decimator output
27	ADC12	DO		Data 12, ADC/Decimator output
28	ADC11	DO		Data 11, ADC/Decimator output
29	ADC10	DO		Data 10, ADC/Decimator output
30	ADC9	DO		Data 9, ADC/Decimator output
31	ADC8	DO		Data 8, ADC/Decimator output
32	ADC7	DO		Data 7, ADC/Decimator output
33	VDD5IF	Supply		Digital power supply
34	VDDDIG	Supply		Digital power supply , 2.5V
35	CLK	DI/O		Master/Slave clock 35MHz
36	VDDxIF	Supply		Digital power supply data interface
37	VDDADC	Supply		Analog power supply ADC, 2.5V
38	ADC6	DO		Data 6, ADC/Decimator output

Pin	Symbol	I/O	Logic	Description
39	ADC5	DO		Data 5, ADC/Decimator output
40	ADC4	DO		Data 4, ADC/Decimator output
41	ADC3	DO		Data 3, ADC/Decimator output
42	ADC2	DO		Data 2, ADC/Decimator output
43	VDDxIF	Supply		Digital power supply data interface
44	ADC1	DO		Data 1, ADC/Decimator output
45	ADC0	DO		Data 0, ADC/Decimator output
46	DOUT	DO		Serial control interface data output
47	DIN	DI		Serial control interface data input
48	VDDVGA	Supply		Analog power supply VGA , 2.5V
49	OUTP2	AO		Positive line driver output 2
50	VDDLD	Supply		Analog power supply line driver , 5V
51	VDDLD	Supply		Analog power supply line driver , 5V
52	OUTN2	AO		Negative line driver output 2
53	OUTP1	AO		Positive line driver output 1
54	VDDLD	Supply		Analog power supply line driver , 5V
55	VDDLD	Supply		Analog power supply line driver , 5V
56	OUTN1	AO		Negative line driver output 1

Note: The device has no dedicated GND-pins. The GND connection is established through the exposed die pad and must be soldered or otherwise connected carefully to the PCB.

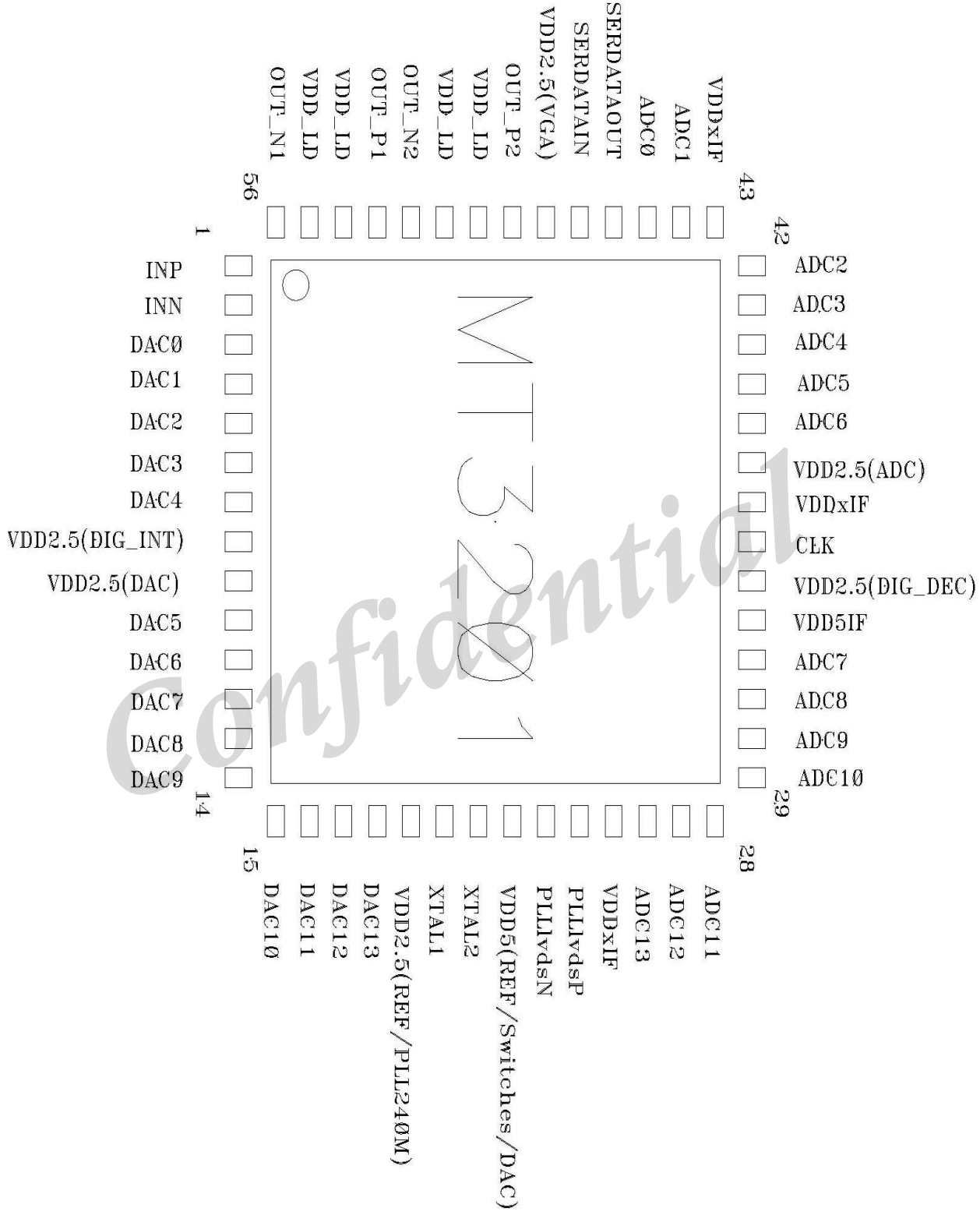

Figure 11 Pin Diagrams

5. Package Information

The MT3201 is packaged in a 8mm×8mm, 56 pin Quad Flat No lead package (QFN) suitable for surface mounting, as shown in Figure 12.

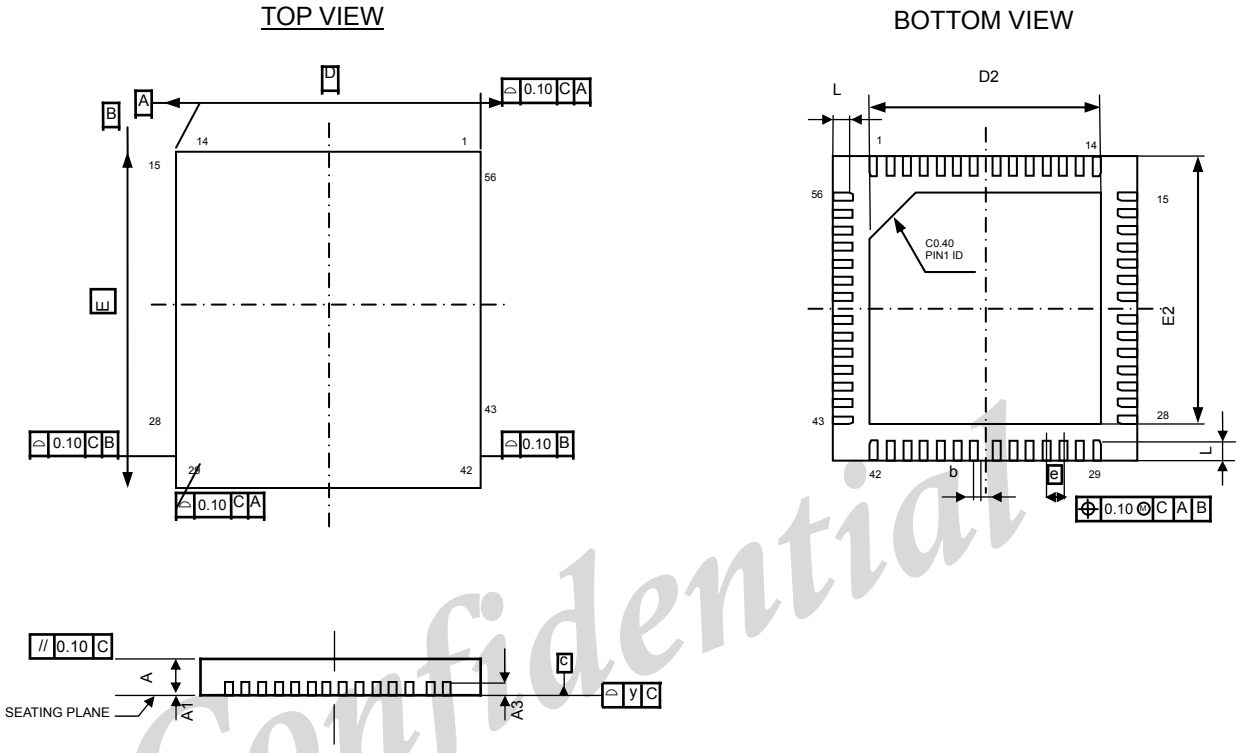

Figure 12 Package

VARIATIONS

SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.6	29.5	31.5
A1	0	0.02	0.05	0	0.79	1.97
A3		0.203 REF			7.99 REF	
B	0.18	0.25	0.30	7.09	9.84	11.81
D		8.00 BSC			314.96 BSC	
D2	6.50	6.65	6.80	255.91	261.81	267.72
E		8.00 BSC			314.96 BSC	
E2	6.50	6.65	6.80	255.91	261.81	267.72
e		0.50 BSC			19.69 BSC	
L	0.35	0.40	0.45	13.78	15.75	17.72
y		0.08			3.15	

NOTE:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. REFER TO JEDEC STD. MO-220
3. DIMENSION “b” APPLINES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.18 AND 0.30mm FROM TERMINAL TIP.
4. LEADFRAME MATERIAL IS OLIN194 AND THICKNESS IS 0.203mm (8 MIL)

6. Ordering Information

Prefix	Part No. (4 numbers)	Package			Version
		RoHS or Not	Package Type		
MT	3201	G: **Green Product** N: **Pb Product**	N: **QFN** P: **QFP** L: **LQFP** C: **CHIP** B: **BGA**	-	B1

Part Number

- MT3201GN-B1: 1 port VDSL1 AFE chip with QFN56 package