Merlin Device

Single VDSL2 Analog Front End Chip

MT3301

Data Sheet

義傳科技股份有限公司
Metanoia Communications Inc.

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Single VDSL2 AFE Chip

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PRODUCT PREVIEW

General Description

The MT3301 is a highly integrated Analog Front End (AFE) for VDSL2 application which provides all analog functions necessary for receiving and transmitting VDSL2 data according to ETSI and ANSI. The high integrity with low distortion and noise reduces the need for complex and costly external components. A serial control interface allows the software programming of various functional blocks. Power back off combined with power down for each block provides the flexible power saving policy. An on-chip clean up PLL provides all the required internal clocks. As single port device it is intended to be used in customer premises equipment (CPE). The full 8MHz/12MHz/17MHz/30MHz bandwidth support in downstream and upstream direction also allows the use in central office (CO).

Key Features

- Highly integrated VDSL2 Analog Front End (AFE) including line driver
- 5V/2.5V dual analog supply for high efficiency line driver
- Digital I/O supply variable from 1.2V up to 3.3V
- Supports 2, 3, 4, 5 and 6 bands of operation (U0 optional)
- I/O data stream at 35 MSPS / 70MSPS
- 14-bit resolution / 12-bit accuracy DAC with low out of band noise fitting PSD masks
- 4th order programmable low-pass filter
- Variable gain amplifier (VGA) with up to 35dB gain
- 14-bit resolution / 12-bit accuracy ADC with sophisticated Sigma-Delta architecture
- On-chip clean-up PLL
- Minimum of external components necessary
- Various power saving modes
- 35.328MHz crystal reference oscillator
- All functions controllable through serial bus interface

Applications

- VDSL2/ADSL2+ CO
- VDSL2/ADSL2+ CPE
- Power line networking
- HPNA
- MDU/MTU applications

TABLE OF CONTENTS

1 General Description 1
1-1 MT3301 Key Features 2
1-2 MT3301 Applications 2
1-3 MT3301 Application Block Diagram 2
2 Functional Description 3
2-1 Overview 3
2-2 Transmit Path 4
2-2-1 Interpolation Filter 4
2-2-2 Digital to Analog Converter 4
2-2-3 Power Back Off 4
2-2-4 Line Driver 4
2-3 Receive Path 5
2-3-1 Variable Gain Amplifier 5
2-3-2 Analog to Digital Converter/Decimation Filter 5
2-4 Common Blocks 6
2-4-1 Crystal Oscillator 6
2-4-2 TX and RX Data I/O 7
2-4-3 Serial Control Interface 7
2-5 Programming 8
2-5-1 Chip Register Addresses 8
2-5-2 Address 0 (VGA/Filter) 9
2-5-3 Address 1 (ADC/VGA2) 10
2-5-4 Address 2 (DCXO Frequency Adjustment) 11
2-5-5 Address 3 (DAC/Post Filter/Line Driver) 11
2-5-6 Address 4 (Bias/Reference) 13
2-5-7 Address 5 (PLL/DCXO 2) 14
2-5-8 Address 6 (Digital Circuit/POFI Power Saving) 15
2-5-9 Address 7 (Others) 16
3. Parameters 17
3-1 Absolute Maximum Ratings 17
3-2 Operating Conditions 17
3-3 Thermal Resistance 17
3-4 Electrical Characteristics 18
4. Pin Description 21
5. Package Information 24
6. Ordering Information 25

LIST OF FIGURES

Figure 1 Typical CPE Application Block Diagram....2
Figure 2 Functional Block Diagram....3
Figure 3 Block Diagram of Transmit Path....4
Figure 4 Block Diagram of Receive Path....5
Figure 5 Oscillator/PLL Block Diagram....6
Figure 6 Serial Control Interface Protocol....7
Figure 7 Data and control interface timing....20
Figure 8 Pin Diagrams....23
Figure 9 Package....24

1 General Description

The MT3301 is a highly integrated Analog Front End (AFE) for VDSL2 application which provides all analog functions necessary for receiving and transmitting VDSL2 data according to ETSI and ANSI. The high integrity with low distortion and noise reduces the need for complex and costly external components. A serial control interface allows the software programming of various functional blocks. Power back off combined with power down for each block provides the flexible power saving policy. An on-chip clean up PLL provides all the required internal clocks. As single port device it is intended to be used in customer premises equipment (CPE). The full 8MHz/12MHz/17MHz/30MHz bandwidth support in downstream and upstream direction also allows the use in central office (CO).

In transmit path, it includes an interpolation filter, a 14-bit DAC, a smoothing LPF, a HPF, and a high performance line driver. The transmit signal bandwidth can be as wide as 30MHz with high linearity. An additional HPF is used to prevent the residual side-lobe from interfering in POTS. A programmable attenuation is designed from 0dB down to -20dB in 0.5dB steps. The HPF output can serve as the input to an external line driver if needed, or it can be the input of the internal line driver. The internal line driver provides sufficient power settings required by the VDSL2 standards for PSD masks.

The receive path consists of a variable gain amplifier (VGA), an anti-aliasing LPF, a HPF, a sophisticated 14-bit ADC and a decimation filter. The VGA has a minimum gain setting of -6dB and a maximum of 35dB. The HPF cutoff frequency can be set from 32kHz to 3MHz which do more echo rejection from transmit band.

The MT3301 AFE provides highly integrated solution for VDSL2. It is available in a space saving, 64pin QFN, and is specified over the commercial (-40C to +85C) temperature range.

1-1 MT3301 Key Features

- Highly integrated VDSL2 Analog Front End (AFE) including line driver
- 5V/2.5V dual analog supply for high efficiency line driver
- Digital I/O supply variable from 1.2V up to 3.3V
- Supports 2, 3, 4, 5 and 6 bands of operation (U0 optional)
- I/O data stream at 35 MSPS / 70MSPS
- 14-bit resolution / 12-bit accuracy DAC with low out of band noise fitting PSD masks
- 4th order programmable low-pass filter
- Variable gain amplifier (VGA) with up to 35dB gain
- 14-bit resolution / 12-bit accuracy ADC with sophisticated Sigma-Delta architecture
- On-chip clean-up PLL
- Minimum of external components necessary
- Various power saving modes
- 35.328MHz crystal reference oscillator
- All functions controllable through serial bus interface

1-2 MT3301 Applications

- VDSL2/ADSL2+ CO
- VDSL2/ADSL2+ CPE
- Power line networking
- HPNA
- MDU/MTU applications

1-3 MT3301 Application Block Diagram

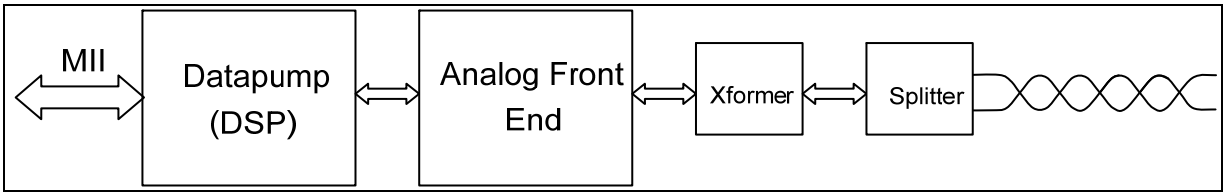

Figure 1 Typical CPE Application Block Diagram

2 Functional Description

2-1 Overview

The MT3301 incorporates a fully integrated AFE with line driver compliant to the ITU standard[1]. TX and RX paths can work fully independent but share common blocks like the PLL and the serial bus interface. The absence of nearly all external components and the low pin count in combination with the small package outline contributes to a very dense board layout.

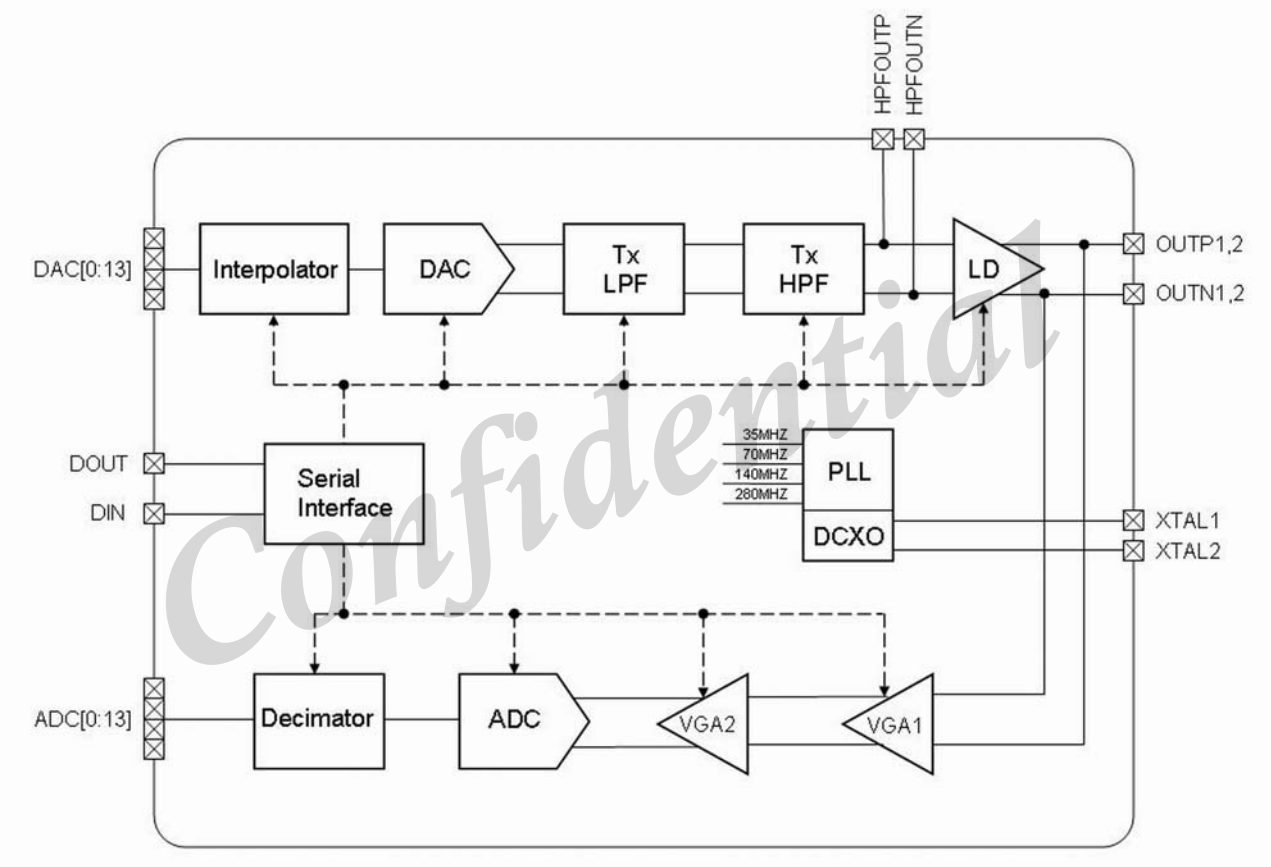

Figure 2 Functional Block Diagram

[1] Band allocations e.g. frequency plans A, B, etc are supported but the separation of up- and downstream has to be performed by the DSP.

2-2 Transmit Path

The MT3301 transmit path consists of 5 blocks: a digital interpolation filter, a current steering DAC, a 4th order post low pass filter (LPF), a high pass filter (HPF), and a high performance line driver.

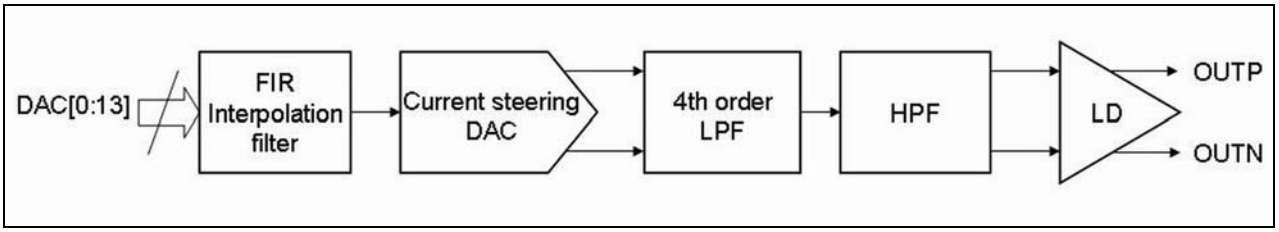

Figure 3 Block Diagram of Transmit Path

2-2-1 Interpolation Filter

The interpolation filter receives a 14-bit wide data stream in two's complement at 35.328MSPS/70.656MSPS, and is programmable for application of 8MHz/12MHz/17MHz/30MHz signal bandwidth. It relaxes the following LPF requirement by suppressing the image signal and increasing the LPF's transition band simultaneously. To attenuate images, the filter has an up-sampled output of 141.312MSPS/282.624MSPS which feeds the current steering DAC.

2-2-2 Digital to Analog Converter (DAC)/TX Post Low Pass Filter/TX High Pass Filter

The DAC is a 14-bit resolution current steering DAC which operates at 141.312MHz/ 282.624MHz with 12-bit accuracy. The 4th order continuous-time post low pass filter following the DAC guarantees the required suppression of all out-of-band images and noise. The HPF reduces the side-lobe signal that might interfere in POTS. The typical corner frequencies of LPF and HPF are kept within a ±7% range by means of an automatic RC-time constant adjustment during power-up. The output of HPF can serve as the input to an external line driver or to the internal line driver.

2-2-3 Power Back Off

To allow a power back off (PBO) for line power, a programmable attenuation is realized from 0dB down to -20dB in 0.5dB steps. To keep the DAC operating with the optimal S/N conditions, this attenuation is mainly realized in the post-filter block. If again finer attenuation steps are necessary, digital attenuation using the DSP can be used in conjunction with the analog attenuation.

2-2-4 Line Driver

The line driver takes its input signal from the high pass filter. The fully integrated line driver reaches an extremely high linearity by means of a sophisticated compensation technique, whereby additional outputs and external circuitry are needed. To minimize the power consumption, 40% of the output impedance is synthesized. This configuration allows a highly efficient line driver design with a single 5V supply only. The necessary amplifier feedback path is also used as the input of the receive path. The integrated line driver provides sufficient power settings required by the

VDSL2 standards for PSD masks. A properly selected line driver can be connected externally if larger power is needed.

2-3 Receive Path

The receive path consists of a two stage variable gain amplifiers (VGA), a continuous time sigma-delta ADC, and a digital decimation filter.

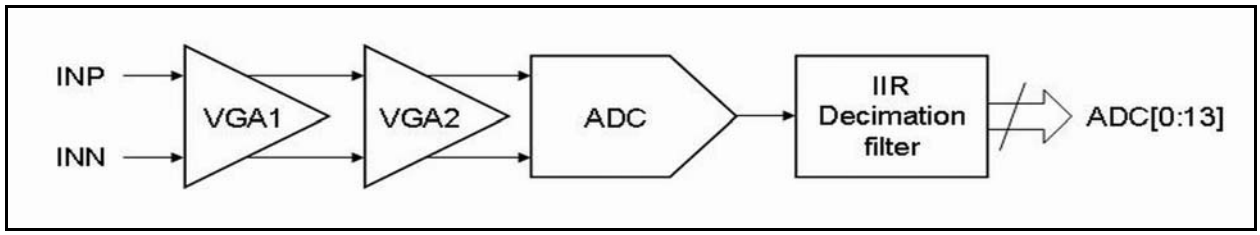

Figure 4 Block Diagram of Receive Path

2-3-1 Variable Gain Amplifier

The VGA is used to adapt the dynamic range of the received signal to best fit the S/N and dynamic range requirements of the ADC. A first order high pass filter located in the VGA attenuates the remaining signal of the first down-stream band D1. Hence, the hybrid performance can be optimized to reduce the remaining echo resulting in an improved overall rejection.

The VGA has a minimum gain setting of -6dB and a maximum of 35dB. The gain step is 1 dB between 12 and 35 dB gain. Below 12dB gain, 2dB steps are possible and the first VGA is bypassed.

2-3-2 Analog to Digital Converter/Decimation Filter

The 12-bit accurate Analog to Digital Converter is implemented as a continuous time Sigma-Delta modulator with subsequent decimation stages. The 30MHz analog bandwidth modulator uses a sampling frequency of 280MHz. The 6 bit output of the modulator passes through a SINC and an IIR-filter. This filter delivers a 14-bit wide 35.328MSPS/70.656MSPS output stream in two's complement. This filter is programmable for applications of 8MHz/12MHz/17MHz/30MHz signal bandwidth.

2-4 Common Blocks

2-4-1 Crystal Oscillator

The reference-oscillator requires a 35.328MHz crystal to be connected between pins XTAL1 and XTAL2. To compensate for the tolerances of the crystal, the oscillator allows a frequency adjustment by switching internal capacitors within a range from 6pf to 38pf in about 5fF-steps at both XTAL1/2 pins. The resulting frequency range of the adjustment ultimately depends on the crystal's equivalent circuit. Typical values are ±200ppm frequency range.

This adjustment can also be used to synchronize the modem timing with the system wide timing.

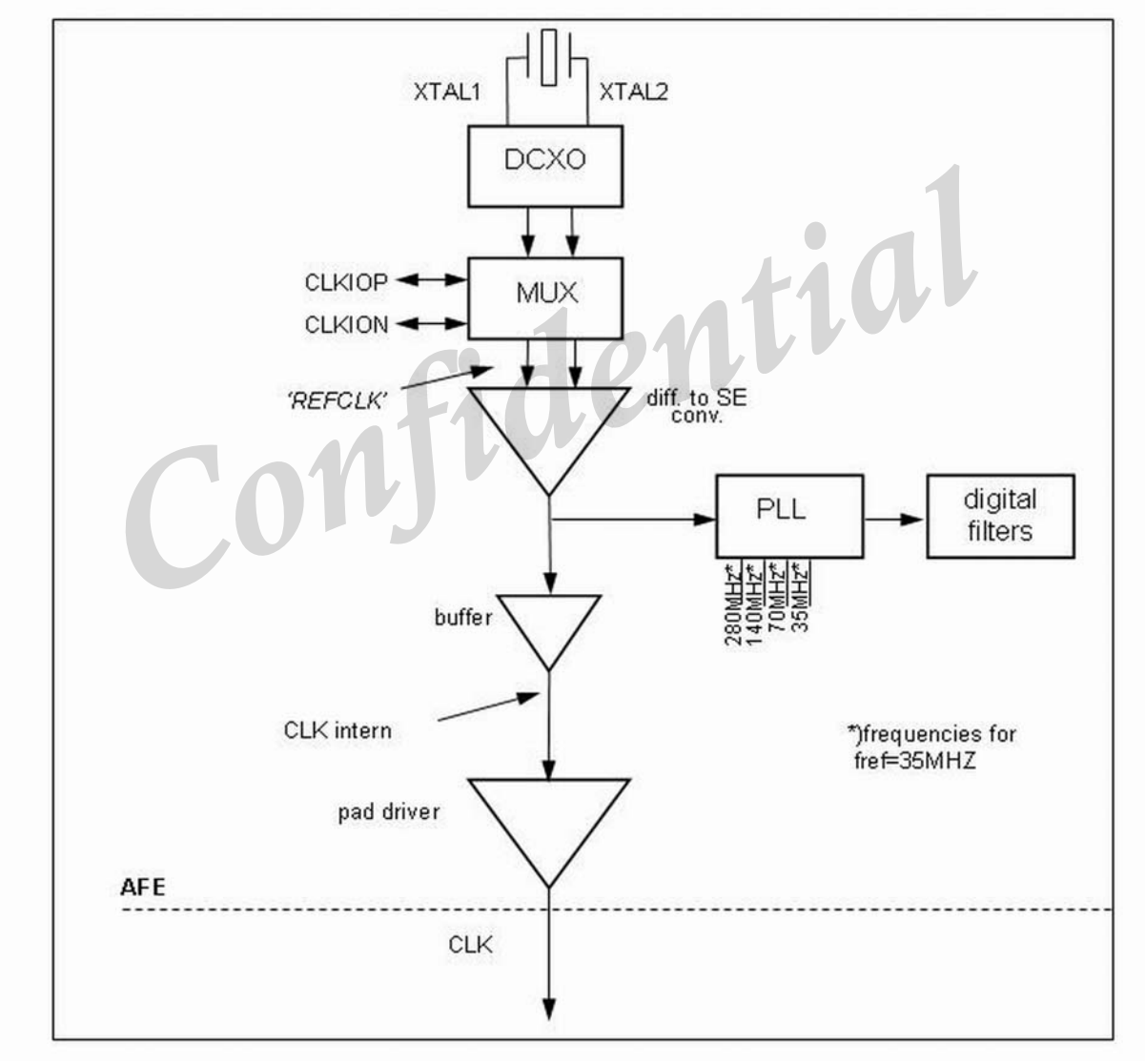

Figure 5 Oscillator/PLL Block Diagram

2-4-2 TX and RX Data I/O

The TX and RX data between the DSP and the AFE is exchanged at a sample rate of 35.328MSPS or 70.656MSPS. Synchronization is guaranteed by the system wide 35.328MHz clock (pin CLK).

2-4-3 Serial Control Interface

The serial control interface consists of the three connections CLK, DIN and DOUT. The CLK is the system wide 35.328MHz reference clock provided through the AFE. The DIN line carries information from the DSP to the AFE, whereas DOUT transfers information from the AFE to the DSP.

The protocol comprises of

1 startbit`0`,

a data word of
12-bit data d11-d0 (in case of a 'Read' command the data won't be evaluated),

and register/ command bits with
3-bit register address a2-a0 and
1-bit R/W, Read=0, Write=1.

The protocol is shown in Figure 6: Serial Control Interface Protocol.

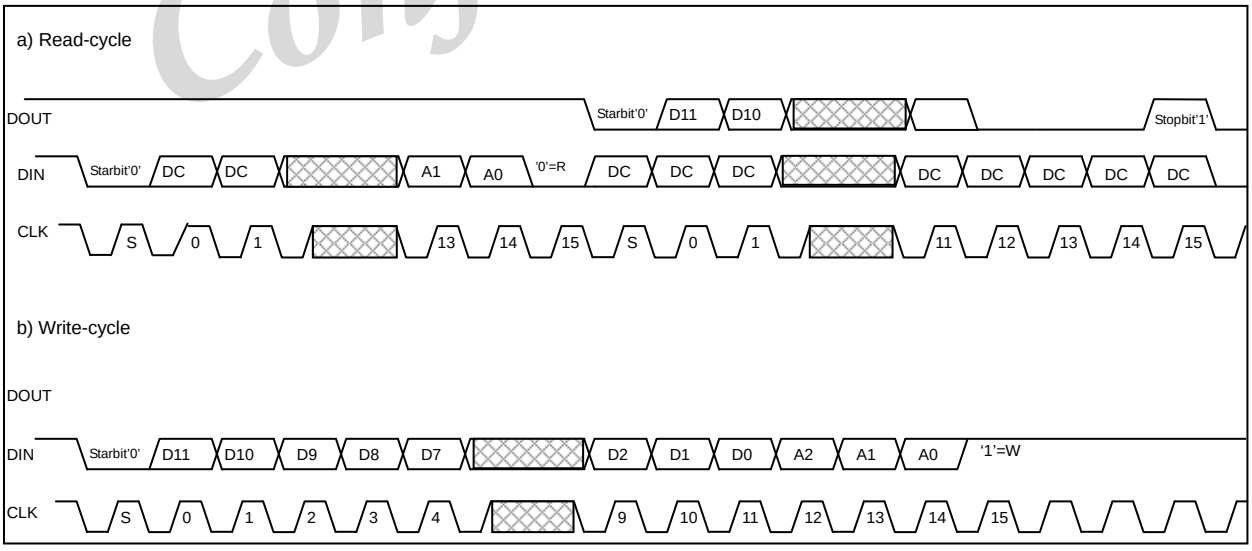

Figure 6 Serial Control Interface Protocol

When the DSP needs to read back the data from the AFE, a "Read" command is initiated. One clock cycle later, the AFE will transmit on a dedicated pin DOUT, starting with a startbit '0', the 12-bit data word d11-d0 of the specified

address a2-a0 followed by 3 ‘0’ and a stopbit ‘1’.

The serial interface allows the programming of the functions of the constitutive blocks, e.g. power down and gain settings.

2-5 Programming

2-5-1 Chip Register Addresses

The default values of all register bits at power on is “0”. When register setting instructions given in this document make no mention of certain bits, they must be left or set to “0”.

Register#	Block (Function)
000 (0)	VGA
001 (1)	ADC/VGA
010 (2)	DCXO frequency adjustment
011 (3)	DAC/Post filter/Line driver
100 (4)	Bias/References
101 (5)	PLL/DCXO2
110 (6)	Reserved*)
111 (7)	Miscellaneous

***)Note:** Register 6 contains bit setting for control during test. They are for internal use only and must be set to “0”.

2-5-2 Address 0 (VGA/Filter)

Function	11	3
TX High Pass Filter Corner Frequency		
32KHz	0	0
138KHz	0	1
276KHz	1	0
3MHz	1	1

Function	10	9	8	7
VGA Gain 1				
-6dB	0	0	0	0
Not Allowed	0	0	0	1
0dB	0	0	1	0
Not Allowed	0	0	1	1
Not Allowed	0	1	0	0
Not Allowed	0	1	0	1
6dB	0	1	1	0
Not Allowed	0	1	1	1
12dB	1	0	0	0
13dB	1	0	0	1
18dB	1	0	1	0
19dB	1	0	1	1
Not Allowed	1	1	0	0
Not Allowed	1	1	0	1
24dB	1	1	1	0
25dB	1	1	1	1

Function	6	5
RX High Pass Filter Corner Frequency		
32KHz	0	0
138KHz	0	1
276KHz	1	0
3MHz	1	1

Function	4
RX Low Pass Filter	
Full Bandwidth (30MHz)	0
Activate 12MHz Low Pass Filter	1

Function	2	1	0
For Internal Use Only			
Must be '111'*)	1	1	1

2-5-3 Address 1 (ADC/VGA2)

Function	11
ADC/VGA Power Down	
ADC/VGA Running	0
ADC/VGA Power Down	1

Function	10	9	8
VGA Gain 2			
0dB	0	0	0
2dB	0	0	1
4dB	0	1	0
4dB	0	1	1
6dB	1	0	0
8dB	1	0	1
10dB	1	1	0
10dB	1	1	1

***)Note:** Underlined settings are recommended settings. If no indication is given the setting is according to application requirements.

2-5-4 Address 2 (DCXO Frequency Adjustment)

Function	11	10	9	…	2	1	0
Crystal Oacillator Frequency Adjustment							
0fF	0	0	0	…	0	0	0
5fF	0	0	0	…	0	0	1
10fF	0	0	0	…	0	1	0
…							
…							
…							
…							
20.470pF	1	1	1		1	1	0
20.475pF	1	1	1		1	1	1

2-5-5 Address 3 (DAC/Post Filter/Line Driver)

Function	11
DAC/Post Filter Power Down	
DAC/Post Filter Running	0
DAC/Post Filter Power Down	1

Function	10	9
Power Back Off (PBO), Coarse Steps		
0dB	0	0
-4dB	0	1
-8dB	1	0
-12dB	1	1

Function	8	7	6
Power Back Off(PBO), Fine Steps			
0dB	0	0	0
-0.5dB	0	0	1
-1dB	0	1	0
-1.5dB	0	1	1
-2dB	1	0	0
-2.5dB	1	0	1
-3dB	1	1	0
-3.5dB	1	1	1

Function	5
Line Driver (LD) Power Down	
LD Power Down	0
LD Running	1

Function	4	3
Output Impedance during Power Down		
Infinite	0	0
128 Ohm	0	1
128 Ohm	1	0
64 Ohm	1	1

Function	2
Failure Protection	
Over Temperature and Over Current Protection Active	0
Over Temperature and Over Current Protection Disable	1

Function	1	0
Line Driver Bias Adjustment		
Standard Current	0	0
Standard Current x 0.5	0	1
Output Stage Current x 0.66	1	0
Standard Current x 0.66 / Output Stage Current x 0.5	1	1

2-5-6 Address 4 (Bias/Reference)

Function	11	10	9	8
TX Voltage Adjustment				
Default	0	0	0	0
Setting ΔV= - 0.9%	0	0	0	1
Setting ΔV= - 1.8%	0	0	1	0
Setting ΔV= - 2.7%	0	0	1	1
Setting ΔV= - 3.6%	0	1	0	0
Setting ΔV= - 4.5%	0	1	0	1
Setting ΔV= - 5.4%	0	1	1	0
Setting ΔV= - 6.3%	0	1	1	1
Setting ΔV=+7.2%	1	0	0	0
Setting ΔV=+6.3%	1	0	0	1
Setting ΔV=+5.4%	1	0	1	0
Setting ΔV=+4.5%	1	0	1	1
Setting ΔV=+3.6%	1	1	0	0
Setting ΔV=+2.7%	1	1	0	1
Setting ΔV=+1.8%	1	1	1	0
Setting ΔV=+0.9%	1	1	1	1

Function	7	6
Bias Current Adjustment		
Default	0	0
+12.5%	0	1
-25%	1	0
-12.5%	1	1

Function	5	4	3
Shutdown Temperature			
181°C	0	0	1
175°C	1	0	1
169°C	0	1	1
163°C	1	1	1
147°C	0	0	0
139°C	1	0	0
125°C	0	1	0
113°C	1	1	0

Function	2
Reference Power Down	
References Running	0
References Power Down	1

Function	1	0
For Internal Use Only		
Must be '00'	0	0

2-5-7 Address 5 (PLL/DCXO 2)

Function	11	10
Crystal Drive Level (Depending on Crystal Type)		
Maximum	0	0
High Medium	0	1
Low Medium	1	0
Minimum	1	1

Function	9
Power Down	
PLL Running	0
PLL Power Down	1

Function	8
PLL Mode	
Automatic Startup Procedure Enabled	0
Manual Startup	1

Function	7	6
Charge Pump Current		
20uA	0	0
30uA	0	1
50uA	1	0
140uA	1	1

Function	5
Reference Frequency Selection	
Reference is 30.240MHz	0
Reference is 35.328MHz	1

Function	4
Freeze Tuning	
Tuning Running	0
Tuning Frozen	1

Function	3
External 280MHz CLK	
Disable	0
Enable	1

Function	2
Bias Current for VCO	
5.2mA	0
8.6mA	1

Function	1	0
For Internal Use Only		
Must be '00'	0	0

2-5-8 Address 6 (Digital Circuit/POFI Power Saving)

Function	11	10	9	8	7	6
For Internal Use Only						
Must be '000000'	0	0	0	0	0	0

Function	5	4	3	2	1	0
For Internal Use Only						
Must be '000000'	0	0	0	0	0	0

2-5-9 Address 7 (Others)

Function	11
Line Driver (LD) Power Gain*)	
High Gain	0
Low Gain	1

Function	10
External Line Driver (LD) Power Down	
External LD Running	0
External LD Power Down	1

Function	9
Operation Mode Selection	
8a/8b/12a/17a Profile	0
30a Profile	1

Function	8	7	6	5	4	3	2	1	0
For Internal Use Only									
Must be '000000'	0	0	0	0	0	0	0	0	0

***)Note:** Bit 11 controls the maximum power that line driver can provide. If the turns ratio of the transformer is 1:7, high gain provides 20.5 dbm maximum power, low gain provides 14.5 dbm. If the ratio is 1:4, high gain provides 14.5 dbm maximum power.

3. Parameters

3-1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{STG}	Storage Temperature		-65		125	℃
T_J	Junction Temperature		-40		125	℃
V_{ESD}	Electrostatic Discharge Voltage Capability	HBM Mil.Std 883			2	kV

3-2 Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD-A1}	Analog supply voltage DAC,LD			5		V
V_{DD-A2}	Analog supply voltage VGA,ADC,PLL			2.5		V
V_{DD-D}	Digital core supply voltage			2.5		V
$V_{DD-I/O}$	I/O-supply voltage		1.1		3.5	V
T_{AMB}	Ambient temperature		-40	25	85	℃

3-3 Thermal Resistance

Parameter	SYM	Condition	Min.	Typ.	Max.	Unit
Thermal resistance Junction to ambient	θja	4 layer PCB, 0m/s airfolw	-	25.89	-	℃/W
Thermal resistance Junction to case	θjc	4 layer PCB, 0m/s airfolw	-	2.47	-	℃/W

3-4 Electrical Characteristics

Standard conditions unless otherwise stated: V_{DD-A1}=5V, V_{DD-A2}=2.5V, V_{DD-D2}=2.5, $V_{DD-I/O}$=1.2V, T_A=25℃, Crystal oscillator frequency 35.328MHZ

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD-A1}	Analog supply voltage DAC,LD		4.75	5	5.25	V
V_{DD-A2}	Analog supply voltage VGA,ADC,PLL		2.375	2.5	2.625	V
V_{DD-D}	Digital core supply voltage		2.375	2.5	2.625	V
$V_{DD-I/O}$	I/O-supply voltage		1.1		3.5*	V
$P_{SUPPLY1}$	Power consumption	@ 14.5dBm line power, 14.5db Crest factor		1440		mW
	Transmit path					
DR_{TX}	Input data rate	different data rate for different profile	35.328	-	70.656	MS/s
Res_{TX}	Resolution		-	14	-	bits
$V_{outmaxTX}$	Max. output voltage	@ 0dBfs, PBO=0dB, concept of synthesized impedance	8			V_{dpp}
$V_{outCMTX}$	Common mode output voltage			V_{DD-A1} /2		V
$I_{outmaxTX}$	Max. output current		800			mA
PSD_{IBLTX}	Output noise in-band	line referred, 138kHz..30MHz		-128		dBm/Hz
PSD_{OBLTX}	Output noise out-of-band	line referred, > 30MHz		-128		dBm/Hz
f_{lowTX}	Signal bandwidth lower corner frequency			32		kHz
f_{highTX}	Signal bandwidth upper corner frequency		30			MHz
PBR_{TX}	Passband ripple			0.5		dB
THD_{TX-3}	Total harmonic distortion	f_{in}=1,4,6,10MHz @ -3dBfs harmonics in band			-70	dBc
MBD_{TX}	Missing band depth			55		dB
GR_{PBO}	Power back off range		-14.5		0	dB
SS_{PBO}	PBO step size			0.5		dB
SS_{PBOADJ}	PBO accuracy		-0.5		0.5	dB

*The supply voltage for the digital I/O's can take any voltage between 1.1V and 3.5V.

Electrical Characteristics cont.

Symbol	Receive path	Condition	Min	Typ	Max	Unit
DR_{RX}	Output data rate	different data rate for different profile	35.328	-	70.656	MS/s
Res_{RX}	Resoltion		-	14	-	bits
$V_{inmaxRX}$	Max. input voltage	VGA gain = 0dB		3.6		V_{dpp}
GR_{VGA}	VGA gain range		-6		35	dB
SS_{VGA}	VGA step size	Gain -6dB through + 12dB Gain +12dB through + 35dB		2 1		dB dB
SS_{VGAADJ}	VGA accuracy		-0.5		0.5	dB
f_{lowRX}	Signal bandwidth lower corner frequency			32		kHz
f_{highRX}	Signal bandwidth upper corner frequency		30			MHz
PBR_{RX}	Passband ripple			1		dB
$SFDR_{RX}$	Spurious free dynamic range	fref =1 MHz		-70		dBc
THD_{RX-3}	Total harmonic distortion	f_{in} =1,4,6,10MHz @ -3dBfs			-70	dBc
PSD_{LRX}	Input noise	line referred		-135		dBm/Hz
MBD_{RX}	Missing band depth			55		dB
	Xtal oscillator					
f_{OSC}	Frequency	Xtal TBD		35.328		MHz
ΔC_{trim}	Capacitor trimming range	See section 2-4-1	6		38	pF
	Digital I/O's					
V_{IH}	Input 'high'		$V_{DD-I/O}$ *0.8			V
V_{IL}	Input 'low'				$V_{DD-I/O}$ *0.2	V
V_{OH}	Output 'high'		$V_{DD-I/O}$ -0.1			V
V_{OL}	Output 'low'				0.1	V
C_{in}	Input capacitance				5	pF
C_{load}	Output capacitance	@ 60MHz signal			30	pF
	I/O timing					
T_{CLK30}	Clock period	CLK30=1/f_{OSC}		28.306		ns
DC	Clock duty cycle	CLK30		50		%
T_R/T_F	Rise/fall time	20% to 80%		2.5		ns
$T_{invalidADC}$	Invalid time ADC,DOUT	See Figure 7	0		6	ns
$T_{setupdac}$	Setup time DAC		12			ns
$T_{holddac}$	Hold time DAC		0			ns

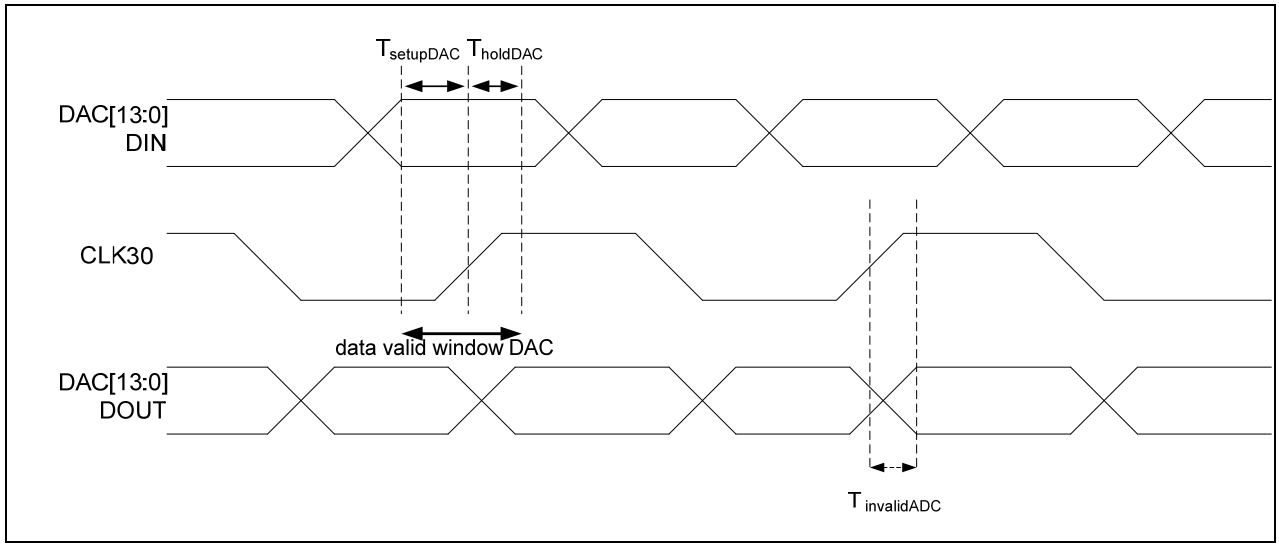

Figure 7 Data and control interface timing

4. Pin Description

Pin	Symbol	I/O	Logic	Description
1	fbP/VGAINP	AI		Internal LD Feedback Input P / VGA Input P
2	NC	-		-
3	fbN/VGAINN	AI		Internal LD Feedback Input N / VGA Input N
4	NC	-		-
5	NC	-		-
6	NC	-		-
7	DAC0	DI		Data 0,Interpolator/DAC input
8	DAC1	DI		Data 1,Interpolator/DAC input
9	DAC2	DI		Data 2,Interpolator/DAC input
10	DAC3	DI		Data 3,Interpolator/DAC input
11	DAC4	DI		Data 4,Interpolator/DAC input
12	VDDDIG	Supply		Digital power supply,(2.5V)
13	VDDDAC	Supply		Analog power supply DAC,(2.5V)
14	DAC5	DI		Data 5,Interpolator/DAC input
15	DAC6	DI		Data 6,Interpolator/DAC input
16	DAC7	DI		Data 7,Interpolator/DAC input
17	DAC8	DI		Data 8,Interpolator/DAC input
18	DAC9	DI		Data 9,Interpolator/DAC input
19	DAC10	DI		Data 10,Interpolator/DAC input
20	DAC11	DI		Data 11,Interpolator/DAC input
21	DAC12	DI		Data 12,Interpolator/DAC input
22	DAC13	DI		Data 13,Interpolator/DAC input
23	VDDPLL	Supply		Analog power supply bandgap,REF/DCXO/PLL,(2.5V)
24	XTAL1	AI		Oscillator crystal pin 1
25	XTAL2	AI		Oscillator crystal pin 2
26	VDD5	Supply		Analog power supply bandgap,REF/Switches/DAC,(5.0V)
27	VDDxIF	Supply		Digital power supply data interface, (3.3V)
28	ADC13	DO		Data 13,ADC/Decimator output
29	ADC12	DO		Data 12,ADC/Decimator output
30	ADC11	DO		Data 11,ADC/Decimator output
31	ADC10	DO		Data 10,ADC/Decimator output
32	ADC9	DO		Data 9,ADC/Decimator output
33	ADC8	DO		Data 8,ADC/Decimator output
34	ADC7	DO		Data 7,ADC/Decimator output
35	EXT LD PD	DO		External LD powerdown control
36	VDD5IF	Supply		Digital power supply, (5.0V)
37	VDDDIG	Supply		Digital power supply, (2.5V)
38	DECvss1	Supply		Digital power supply,GND

Pin	Symbol	I/O	Logic	Description
39	CLK30	DO		Clock 35MHz Out
40	VDDxIF	Supply		Digital power supply data interface,(3.3V)
41	DECvss2	Supply		Digital power supply,GND
42	VDDADC	Supply		Analog power supply ADC,(2.5V)
43	ADC6	DO		Data 6,ADC/Decimator output
44	ADC5	DO		Data 5,ADC/Decimator output
45	ADC4	DO		Data 4,ADC/Decimator output
46	ADC3	DO		Data 3,ADC/Decimator output
47	ADC2	DO		Data 2,ADC/Decimator output
48	VSS	Supply		Digital power supply,GND
49	VDDxIF	Supply		Digital power supply data interface,(3.3V)
50	ADC1	DO		Data 1,ADC/Decimator output
51	ADC0	DO		Data 0,ADC/Decimator output
52	SERDATAOUT	DO		Serial control interface data output
53	SERDATAIN	DI		Serial control interface data intput
54	VDDVGA	Supply		Analog power supply VGA,(2.5V)
55	HYB_LDP	AI		Hybrid input P
56	HYB_LDN	AI		Hybrid input N
57	OUTP1	AO		Positive line driver output 1
58	VDDA	Supply		Analog power supply line driver,5.0V
59	VDDA	Supply		Analog power supply line driver,5.0V
60	OUTN1	AO		Negative line driver output 1
61	OUTP2	AO		Positive line driver output 2
62	VDDA2	Supply		Analog power supply line driver,5.0V
63	VDDA2	Supply		Analog power supply line driver,5.0V
64	OUTN2	AO		Negative line driver output 2

***) Note**：Package bottom pad is used as the ground pin as well as the heat sink function. Therefore, it must be assigned and soldered carefully to the PCB.

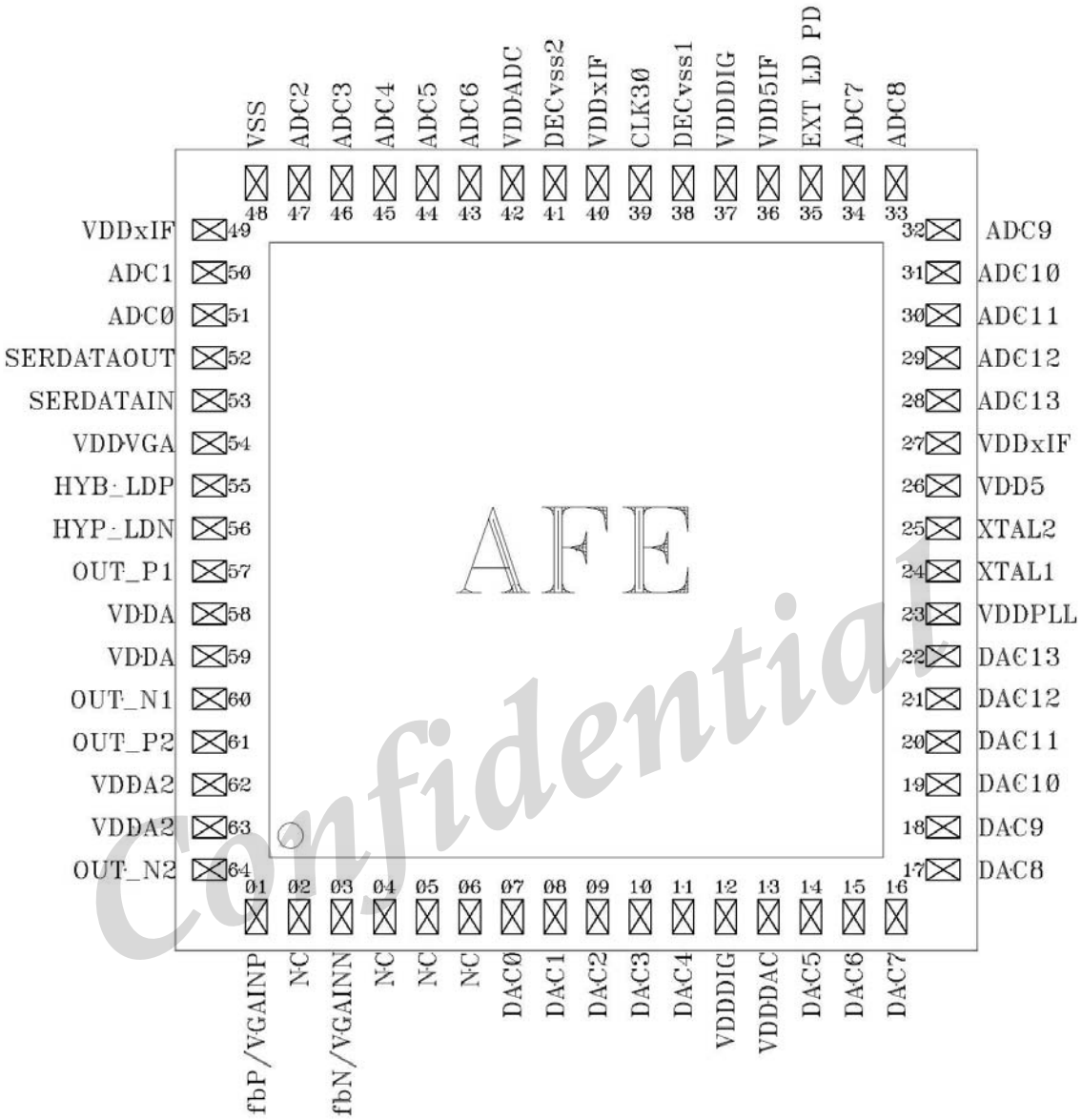

Figure 8 Pin Diagrams

5. Package Information

The MT3301 is packaged in a 9mm×9mm, 64 pin Quad Flat No lead package (QFN) suitable for surface mounting, as shown in Figure 9.

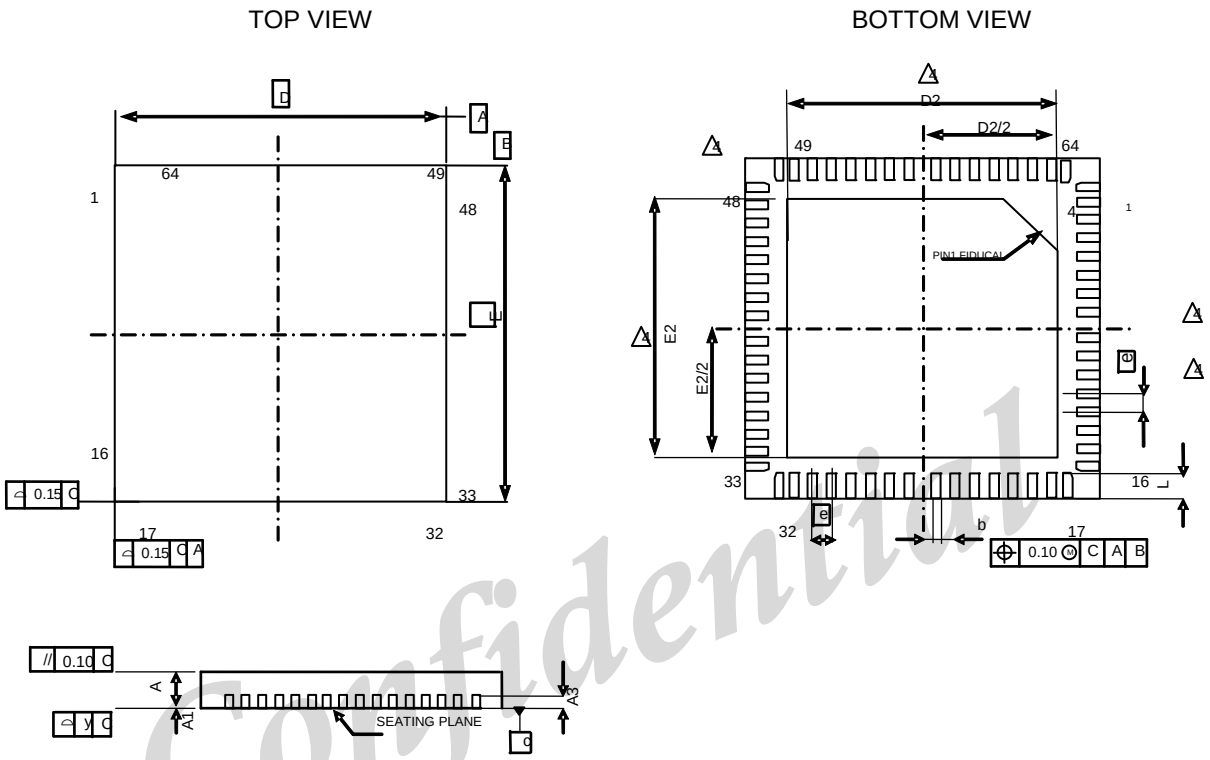

Figure 9 Package

VARIATIONS

SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.6	29.5	31.5
A1	0	0.02	0.05	0	0.79	1.97
A3		0.203 REF			8 REF	
b	0.18	0.25	0.28	7.1	9.8	11.0
D		9.00 BSC			354.3 BSC	
D2	7.20	7.30	7.40	283	287	291
E		9.00 BSC			354.3 BSC	
E2	7.20	7.30	7.40	283	287	291
e		0.50 BSC			19.7 BSC	
L	0.35	0.40	0.45	13.8	15.7	17.7
y		0.08			3.15	

NOTE:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. REFER TO JEDEC STD. MO-220 WMMD
3. DIMENSION “b” APPLINES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL TIP.
4. LEADFRAME MATERIAL IS OLIN194 AND THICKNESS IS 0.203mm (8 MIL)

6. Ordering Information

Prefix	Part No. (4 numbers)	Package		-	Version
		RoHS or Not	Package Type		
MT	3301	G: **Green Product** N: **Pb Product**	N: **QFN** P:**QFP** L: **LQFP** C:**CHIP** B:**BGA**	-	A3

Part Number

■ MT3301GN-A3: 1 port VDSL2 AFE chip with 64-QFN package.