MT5302 Device

Dual Port VDSL2 DMT+AFE Chip

Data Sheet

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Metanoia Communications Inc.

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Dual Port VDSL2 DMT+AFE Chip

MT5302

PRODUCT PREVIEW

General Description

The MT5302 is part of the Metanoia VDSL2 chipset solution. It is a single chip programmable Discrete Multi-Tone (DMT) Digital Subscriber Loop (DSL) digital modulator/ demodulator processor units for broadband access. The Device supports all committee T1E1.4 and ITU-T G.993.2 DSL discrete multi-tone based specifications, as well as IEEE 802.3 10PASS-TS.

Key Features

- Single chip configurable DMT data pump supporting 100Mbps/100Mbps DS/US payload data rate.
- Up to 3072 DMT carriers supported in the downstream and upstream directions.
- All 4096 DMT carriers can be used between U/DS, with four DMT pass-bands per direction
- Conformance to T1E1, ITU-T standards for VDSL2, and current IEEE 802.3ah draft for 10PASS-TS (EFM)
- Configurable band-plan, conforms to NA, EUR and Swedish Band-plans subject to the 3072/4096 and 8-band/4-passband constraints
- Trellis coding support for up to 3072 DMT carriers in any VDSL2 mode.
- Supports Seamless Rate Adaptation (SRA) and Dynamic Rate Repartitioning (DRR)
- Dual latency support with independent interleaver for each path and 128KB on-chip GCI memory
- Flexible QoS classification and queueing supports hardware based latency path routing
- Supports SMII dual port
- No external RAM required. Internal RAM booted from EEPROM, Flash, or external uP
- PHY software and management through IEEE 802.3 MDIO serial or a bi-directional octal interface
- Optimized to support low latency applications as required for voice
- 4 KHz and 8 KHz symbol rates allow variable bandwidth per bin
- 448 LBGA package (LQFP)

Applications

- IP digital Subscriber Loop Access Multiplexer solution
- Multi-Service Access Platforms (MSAP)
- Customer Premise/Located Equipment for Internet Access and VoIP

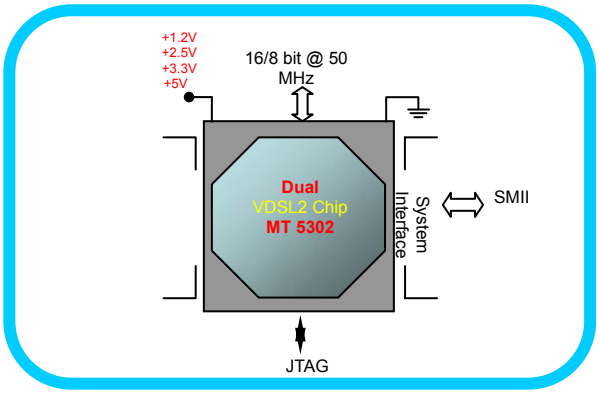

Figure 1 APPLICATION

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1. General Description

1-1 MT5302 Key Features

The MT5302 supports as the following features.

General Device Level

- Single chip configurable DMT processor
- Up to 3072 DMT carriers downstream
- Up to 3072 DMT carriers upstream
- Total DMT carriers U/D are limited to 4096
- Four DMT pass-bands in each direction
- Conformance to T1E1, ITU-T standards for VDSL2
- Conformance to current IEEE 802.3ah draft for 10PASS-TS (EFM)
- Configurable band-plan, conforms to North America, European and Swedish
- Band-plans subject to the 3072/4096 and 4-band /8-passband constraints
- Trellis coding support for up to 3072 DMT bins in any mode including VDSL2
- Programmable soft error detection and correction improves impulse noise rejection
- Supports Seamless Rate Adaptation (SRA) and Dynamic Rate Repartitioning (DRR)
- Dual latency support with independent interleaver for each path and 128KB on-chip GCI memory
- Programmable Upstream Band-split for DMT VDSL2
- Support for one VDSL2 Analog Front End
- IEEE 802.3 support for two SMII.
- Support quality of service (QoS) classification and queueing based on VLAN and Ethertype
- Internal RAM for software stored in external flash or managed through MAC interface
- PHY software and management through IEEE 802.3 MDIO serial or a bi-directional octal interface
- Optimized to support low latency applications, as required for voice
- 4 KHz and 8 KHz symbol rates allow variable bandwidth per bin
- Advanced power management
- 448 LBGA package Highly integrated VDSL2 Analog Front End (AFE) including line driver
- 5V/2.5V dual analog supply for high efficiency line driver
- Digital I/O supply variable from 1.2V up to 3.3V
- Supports 2, 3, 4, 5 and 6 bands of operation (U0 optional)
- I/O data stream at 35 MSPS / 70MSPS
- 14-bit resolution / 12-bit accuracy DAC with low out of band noise fitting PSD masks
- 4th order programmable low-pass filter
- Variable gain amplifier (VGA) with up to 35dB gain
- 14-bit resolution / 12-bit accuracy ADC with sophisticated Sigma-Delta architecture
- On-chip clean-up PLL
- Minimum of external components necessary
- Various power saving modes

- 35.328MHz crystal reference oscillator
- All functions controllable through serial bus interface

1-2 MT5302 Application

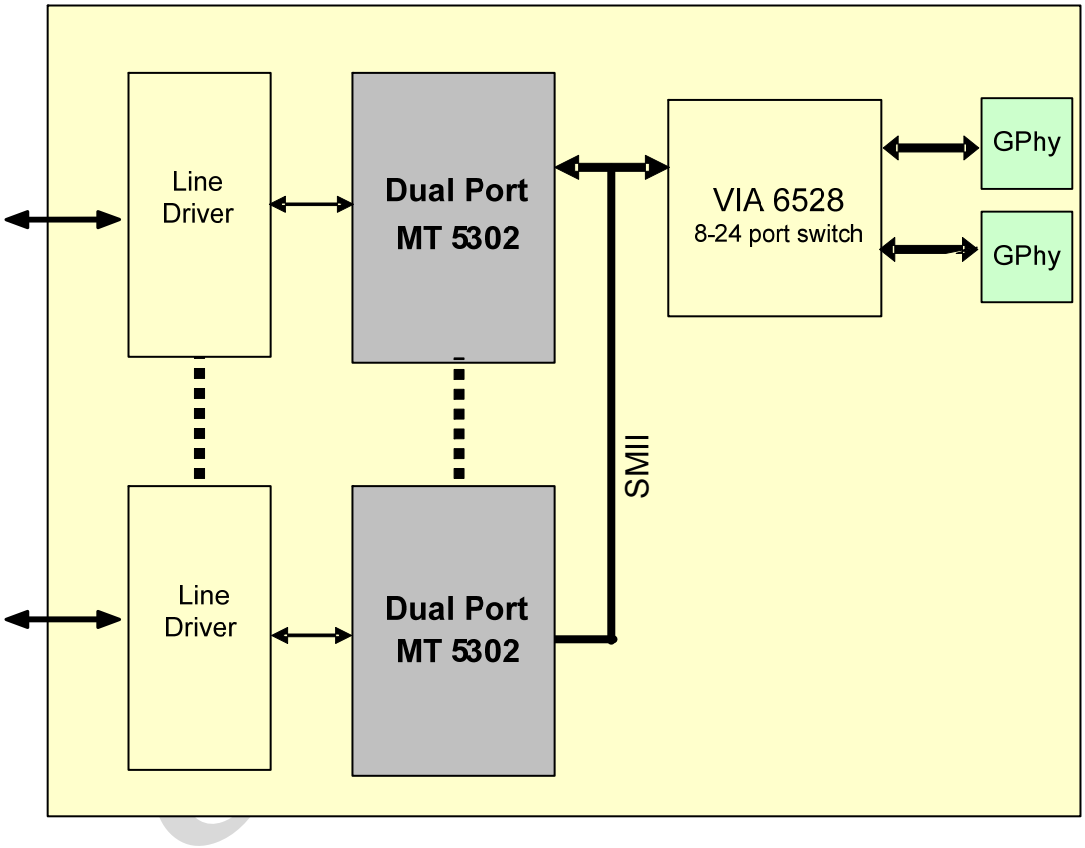


Figure 2 MTU/MDU IP DSLAM/ORD

2. Device Description

2-1 Block Diagram

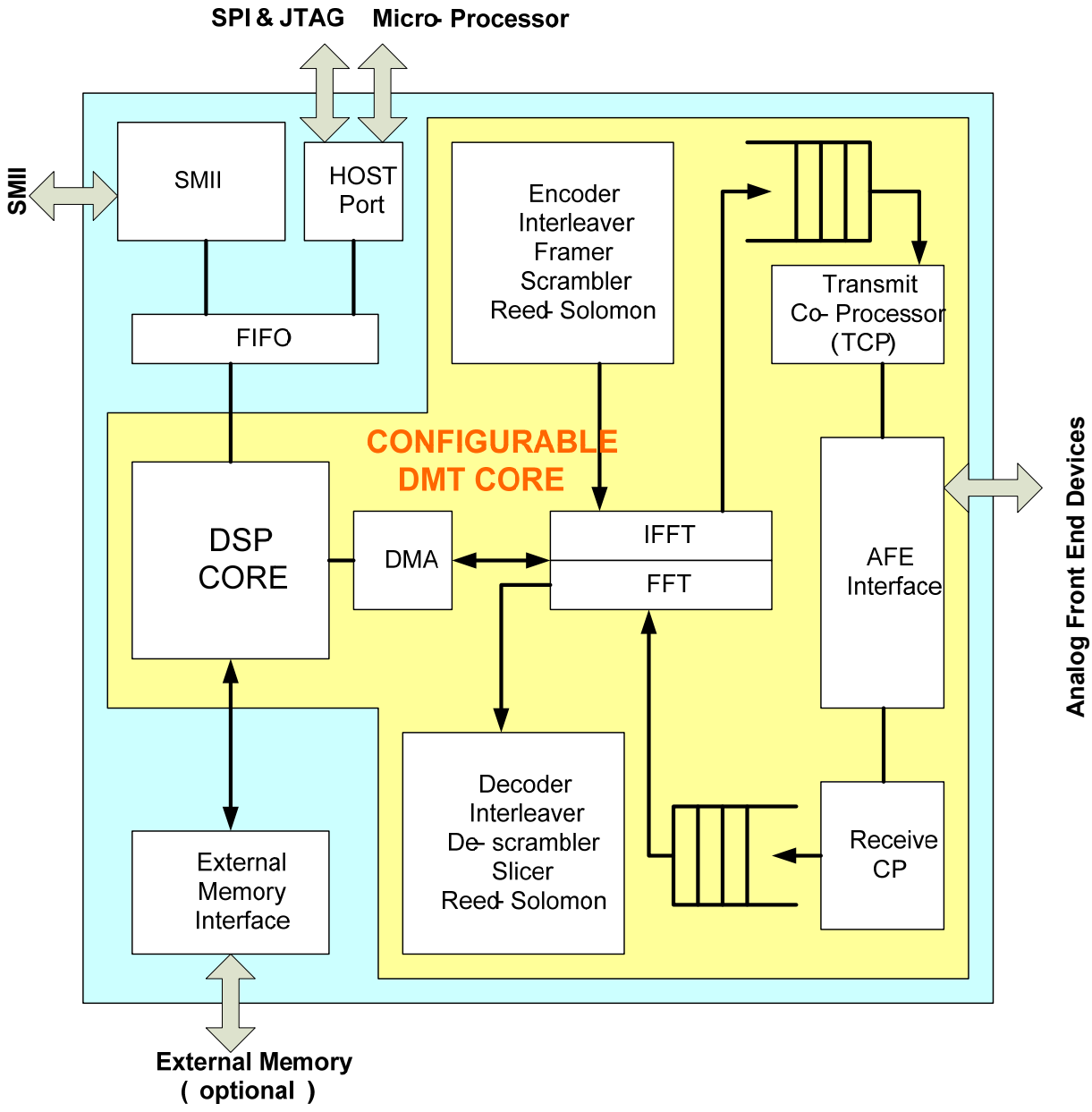


Figure 3 DAC block diagram

2-2 Block Diagram Description

The MT5302 architecture is an area and power efficient implementation of a DMT data pump supporting all VDSL1/2 standards. To meet the high-speed calculation and dataflow requirements of a DMT VDSL2 engine the design was partitioned into a single DSP with multiple hardware coprocessor blocks. The DSP is used for higher-level functions and control while most DMT calculations and data movement are performed in the hardware blocks.

The MT5302 ASIC performs all of the digital functions of a DMT based VTU-O or VTU-R physical interface. This includes all digital processing below the á and â interfaces in the VDSL2 reference model. The device is designed to be inserted into a system 10/100 Ethernet PHY and Ethernet SMII interfaces. The device can be controlled using the MDIO interface or a parallel host interface.

The top-level block diagram for the MT5302 chip is shown in Figure 5. The DSP core employed is compatible with a Motorola 56300 and thus contains an X, Y, and P memory space. All of the memory required for VDSL2 operation is provided on chip but an optional off chip memory can be used to support advanced features. The hardware coprocessors include an Encoder, Decoder, FFT coprocessor, TEQ coprocessor, and an AFE interface control processor. These processors perform all DMT operations from framing to cyclic extension and time domain filtering. The coprocessors are flexible enough to handle current and future DSL configurations but do not require a lot of attention from the DSP.

Each hardware block has a set of registers mapped in the X or Y peripheral address space of the DSP. A peripheral bus interface is used for transferring control information between the DSP and the hardware blocks. The local memory within each hardware block is also indirectly mapped into the peripheral address space via a memory port. This mapping gives the DSP the ability to setup DMA transfers of data to and from the distributed memories. Since a DMA interface is present on each block, DMA transfers can occur between any combination of hardware blocks, external memory, and the DSP. Between 1 and 16 wait states will be inserted per transfer when external memory is accessed using DMA. The number of wait states depends on the speed of the external memory. The external memory interface is provided for test, debug, and system expansion. External memory is not be required for normal VDSL2 DMT calculations.

Due to the high bandwidth requirements at various stages of the transmitter and receiver the DSP is not used for data movement. Instead each hardware block transfers data to the next under DSP control. These transfers are self-managing, controlled by DSP initialized parameters. Hardware flags are used to synchronize timing between processes. The data transfers occur on dedicated interfaces between each hardware block and the next logical block in the path. Since these interfaces are point-to-point, they are much simpler than those used for the bi-directional peripheral and DMA buses. The point-to-point buses are designed to efficiently support the dataflow requirements for Showtime operation. Since the requirements are different during training the point-to-point buses are configurable.
The hardware blocks can be triggered to begin performing calculations by the DSP or by a signal from another hardware block.

The MT5302 incorporates a fully integrated AFE with line driver compliant to the ITU standard[1]. TX and RX paths can work fully independent but share common blocks like the PLL and the serial bus interface. The absence of nearly all external components and the low pin count in combination with the small package outline contributes to a very dense board layout.

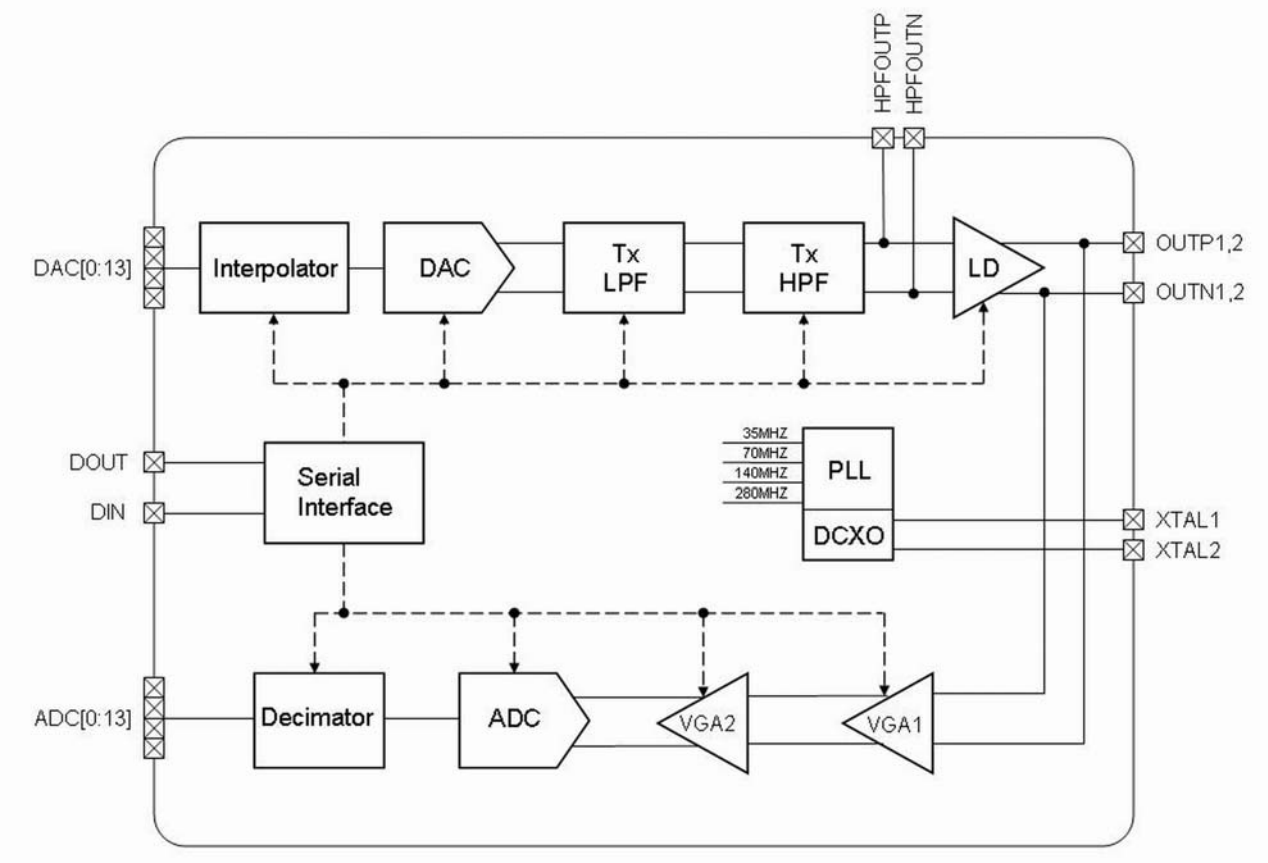


Figure 4 Functional Block Diagram

[1] Band allocations e.g. frequency plans A, B, etc are supported but the separation of up- and downstream has to be performed by the DSP.

2-3 Transmit Path Operation

The data to be transmitted to the remote modem arrives on the MII, SMII, GMII interfaces, and is deposited into a FIFO. Since the Ethernet interfaces aren't normally used simultaneously the FIFO is shared by all interfaces. The FIFO can logically be divided into up to four queues for multichannel operation or to support QoS queueing. The queues can be flexibly mapped into the two available latency paths provided by the VDSL2 datapump. This mechanism provides full support for the VDSL2 bearer channel mapping and also provides a method for routing data to latency paths based on QoS parameters. The queue data can be routed to the DSP memory or any other memory but for normal operation will be routed directly to the encoder.

The encoder performs framing, CRC generation, scrambling, interleaving, bit extraction, constellation encoding, and scaling as defined in the VDSL2 specification. The encoder functions are divided between two hardware modules that share a common DMA, peripheral bus, and local memory: the SRS (Scrambler and Reed-Solomon) and the ICE (Interleaver and Constellation Encoder) module. The encoder is designed to be reasonably generic and programmable by the DSP. This approach provides flexibility for future specification changes and allows for easier reuse of the hardware for training and other non-Showtime functions. The Scrambler/Reed-Solomon (SRS) block receives data either directly from the queues or from DMA and perform framing, CRC generation, scrambling, and Reed-Solomon encoding and then deposits the data in the Interleave memory. The Interleaver/ Constellation Encoder (ICE) block fetches data from the interleave memory and directly from the SRS to perform bit extraction, constellation encoding, rotation, and tone scaling. The complex addressing used for performing the GCI interleave function is normally done by the SRS block as it fills the interleave memory. However, for maximum flexibility the ICE block contains a fully programmable memory interface as well. The encoder fully supports the GCI interleaver function including the ability to perform dynamic interleaver parameter changes for all interleaver profiles up to 128 KB.

After constellation encoding the ICE block performs tone re-ordering and deposits the constellation points into the output FIFO (IFFT input ram). At the correct time the ICE transfers the tones to the FFT/IFFT engine. The per tone gain adjustment is applied as the tones are transfered The FFT/IFFT block is shared between transmit and receive paths but it can simultaneously perform 8192 point FFT and IFFT transforms at up to 8Khz symbol rates. The output of the IFFT is transferred to the TX FIFO. and cyclic extension is applied with full windowing support. The transmit time domain processor extracts the samples from the TX FIFO and performs time domain processing including image supression, POTs filtering, and echo cancellation (long reach VDSL).

The AFE interface block is designed to interface the chip to a VDSL2 AFE. The block is designed to be flexible enough to support existing and future AFEs. Up to 16 bits of data can be driven onto the TX leads and an additional 16 bits received on the RX leads on each 70.656 Mhz sample clock. This interface is flexible enough to support many devices.

2-4 Receive Path Operation

In the receive direction the AFE interface receives one 16-bit sample per 70.656 MHz clock from the AFE and transfers the data to the Receive Co-Processor (RCP). The RCP performs time domain filtering including sample rate reduction and echo cancellation if necessary. Then it calculates the TEQ filter and transfers the samples to the RX FIFO.
Like the TX FIFO, the RX FIFO read and writes pointers are controllable by the DSP for use in symbol alignment. The FIFO can also be programmed to discard the cyclic prefix. After symbol sync is achieved, the RX FIFO can generate symbol rate timing signal. This signal defines the symbol boundary and can be used to trigger the other hardware blocks.

When the FFT block is available for performing an FFT, a symbol of data is burst transferred into the block. Like the IFFT, the FFT block takes advantage of the idle butterfly hardware to perform scaling during input/output transfers. The FFT/IFFT engine provides two 4096 entry gain tables that are shared between the IFFT input and FFT output. This structure allows all tones to have a separate gain and allows the gain updates to be performed at any time to support bit swap operations. The FFT signals the FCP and/or DSP when the output is ready. The FCP performs the FEQ filtering (including filter training), slicing, Viterbi decoding, SNR calculations, and framing. To save processing time and hardware requirements the FCP only operates on the active bins for the RX direction. The FCP block performs reverse tone ordering as it reads the data out of the FFT Output buffer. To facilitate training symbol recovery, the FCP also has pseudo-random number generator and tone rotator.

The FCP contains a specialized complex data processor that is capable of performing all FEQ, SNR, and slicing operations. The processor contains it s own program space that is written by the DSP. When the FCP has re-assembled the bit stream, it writes the data into the de-interleave memory including erasure information for soft detected errors. The de-interleaver complexity occurs in the DRS module but the FCP also has the ability to perform complex transfers to memory and the DMA bus. The de-interleave memory is shared with the DSP in the same fashion as the interleave memory. Simultaneous accesses by the DSP and hardware will result in hardware wait states. The FCP signals the DRS and/or DSP when enough data is available for de-interleaving to begin.

De-interleaving, Reed-Solomon decoding, CRC check, and de-scrambling are performed by the DRS block. The de-interleave function is performed by the addressing logic as data is fetched for Reed-Solomon decoding. Unlike the Reed-Solomon encoder, the decoder needs to have access to a full code word of data in case it needs to make corrections. Therefore, the Reed-Solomon decoder has a local 255 byte buffer to hold the maximum sized Reed-Solomon code word and an additional 255 bits for erasure information. After any corrections are made the data is de-scrambled, CRC checks are performed at super-frame boundaries, VOC and other the fast bytes are extracted and DMA transferred to DSP memory for DSP access. The de-framing logic has the same degree of programmability as the framer in the SRS block. The final output of the block is either point-to-point or DMA transferred to DSP memory or directly to the MII/SMII/GMII interface FIFO.

2-5 Analog Front End (AFE) Interface

AFE Interface is controlled by a 24-bit control register which can be configured and modified via API command. The controls provide the flexibility to support many AFE devices.

Bit	Symbol	Description
23-20	AFE_WCNT_MASK	This is a mask for the word counter. It generates a circular word count for the number of serial words (or bits in serial mode) between sync pulses.
19-16	AFE_WCNT_AOFF	This offsets the ADC word count prior to masking by the word count mask above. It essentially rotates the count to the proper alignment to match the
15-12	AFE_WCNT_DOFF	This offsets the DAC word count prior to masking by the word count mask above. It essentially rotates the count to the proper alignment to match the
11	BIG_ENDIAN	Enables big endian transfers (MSBs first) on Word wide interfaces.
10-8	AFE_WSIZE	Defines the number of bits transferred on the interface in parallel. For each transfer clock edge.
7	DDR	Enables double data rate mode. Data is supplied on both edges of the clock
6	AFE_SYNC_POL	Defines the polarity of the sync pulse. The sync pulse is always sampled on the negative edge of the clock. 0 = positive pulse 1 = negative pulse
5	AFE_ADC_POL	Defines the edge on which the ADC input is sampled. 0 = positive edge 1 = negative edge
4	AFE_DAC_POL	Defines the edge on which the DAC sample is clocked 0 = positive edge 1 = negative edge
3	DAC_CLK_OUT	Enables the DAC interface clock to be driven onto bit 5 of the DAC data bus. The supplied clock is a delayed version of the AFE input clock.
2	DAC_SYNC_OUT	Enables the DAC sync signal to be driven onto bit 6 of the DAC data bus. Depending on the WCNT settings, the DAC sync may or may not match the sync provided by the AFE.
1	Reserved	Reserved

0	AFE_CLK0	Enables AFE#0 clock 0 = Disabled 1 = Enabled

Table 1 AFEFR as Shown in the Following Table

The word count mask specifies the 2^n count value of a circular word counter. This is generally set to the number of data samples between sync pulses.

For the 16-bit parallel interface, setting the word count mask to anything other than zero creates a multi-channel mode, e.g., word count mask = 1 interleaves samples of channel 0 and channel 1 with the sync0 pulse determining the channel assignment. Setting word count mask = 3 specifies a 4-channel mode. With word count mask = 0 the sync pulse is ignored and the interface is clamped at channel 0. The nibble and byte-serial modes transmit least significant portion of the word first in time. The bit and dibit-serial modes transmit most significant portion of the word first in time. This matches the individual specifications of the AFE devices supported.

Individual word count offsets for both the ADC and DAC allow the sync pulse position to have an arbitrary alignment relative to the channel data. They essentially rotate the word count to match the channel number or word position of the data being transferred by the interface.

The AFE block is equipped with a low-power gated clock mode. Setting the soft reset bit of the CTL register will gate off the clock for the module and reset all logic. This capability is useful for reducing power consumption when MT5302 is not operating.

The AFE interface usessingle clocks: CLK. These clocks are asynchronous to the system clock; however, the minimum period (14.15 ns) must beat least twice the system clock period.Two snapshot registers capture different portions of the ADC input on each of the selected external clock edges. This guarantees proper operation for clock frequencies up to 70 MHz. Each external clock is double delayed and differentiated for both positive and negative edge. Double delayed input data is captured on the selected pos/neg edge. Output data is supplied on the selected pos/neg edge. Sync pulses are always captured on the negative edge since all supported converters provide sync pulses synchronous with the positive edge of their respective clocks.

2-5-1 Transmit Path

The AFE transmit path consists of 5 blocks: a digital interpolation filter, a current steering DAC, a 4th order post low pass filter (LPF), a high pass filter (HPF), and a high performance line driver.

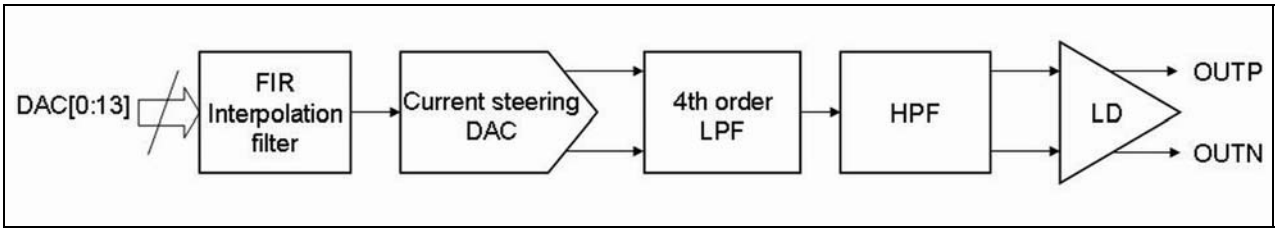


Figure 5 Block Diagram of Transmit Path

2-5-1-1 Interpolation Filter

The interpolation filter receives a 14-bit wide data stream in two's complement at 35.328MSPS/70.656MSPS, and is programmable for application of 8MHz/12MHz/17MHz/30MHz signal bandwidth. It relaxes the following LPF requirement by suppressing the image signal and increasing the LPF's transition band simultaneously. To attenuate images, the filter has an up-sampled output of 141.312MSPS/282.624MSPS which feeds the current steering DAC.

2-5-1-2 Digital to Analog Converter (DAC)/TX Post Low Pass Filter/TX High Pass Filter

The DAC is a 14-bit resolution current steering DAC which operates at 141.312MHz/ 282.624MHz with 12-bit accuracy. The 4th order continuous-time post low pass filter following the DAC guarantees the required suppression of all out-of-band images and noise. The HPF reduces the side-lobe signal that might interfere in POTS. The typical corner frequencies of LPF and HPF are kept within a ±7% range by means of an automatic RC-time constant adjustment during power-up. The output of HPF can serve as the input to an external line driver or to the internal line driver.

2-5-1-3 Power Back Off

To allow a power back off (PBO) for line power, a programmable attenuation is realized from 0dB down to -20dB in 0.5dB steps. To keep the DAC operating with the optimal S/N conditions, this attenuation is mainly realized in the post-filter block. If again finer attenuation steps are necessary, digital attenuation using the DSP can be used in conjunction with the analog attenuation.

2-5-1-4 Line Driver

The line driver takes its input signal from the high pass filter. The fully integrated line driver reaches an extremely high linearity by means of a sophisticated compensation technique, whereby additional outputs and external circuitry are needed. To minimize the power consumption, 40% of the output impedance is

synthesized. This configuration allows a highly efficient line driver design with a single 5V supply only. The necessary amplifier feedback path is also used as the input of the receive path. The integrated line driver provides sufficient power settings required by the VDSL2 standards for PSD masks. A properly selected line driver can be connected externally if larger power is needed.

2-5-2 Receive Path

The receive path consists of a two stage variable gain amplifiers (VGA), a continuous time sigma-delta ADC, and a digital decimation filter.

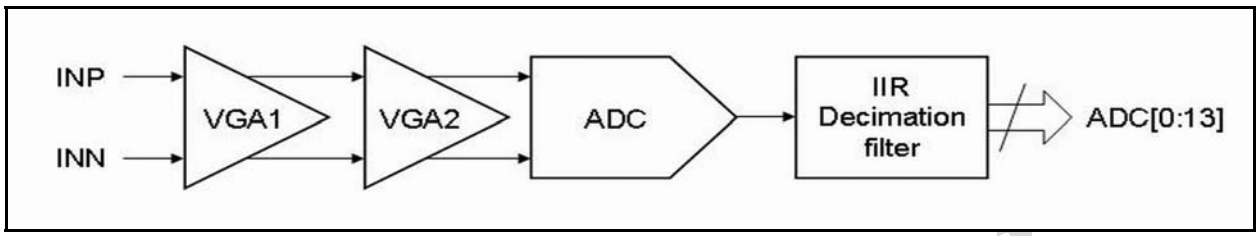


Figure 6 Block Diagram of Receive Path

2-5-2-1 Variable Gain Amplifier

The VGA is used to adapt the dynamic range of the received signal to best fit the S/N and dynamic range requirements of the ADC. A first order high pass filter located in the VGA attenuates the remaining signal of the first down-stream band D1. Hence, the hybrid performance can be optimized to reduce the remaining echo resulting in an improved overall rejection.

The VGA has a minimum gain setting of -6dB and a maximum of 35dB. The gain step is 1 dB between 12 and 35 dB gain. Below 12dB gain, 2dB steps are possible and the first VGA is bypassed.

2-5-2-2 Analog to Digital Converter/Decimation Filter

The 12-bit accurate Analog to Digital Converter is implemented as a continuous time Sigma-Delta modulator with subsequent decimation stages. The 30MHz analog bandwidth modulator uses a sampling frequency of 280MHz. The 6 bit output of the modulator passes through a SINC and an IIR-filter. This filter delivers a 14-bit wide 35.328MSPS/70.656MSPS output stream in two's complement. This filter is programmable for applications of 8MHz/12MHz/17MHz/30MHz signal bandwidth.

2-5-3 Common Blocks

2-5-3-1 Crystal Oscillator

The reference-oscillator requires a 35.328MHz crystal to be connected between pins XTAL1 and XTAL2. To compensate for the tolerances of the crystal, the oscillator allows a frequency adjustment by switching internal capacitors within a range from 6pf to 38pf in about 5fF-steps at both XTAL1/2 pins. The resulting

frequency range of the adjustment ultimately depends on the crystal's equivalent circuit. Typical values are ±200ppm frequency range.

This adjustment can also be used to synchronize the modem timing with the system wide timing.

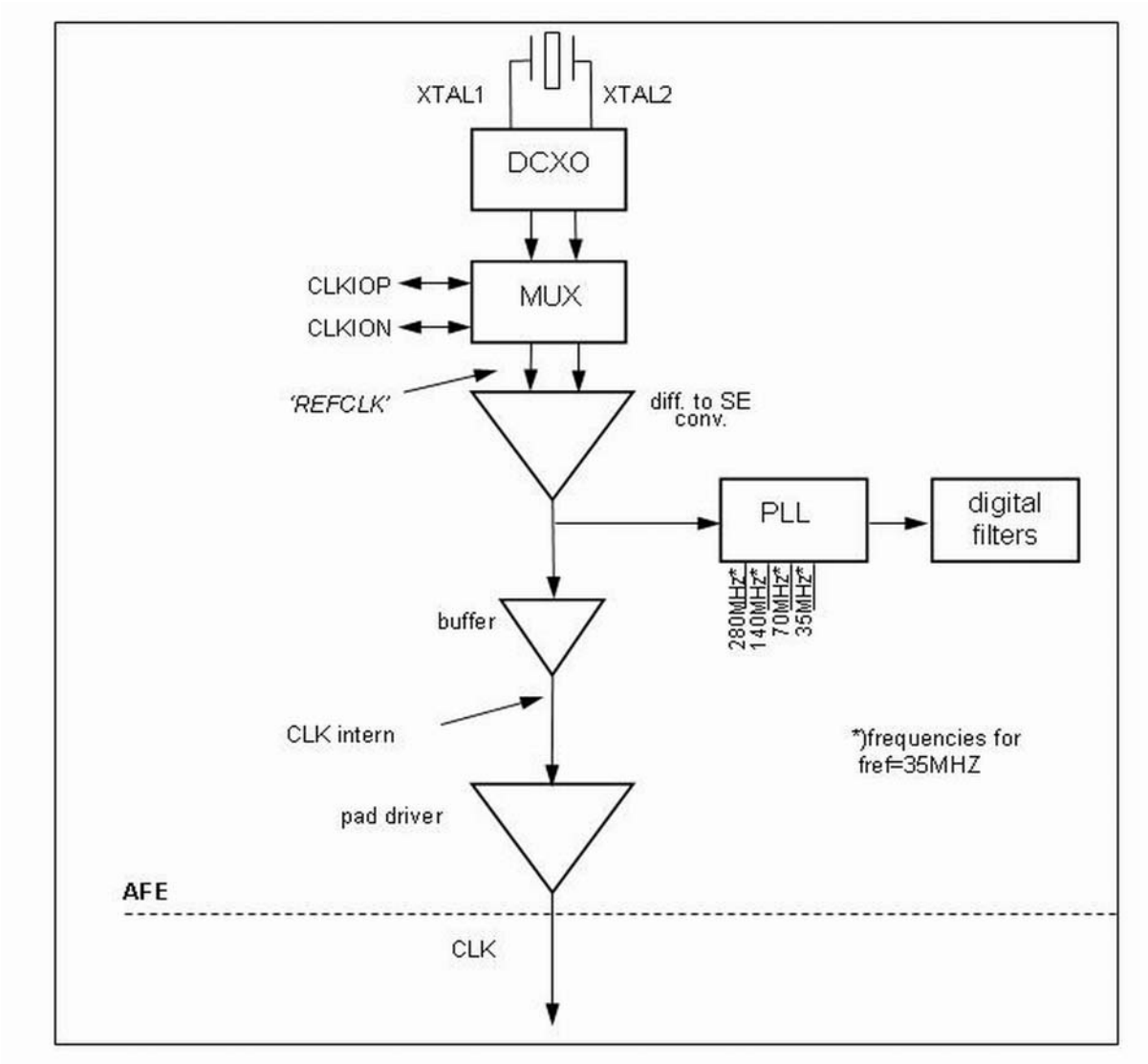


Figure 7 Oscillator/PLL Block Diagram

2-5-3-2 TX and RX Data I/O

The TX and RX data between the DSP and the AFE is exchanged at a sample rate of 35.328MSPS or 70.656MSPS. Synchronization is guaranteed by the system wide 35.328MHz clock (pin CLK).

2-5-3-3 Serial Control Interface

The serial control interface consists of the three connections CLK, DIN and DOUT. The CLK is the system

wide 35.328MHz reference clock provided through the AFE. The DIN line carries information from the DSP to the AFE, whereas DOUT transfers information from the AFE to the DSP.

The protocol comprises of
1 startbit`0`,

a data word of
12-bit data d11-d0 (in case of a 'Read' command the data won't be evaluated),

and register/ command bits with
3-bit register address a2-a0 and
1-bit R/W, Read=0, Write=1.

The protocol is shown in Figure 6: Serial Control Interface Protocol.

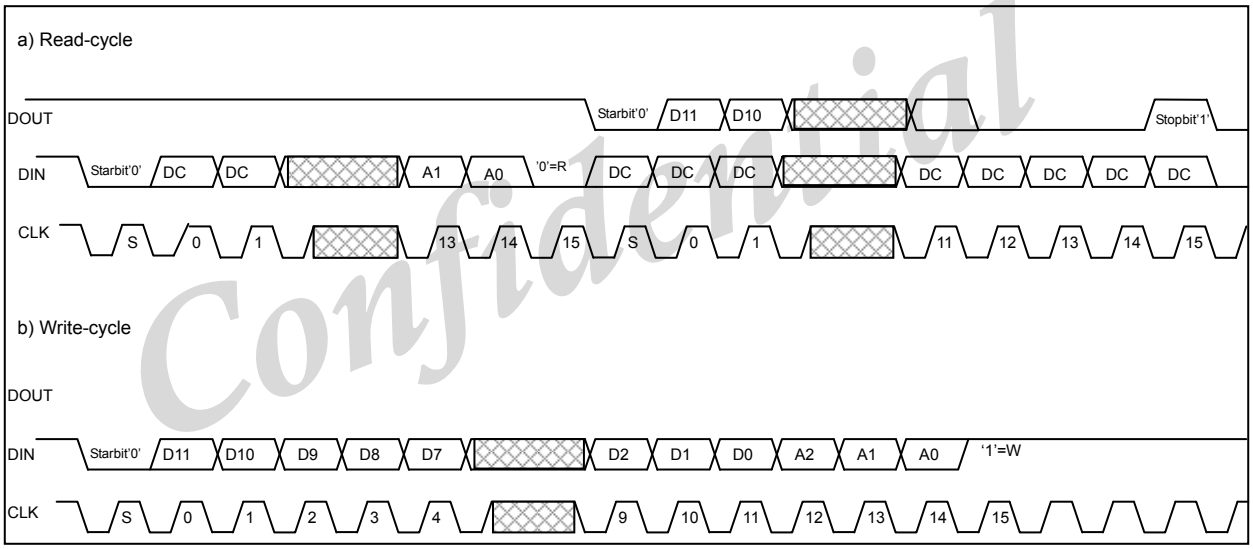


Figure 8 Serial Control Interface Protocol

When the DSP needs to read back the data from the AFE, a "Read" command is initiated. One clock cycle later, the AFE will transmit on a dedicated pin DOUT, starting with a startbit '0', the 12-bit data word d11-d0 of the specified address a2-a0 followed by 3 '0' and a stopbit '1'.

The serial interface allows the programming of the functions of the constitutive blocks, e.g. power down and gain settings.

2-5-4 Programming

2-5-4-1 Chip Register Addresses

The default values of all register bits at power on is “0”. When register setting instructions given in this document make no mention of certain bits, they must be left or set to “0”.

Register#	Block (Function)
000 (0)	VGA
001 (1)	ADC/VGA
010 (2)	DCXO frequency adjustment
011 (3)	DAC/Post filter/Line driver
100 (4)	Bias/References
101 (5)	PLL/DCXO2
110 (6)	Reserved*)
111 (7)	Miscellaneous

***)Note:** Register 6 contains bit setting for control during test. They are for internal use only and must be set to “0”.

2-5-4-2 Address 0 (VGA/Filter)

Function	11	3
TX High Pass Filter Corner Frequency		
32KHz	0	0
138KHz	0	1
276KHz	1	0
3MHz	1	1

Function	10	9	8	7
VGA Gain 1				
-6dB	0	0	0	0
Not Allowed	0	0	0	1
0dB	0	0	1	0
Not Allowed	0	0	1	1
Not Allowed	0	1	0	0
Not Allowed	0	1	0	1
6dB	0	1	1	0
Not Allowed	0	1	1	1
12dB	1	0	0	0
13dB	1	0	0	1
18dB	1	0	1	0
19dB	1	0	1	1
Not Allowed	1	1	0	0
Not Allowed	1	1	0	1
24dB	1	1	1	0
25dB	1	1	1	1

Function	6	5
RX High Pass Filter Corner Frequency		
32KHz	0	0
138KHz	0	1
276KHz	1	0
3MHz	1	1

Function	4
RX Low Pass Filter	
Full Bandwidth (30MHz)	0
Activate 12MHz Low Pass Filter	1

Function	2	1	0
For Internal Use Only			
Must be '111'*)	1	1	1

2-5-4-3 Address 1 (ADC/VGA2)

Function	11
ADC/VGA Power Down	
ADC/VGA Running	0
ADC/VGA Power Down	1

Function	10	9	8
VGA Gain 2			
0dB	0	0	0
2dB	0	0	1
4dB	0	1	0
4dB	0	1	1
6B	1	0	0
8dB	1	0	1
10dB	1	1	0
10dB	1	1	1

***)Note:** Underlined settings are recommended settings. If no indication is given the setting is according to application requirements.

2-5-4-4 Address 2 (DCXO Frequency Adjustment)

Function	11	10	9	…	2	1	0
Crystal Oacillator Frequency Adjustment							
0fF	0	0	0	…	0	0	0
5fF	0	0	0	…	0	0	1
10fF	0	0	0	…	0	1	0
…							
…							
…							
…							
20.470pF	1	1	1		1	1	0
20.475pF	1	1	1		1	1	1

2-5-4-5 Address 3 (DAC/Post Filter/Line Driver)

Function	11
DAC/Post Filter Power Down	
DAC/Post Filter Running	0
DAC/Post Filter Power Down	1

Function	10	9
Power Back Off (PBO), Coarse Steps		
0dB	0	0
-4dB	0	1
-8dB	1	0
-12dB	1	1

Function	8	7	6
Power Back Off(PBO), Fine Steps			
0dB	0	0	0
-0.5dB	0	0	1
-1dB	0	1	0
-1.5dB	0	1	1
-2dB	1	0	0
-2.5dB	1	0	1
-3dB	1	1	0
-3.5dB	1	1	1

Function	5
Line Driver (LD) Power Down	
LD Power Down	0
LD Running	1

Function	4	3
Output Impedance during Power Down		
Infinite	0	0
128 Ohm	0	1
128 Ohm	1	0
64 Ohm	1	1

Function	2
Failure Protection	
Over Temperature and Over Current Protection Active	0
Over Temperature and Over Current Protection Disable	1

Function	1	0
Line Driver Bias Adjustment		
Standard Current	0	0
Standard Current x 0.5	0	1
Output Stage Current x 0.66	1	0
Standard Current x 0.66 / Output Stage Current x 0.5	1	1

2-5-4-6 Address 4 (Bias/Reference)

Function	11	10	9	8
TX Voltage Adjustment				
Default	0	0	0	0
Setting ΔV= - 0.9%	0	0	0	1
Setting ΔV= - 1.8%	0	0	1	0
Setting ΔV= - 2.7%	0	0	1	1
Setting ΔV= - 3.6%	0	1	0	0
Setting ΔV= - 4.5%	0	1	0	1
Setting ΔV= - 5.4%	0	1	1	0
Setting ΔV= - 6.3%	0	1	1	1
Setting ΔV=+7.2%	1	0	0	0
Setting ΔV=+6.3%	1	0	0	1
Setting ΔV=+5.4%	1	0	1	0
Setting ΔV=+4.5%	1	0	1	1
Setting ΔV=+3.6%	1	1	0	0
Setting ΔV=+2.7%	1	1	0	1
Setting ΔV=+1.8%	1	1	1	0
Setting ΔV=+0.9%	1	1	1	1

Function	7	6
Bias Current Adjustment		
Default	0	0
+12.5%	0	1
-25%	1	0
-12.5%	1	1

Function	5	4	3
Shutdown Temperature			
181˚C	0	0	1
175˚C	1	0	1
169˚C	0	1	1
163˚C	1	1	1
147˚C	0	0	0
139˚C	1	0	0
125˚C	0	1	0
113˚C	1	1	0

Function	2
Reference Power Down	
References Running	0
References Power Down	1

Function	1	0
For Internal Use Only		
Must be '00'	0	0

2-5-4-7 Address 5 (PLL/DCXO 2)

Function	11	10
Crystal Drive Level (Depending on Crystal Type)		
Maximum	0	0
High Medium	0	1
Low Medium	1	0
Minimum	1	1

Function	9
Power Down	
PLL Running	0
PLL Power Down	1

Function	8
PLL Mode	
Automatic Startup Procedure Enabled	0
Manual Startup	1

Function	7	6
Charge Pump Current		
20uA	0	0
30uA	0	1
50uA	1	0
140uA	1	1

Function	5
Reference Frequency Selection	
Reference is 30.240MHz	0
Reference is 35.328MHz	1

Function	4
Freeze Tuning	
Tuning Running	0
Tuning Frozen	1

Function	3
External 280MHz CLK	
Disable	0
Enable	1

Function	2
Bias Current for VCO	
5.2mA	0
8.6mA	1

Function	1	0
For Internal Use Only		
Must be '00'	0	0

2-5-4-8 Address 6 (Digital Circuit/POFI Power Saving)

Function	11	10	9	8	7	6
For Internal Use Only						
Must be '000000'	0	0	0	0	0	0

Function	5	4	3	2	1	0
For Internal Use Only						
Must be '000000'	0	0	0	0	0	0

2-5-4-9 Address 7 (Others)

Function	11
Line Driver (LD) Power Gain*)	
High Gain	0
Low Gain	1

Function	10
External Line Driver (LD) Power Down	
External LD Running	0
External LD Power Down	1

Function	9
Operation Mode Selection	
8a/8b/12a/17a Profile	0
30a Profile	1

Function	8	7	6	5	4	3	2	1	0
For Internal Use Only									
Must be '000000'	0	0	0	0	0	0	0	0	0

***)Note:** Bit 11 controls the maximum power that line driver can provide. If the turns ratio of the transformer is 1:7, high gain provides 20.5 dbm maximum power, low gain provides 14.5 dbm. If the ratio is 1:4, high gain provides 14.5 dbm maximum power.

2-6 Ethernet Interfaces

2-6-1 SMII Operation

The Serial Media Independent Interface (SMII) provides all functions equivalent to the MII interface without the overhead of the external wiring of the more parallel form of the interface. This section describes all the differences between SMII and MII interfaces for the signals, functionalities, and other specific information related to the SMII operation.

The data received from the Ethernet MAC on the TX interface is bit serial, eight bits of data and two status bits: TX_EN and TX_ER. Using TX_SYNC for frame alignment the SMII module converts the serial data (least significant bit first in time) to 10-bit parallel data. The TX_EN bit determines if a valid byte is currently available. The byte is valid if TX_EN is asserted even when TX_ER is also asserted. The framing logic passes valid bytes to the FIFO interface. When two SMII channels are used, the SYNC and CLK signals are used for both channels.

If TX_ER is asserted while TX_EN is also active the MAC is indicating that there is an error in the current Ethernet packet. The SMII module stores this error condition in the high bit of the next tag register. It can also generate an interrupt for this condition. The error is propagated into the current frame being sent. The second CRC byte (FCS in the encoder) is complemented to indicate an error frame. When the TX_EN bit is not active both TXD and TX_ER are ignored.

The valid byte stream process remains similar to the MII interface.

The RX path is largely the inverse of the TX. As with the MII module, the SMII module indicates the PHY has detected a data error in the idle status following an active frame. Status indicated by the eight data bits when the link is idle (RX_DV = 0):

RXD0 - RX_ER from previous frame

RXD1 - always 1 = 100 Mbps

RXD2 - full-duplex operation programmable under software control

RXD3 - link active state of the interface (channel specific)

RXD4 - always 0 = jabber OK

RXD5 - always 1 = upper nibble valid

RXD6 - always 0 = false carrier not detected

RXD7 - always 1

The 125 MHz TX_CLK (for SMII) is supplied externally to prevent unusual amounts of clock skew. MT5302 uses a PLL to lock to the phase of this clock when generating the RX signals. The TX_CLK will be looped back to the interface as RX_CLK but with timing that matches the other RX signals. Optionally, MT5302 can generate the 125 Mhz RX_CLK using the PLL.

Received data and control information are signaled in ten bit segments. In 100 MBit mode, each segment represents a new byte of data. As defined in the 802.3 EFM standard, there is no 10 Mbit support.

2-6-2 Other Ethernet Related Operations

MT5302 also has support for two SMII (4 leads) or SSMII (6 leads) interfaces. The TC sub-layer uses a 65th sync byte for every 64 bytes transmitted to encapsulate the framed data but also supports HDLC encapsulation. The TC sub-layer also includes a G(x) = 1 + x^39 + x^58 scrambler/descrambler combination. Protocol is incorporated for mapping the following data types: idle, in-frame, idle->in-frame, in-frame->idle, in-frame->idle->in-frame. For packets containing data a 32-bit CRC is appended. After coding the byte stream is written to the input FIFO. This FIFO is located outside of the MII module.

The RX path is largely the inverse of the TX. Data is fetched from the output FIFO and passed through a decoder. Sync byte detection is performed in the receive path according to a well-defined state machine. The transmit path uses a 64-byte pipeline.

The serial control portion of the MII module implements the management data interface defined in the IEEE Std 802.3 specification. This interface supports dual standard clause 22 and clause 45 operations. Clause 22 is considered to be obsolete, but is included for backwards compatibility with older equipment. This standard defines a Management Data Input/Output (MDIO) interface between Station Management (STA) devices and the sub-layers that form the Physical Layer (PHY). The sub-layers are composed of individually manageable entities known as MDIO Manageable Devices (MMDs). The management data interface uses a data frame to transmit read or write commands to the PHY and to receive response data for reads. Control information is sent by STA in the initial portion of a management frame that determines the data transaction type to execute. The PHY can only return status or accept command as requested by the STA. Protocols must be defined to accomplish the reverse. Three fields control the type of transaction:

OP - the op-code (refer to clause 22/45 for definition)

PRTAD (PHYAD) - the port address (or clause 22 physical address)

DEVAD (REGAD) - the device address (or clause 22 register address)

The MII block is equipped with a low-power gated clock mode. Setting the soft reset bit of the CSR will gate off the clock for the module and reset all logic.

The MDC clock is asynchronous to the system clock; however, its minimum period (400 ns) is much longer

than the system clock (7ns). Therefore, the clock is sampled by the system clock for the purpose of capturing data on the MDIO lead and no MDC clock domain is needed.

2-6-3 Quality of Service Feature

The following list defines the features of the QoS implementation in MT5302. These features allow the device to route packets between the two VDSL2 latency paths based on priority and to perform scheduling within each path. The QoS function can be applied to any Ethernet interface.

1. For TX, sort Ethernet packets into two latency paths based on the defined packet sorting mode. The packets within each latency path are also be queued based on priority.
2. For RX, Ethernet packets from two latency paths are combined before transmitting on MII. Priority queueing is not required in the RX path.
3. A maximum of four priority queues are supported for one Ethernet channel. Multiple Ethernet bearer channels are not supported when QoS is enabled
4. The QoS engine supports four mutually exclusive packet sorting modes:
    a. No sorting. All packets go to the default latency path.(disable QoS function)
    b. Sorting based on ethertype field of Ethernet headers. Up to 8 ethertype values can be specified. Each can be routed to either latency path and priority queue.
    c. Sorting based on VLAN ID range. Up to 8 VID/Netmask pairs can be defined. VIDs matching the range specified by each VID/Netmask pair can be routed to either latency path. Packets within a latency path can also be placed in a high or low priority queue can based on the VLAN priority field.
    d. Sorting based on VLAN priority field. Each of the 8 possible VLAN priority values can be routed to either latency path. Packets within a latency path can also be placed in a high or low priority queue based on the VLAN priority field.
5. A configurable default latency path and queue is provided . Any packet that does not match one of the sorting filters will be sent to this path/queue. Also, in mode c., VLAN packets that do not match one of the VLAN ID filters can be dropped (configuration option) instead of being sent to the default latency path.
6. The Ethertype used for VLAN detection is configurable to support single and multi-tag (Q-in-Q) traffic.
7. Packets are routed based on the outer most VLAN tag. When multiple layers of VLAN are employed MT5302 will sort based on the outer layer and ignore the any inner layers.
8. Pause/Resume frame backpressure is normally used to avoid FIFO overflows. However, each queue can also be configured to drop packets before an overflow occurs. This mechanism allows low priority packets to be dropped without affecting high priority flows. The QoS logic maintains counters keep track of the number of dropped packets.

2-7 Serial Port Interface

The Serial Port Interface (SPI) provides multiple ports that can be used for various purposes. One port will usually be used to control the external AFE while another may be used for EEPROM booting or some other purpose. The ports are all full-duplex serial ports with a lot of flexibility in their programming for communicating with a variety of serial devices.

All Serial Ports include comprise independent transmitter and receiver sections and a common serial clock generator.

2-7-1 Serial Port Rates

The Serial Port interface maximum communication rate is 1/4 of the master clock. Since MT5302 can operate up to 150 MHz, the maximum serial rate is 37.5Mbit per second. All Serial Port Interfaces need four system clocks to operate on a single bit of data. When the serial port is the clock master, The minimum data rate is equal to the DSP clock frequency divided by 4096.Therefore, 36.6Kbit per second is the minimum speed for clock master mode with a 150 MHz DSP clock

2-7-2 Serial Port Operation

Words transferred by the SCI are characterized by word length, shift direction, and word alignment. This section describes these characteristics and the programming associated with them.

2-7-3 Word Length

The Serial Port provides full control of the number of bits per word or the word length. The SCI transmit and receive data registers are 24-bits long, so 32-bits words cannot be transmitted or received. For 32-bit words, the first 24 bits contain valid data and the last bits are not defined.

2-7-4 Shift Direction

The Serial Port presents two options for shift direction: most significant bit (MSB) first or least significant bit (LSB) first. To select shift direction, set bit 6 in Control Register B, SHFD. If SHFD is set, the data is shifted into the receive shift register from the SRD lead and out of the transmit shift register to the STD lead with the LSB first. If SHFD is clear, the data is shifted into the receive shift register from the SRD lead and out of the transmit shift register to the STD lead with the MSB first.

2-7-5 Synchronization Signals

Because the Serial Port is a synchronous interface, it requires clock and frame sync signals to define when the data changes and when a new frame begins. In certain modes, the Serial Port also has the option of two flag signals to use for device selection.

2-7-6 Synchronous versus Asynchronous

The Serial Port includes both synchronous and asynchronous modes. In synchronous mode, the transmitters and receiver use the same clock and frame sync; in asynchronous mode, the transmitters and receiver use different clocks and frame syncs. The Serial Port data transfers are synchronized to a clock in both modes. The choice of synchronous versus asynchronous mode is determined by API command. Setting SYN puts the Serial Port is in synchronous mode; clearing SYN puts it in asynchronous mode.

In synchronous mode: SCK is an input or an output that both the transmitter and receiver use as the clock signal. SC2 is an input or an output that both the transmitter and receiver use as the frame sync signal. SC0 and SC1 can be used as flag signals.

2-7-7 In Asynchronous Mode

SCK is an input or an output that the transmitter uses as the clock signal.

SC2 is an input or an output that the transmitter uses as the frame sync signal.

SC0 is an input or an output that the receiver uses as the clock signal.

SC1 is an input or an output that the receiver uses as the frame sync signal.

The direction of the SC0, SC1, SC2, and SCK leads is determined by the SCD0, SCD1, SCD2, and SCKD bits, respectively, CRB [3:0]. If one of these bits is clear, the corresponding lead is an input. If one of these bits is set, the corresponding lead is an output.

2-7-8 Serial Clock

SCK's direction can be controlled via API command.

2-7-9 Frame Sync

The frame sync signal indicates when a new frame begins. In synchronous mode, the SC2 lead is the frame sync for the receiver and transmitter. In asynchronous mode, SC2 is the frame sync signal for the receiver and SC0 is the frame sync signal for transmitter 0.

Frame sync is generated only when data is ready to be transmitted, i.e., data is written to a transmit data register. This mode requires that the transmit frame sync be internal (output) and the receive frame sync be external (input) for proper operation. Transmit under-runs are impossible in on-demand mode because there are no transmit time slots, thus they are disabled.

2-7-10 Flags

When the Serial Port is in synchronous mode, the SC0 and SC1 leads are available for use as flags.

2-7-11 SPI Protocol: Clock Stop Mode

A system conforming to this protocol has a master-slave configuration. SPI protocol is a 4-wire interface composed of serial data in (master in slave out), serial data out (master out slave in), shift clock (SCK), and an active (low) slave enable signal. Communication between the master and the slave is determined by the presence or absence of the master clock. Data transfer is initiated by the detection of the master clock and is terminated on absence of the master clock. The slave has to be enabled during this period of transfer. When the SPI is the master, the slave enable is derived from the master transmit frame sync pulse, SC2.

The clock stop mode of the Serial Port provides compatibility with the SPI protocol. The SPI supports two SPI transfer formats specified by the clock stop mode field (CKST) in Control Register B. The clock stop mode in conjunction with the CKP bit allows serial clocks to be stopped between transfers using one of four possible timing variations.

2-7-12 SPI Protocol: Start Bit Mode

Some devices require a start bit to indicate the arrival of a data frame. When configured in this mode (SBIT = 1 in Control Register B) an active low start bit precedes the data followed by an active high stop bit. No frame sync is required since the receiving device frames the data. The word length control (WL [4:0]) is adjusted to specify the number of bits.

2-8 Host Port Interface

The host port interface (HPI) is an eight/sixteen bit parallel interface. It supports both master and slave mode operation and provides a DMA interface to the DSP memory for block transfers of up to 512 bytes. The HPI can interface with most of the Microprocessor and DSP available on the market with no external components

MT5302 employs a message interface API for command and response. The command and response message format uses HDLC-like framing, similar to the one used in G.997.1. Each command is followed by an acknowledge response typically within 1 ms. If a command is not acknowledged within 10 ms the command can be assumed to be not understood or some other error condition preventing the command can be assumed. Some commands will be acknowledged and then will be followed by a status frame sent from MT5302 to the host at a later time.

2-9 Boundary Scan (JTAG) Operation

When boundary scan testing is not being performed, the boundary scan register is transparent, allowing the input and output signals at the device leads to pass to and from the device's internal logic. During boundary scan testing, the boundary scan register disables the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. Data is read out from internal test registers LSB first.
The following boundary scan test instructions are supported

-SAMPLE/PRELOAD
-BYPASS
-IDCODE
-EXTEST

EXTEST Test Instruction: One of the required boundary scan tests is the external boundary test (EXTEST) instruction. When this instruction is shifted in, the device is forced into an off-line test mode. While in this test mode, the test bus can shift data through the boundary scan registers to control the external input and output leads. The MT3201 is NOT held in Reset.

SAMPLE/PRELOAD Test Instruction: When the SAMPLE/PRELOAD instruction is shifted in, the device remains fully operational. While in this test mode, input data, and data destined for device outputs, can be captured and shifted out for inspection. The data is captured in response to control signals sent to the TAP controller.

BYPASS Test Instruction: There is no explicit decode for bypass instruction. It is always selected by default. Thus any invalid instruction opcode will map to the bypass instruction. When the BYPASS instruction is shifted in, the device remains fully operational. While in this test mode, a scan operation will transfer serial data from the TDI input, through an internal scan cell, to the TDO lead. The purpose of this instruction is to abbreviate the scan path through the circuits that are not being tested to only a single clock delay.

IDCODE Instruction: When the IDCODE instruction is shifted in, the device remains fully operational. The purpose of this instruction is to output the device ID code register on the TDO lead.

3. Parameters

3-1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{STG}	Storage Temperature		-65		125	℃
T_J	Junction Temperature		-40		125	℃
V_{ESD}	Electrostatic Discharge Voltage Capability	HBM Mil.Std 883			2	kV

3-2 Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD-A1}	Analog supply voltage DAC,LD			5		V
V_{DD-A2}	Analog supply voltage VGA,ADC,PLL			2.5		V
V_{DD-D}	Digital core supply voltage			2.5		V
$V_{DD-I/O}$	I/O-supply voltage		1.1		3.5	V
T_{AMB}	Ambient temperature		-40	25	85	℃

3-3 Electrical Characteristics

Standard conditions unless otherwise stated: V_{DD-A1}=5V, V_{DD-A2}=2.5V, V_{DD-D2}=2.5, $V_{DD-I/O}$=1.2V, T_A=25℃, Crystal oscillator frequency 35.328MHZ

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD-A1}	Analog supply voltage DAC,LD		4.75	5	5.25	V
V_{DD-A2}	Analog supply voltage VGA,ADC,PLL		2.375	2.5	2.625	V
V_{DD-D}	Digital core supply voltage		2.375	2.5	2.625	V
$V_{DD-I/O}$	I/O-supply voltage		1.1		3.5*	V
$P_{SUPPLY1}$	Power consumption	@ 14.5dBm line power, 14.5db Crest factor		1440		mW
	Transmit path					
DR_{TX}	Input data rate	different data rate for different profile	35.328	-	70.656	MS/s
Res_{TX}	Resolution		-	14	-	bits
$V_{outmaxTX}$	Max. output voltage	@ 0dBfs, PBO=0dB, concept of synthesized impedance	8			V_{dpp}
$V_{outCMTX}$	Common mode output voltage			V_{DD-A1} /2		V
$I_{outmaxTX}$	Max. output current		800			mA
PSD_{IBLTX}	Output noise in-band	line referred, 138kHz..30MHz		-128		dBm/Hz
PSD_{OBLTX}	Output noise out-of-band	line referred, > 30MHz		-128		dBm/Hz
f_{lowTX}	Signal bandwidth lower corner frequency			32		kHz
f_{highTX}	Signal bandwidth upper corner frequency		30			MHz
PBR_{TX}	Passband ripple			0.5		dB
THD_{TX-3}	Total harmonic distortion	f_{in} =1,4,6,10MHz @ -3dBfs harmonics in band			-70	dBc
MBD_{TX}	Missing band depth			55		dB
GR_{PBO}	Power back off range		-14.5		0	dB
SS_{PBO}	PBO step size			0.5		dB
SS_{PBOADJ}	PBO accuracy		-0.5		0.5	dB

*The supply voltage for the digital I/O's can take any voltage between 1.1V and 3.5V.

Electrical Characteristics cont.

Symbol	Receive path	Condition	Min	Typ	Max	Unit
DR_{RX}	Output data rate	different data rate for different profile	35.328	-	70.656	MS/s
Res_{RX}	Resoltion		-	14	-	bits
$V_{inmaxRX}$	Max. input voltage	VGA gain = 0dB		3.6		V_{dpp}
GR_{VGA}	VGA gain range		-6		35	dB
SS_{VGA}	VGA step size	Gain -6dB through + 12dB Gain +12dB through + 35dB		2 1		dB dB
SS_{VGAADJ}	VGA accuracy		-0.5		0.5	dB
f_{lowRX}	Signal bandwidth lower corner frequency			32		kHz
f_{highRX}	Signal bandwidth upper corner frequency		30			MHz
PBR_{RX}	Passband ripple			1		dB
$SFDR_{RX}$	Spurious free dynamic range	fref =1 MHz		-70		dBc
THD_{RX-3}	Total harmonic distortion	f_{in} =1,4,6,10MHz @ -3dBfs			-70	dBc
PSD_{LRX}	Input noise	line referred		-135		dBm/Hz
MBD_{RX}	Missing band depth			55		dB
	Xtal oscillator					
f_{OSC}	Frequency	Xtal TBD		35.328		MHz
ΔC_{trim}	Capacitor trimming range		6		38	pF
	Digital I/O's					
V_{IH}	Input 'high'		$V_{DD-I/O}$ *0.8			V
V_{IL}	Input 'low'				$V_{DD-I/O}$ *0.2	V
V_{OH}	Output 'high'		$V_{DD-I/O}$ -0.1			V
V_{OL}	Output 'low'				0.1	V
C_{in}	Input capacitance				5	pF
C_{load}	Output capacitance	@ 60MHz signal			30	pF
	I/O timing					
T_{CLK30}	Clock period	CLK30=1/f_{OSC}		28.306		ns
DC	Clock duty cycle	CLK30		50		%
T_R/T_F	Rise/fall time	20% to 80%		2.5		ns
$T_{invalidADC}$	Invalid time ADC,DOUT	See Figure 9	0		6	ns
$T_{setupdac}$	Setup time DAC		12			ns
$T_{holddac}$	Hold time DAC		0			ns

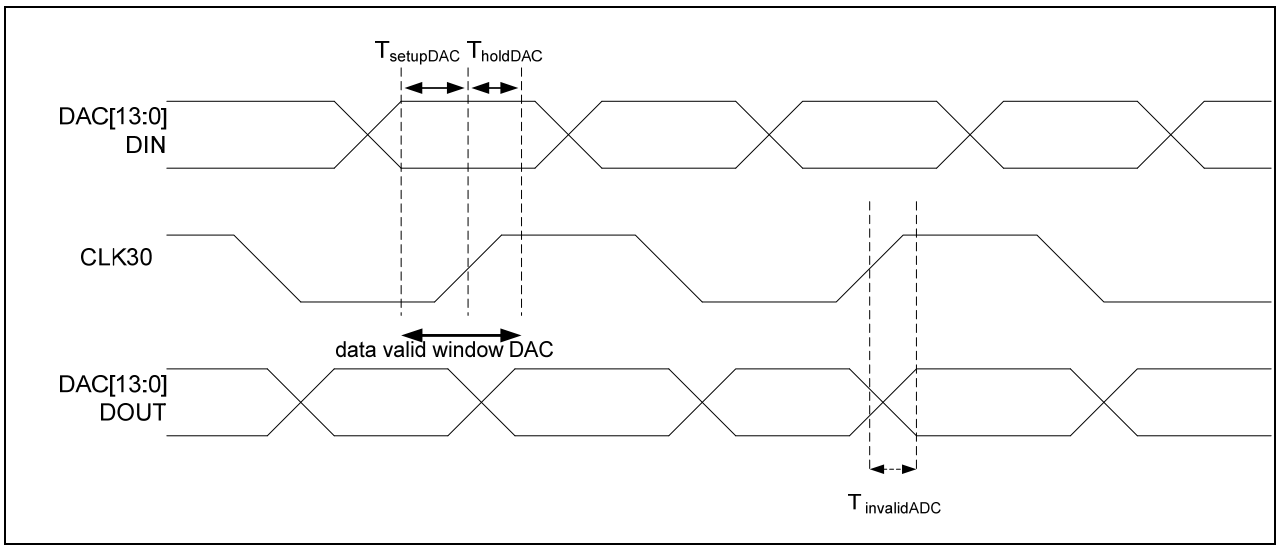


Figure 9 Data and control interface timing

4. Ball Description

Ball	Symbol	Pad Type	Description
V10	IRQA-0	I	External Interrupt A, Port 0
V11	IRQB-0	I	External Interrupt B, Port 0
V19	IRQA-1	I	External Interrupt A, Port 1
V20	IRQB-1	I	External Interrupt B, Port 1
U19	IRQC	I	Master External Interrupt C, controls both ports
U20	IRQD	I	Master External Interrupt D, controls both ports
T21	TMS	IPU	JTAG Port: Test Mode Select
U22	TRSTN	IPU	JTAG Port: Test Reset, Active Low
R19	TDO	O	JTAG Port: Test Date Out
R20	TDI	I	JTAG Port: Test Data In
T22	TCK	I	JTAG Port: Test CLK
R22	DEN	I	JTAG Port: Test Enable
M19	MDIO	I/O	MDIO Data
M20	MDC	I	MDIO CLK
AB15	SMII_RXCLK0	O	Port 0: SMII Receive CLK
AB13	SMII_RXDAT0-0	O	Port 0: SMII Receive Data 0
AB12	SMII_RXDAT1-0	O	Port 0: SMII Receive Data 1
AB14	SMII_RXSYNC0	O	Port 0: SMII Receive Sync Signal
AB6	SMII_TXCLK0	I	Port 0: SMII Transmit CLK
AB5	SMII_TXDAT0-0	I	Port 0: SMII Transmit Data 0
AB4	SMII_TXDAT1-0	I	Port 0: SMII Transmit Data 1
AB7	SMII_TXSYNC0	I	Port 0: SMII Transmit Sync Signal
AB16	SMII_RXCLK1	O	Port 1: SMII Receive CLK
AB18	SMII_RXDAT0-1	O	Port 1: SMII Receive Data 0
AB19	SMII_RXDAT1-1	O	Port 1: SMII Receive Data 1
AB17	SMII_RXSYNC1	O	Port 1: SMII Receive Sync Signal
AB8	SMII_TXCLK1	I	Port 1: SMII Transmit CLK
AB10	SMII_TXDAT0-1	I	Port 1: SMII Transmit Data 0
AB11	SMII_TXDAT1-1	I	Port 1: SMII Transmit Data 1
AB9	SMII_TXSYNC1	I	Port 1: SMII Transmit Sync Signal
A10	HYB_LDP_0	AI	Port 0: External Hybrid Positive Input
A9	HYB_LDN_0	AI	Port 0: External Hybrid Negative Input
A7	OUTP1_0	AO	Port 0: Line Driver Positive Output 1
A5	OUTP2_0	AO	Port 0: Line Driver Positive Output 2
A6	OUTN1_0	AO	Port 0: Line Driver Negative Output 1
A4	OUTN2_0	AO	Port 0: Line Driver Negative Output 2
A1	LDFBP_0	I	Port 0: Line Driver Positive Feedback Input
B1	LDFBN_0	I	Port 0: Line Driver Negative Feedback Input

Ball	Symbol	Pad Type	Description
A2	VGAINP_0	AI	Port 0: VGA Positve Input
B2	VGAINN_0	AI	Port 0: VGA Negative Input
C2	HPFOUTP_0	AO	Port 0: DAC/HPF Positive Ouput to be used with External Line Driver
D2	HPFOUTN_0	AO	Port 0: DAC/HPF Negative Ouput to be used with External Line Driver
A19	HYB_LDP_1	AI	Port 1:External Hybrid Positive Input
A20	HYB_LDN_1	AI	Port 1:External Hybrid Negative Input
A17	OUTP1_1	AO	Port 1: Line Driver Positive Output 1
A15	OUTP2_1	AO	Port 1: Line Driver Positive Output 2
A16	OUTN1_1	AO	Port 1: Line Driver Negative Output 1
A14	OUTN2_1	AO	Port 1: Line Driver Negative Output 2
A11	LDFBP_1	I	Port 1: Line Driver Positive Feedback Input
B11	LDFBN_1	I	Port 1: Line Driver Negative Feedback Input
A12	VGAINP_1	AI	Port 1: VGA Positve Input
B12	VGAINN_1	AI	Port 1: VGA Negative Input
C11	HPFOUTP_1	AO	Port 1: DAC/HPF Positive Ouput to be used with External Line Driver
D11	HPFOUTN_1	AO	Port 1: DAC/HPF Negative Ouput to be used with External Line Driver
H19	EXTERNALPOWERDOWN_1	I	Port 1: GPIO Control of External Line Driver
F11	EXTERNALPOWERDOWN_0	I	Port 0: GPIO Control of External Line Driver
K1	XTAL1_0	I	Port 0: AFE XTAL 1(35.328MHz)
L1	XTAL2_0	O	Port 0: AFE XTAL 2(35.328MHz)
L22	XTAL1_1	I	Port 1: AFE XTAL 1
K22	XTAL2_1	O	Port 1: AFE XTAL 2
W9	XTALI-0	I	Port 0: Master 25MHz CLK Input
W17	XTALI-1	I	Port 1: Master 25MHz CLK Input
L18	SRD0	I	Master SPI Serial Port Receive Data
L17	SFS0	I/O	Master SPI Serial Port Frame Sync
L21	SCK0	I/O	Master SPI Serial Port CLK
M21	STD0	O	Master SPI Serial Port Transmit Data
W18	SCKA-1	O	Port 1: AFE Serial Control CLK
W22	STDA-1	O	Port 1: AFE Serial Control Transmit Data
W21	SRDA-1	I	Port 1: AFE Serial Control Receive Data
W20	ACLK0_1	I	Port 1: AFE Interface CLK
P19	SCKB-1	I/O	Port 1: SPI Serial Port CLK
P20	STDB-1	O	Port 1: SPI Serial Port Transmit Data
T19	SRDB-1	I	Port 1: SPI Serial Port Receive Data
T20	SC2B-1	I/O	Port 1: SPI Serial Port Frame Sync
W10	SCKA-0	O	Port 0: AFE Serial Control CLK

Ball	Symbol	Pad Type	Description
Y10	STDA-0	O	Port 0: AFE Serial Control Transmit Data
Y11	SRDA-0	I	Port 0: AFE Serial Control Receive Data
W11	ACLK0_0	I	Port 0: AFE Interface CLK
L6	SCKB-0	I/O	Port 0: SPI Serial Port CLK
M6	STDB-0	O	Port 0: SPI Serial Port Transmit Data
K5	SRDB-0	I	Port 0: SPI Serial Port Receive Data
J4	SC2B-0	I/O	Port 0: SPI Serial Port Frame Sync
AA5	RESETN0	I	Port 0: Port 0 System Reset Signal, active low
Y20	RESETN1	I	Port 1: Port 1 System Reset Signal, active low
Y13	HPRDY	O	Host Port Ready Signal
R1	EXWEN	I	External Memory Interface Write Enable Signal
Y12	HPCS0	I	Port 0: Host Port Chip Select
Y14	HPCS1	I	Port 1: Host Port Chip Select
V12	HPDS	I	Host Port Data Strobe
W12	HPRD	I	Host Port Read Signal
T2	EXOEN	I	External Memory Interface Output Enable
K6	TESTMODE-0	I	Port 0: Test Mode for SCAN Test on Port 0
N19	TESTMODE-1	I	Port 1: Test Mode for SCAN Test on Port 1
M17	NMI	I	Non-maskable Interrupt
AB2	EXATT1_A2	I/O	Port 1: External Memory Interface Att. Address 2
AB3	EXATT1_A3	I/O	Port 1: External Memory Interface Att. Address 3
W4	EXATT_A0	I/O	Port0/1 :External Memory Interface Att. Address 0
W5	EXATT_A1	I/O	Port0/1 :External Memory Interface Att. Address 1
Y4	EXATT0_A2	I/O	Port 0 : External Memory Interface Att. Address 2
Y5	EXATT0_A3	I/O	Port 0 : External Memory Interface Att. Address 3
W13	EXDAT0	I/O	External Memory Interface Data 0
W14	EXDAT1	I/O	External Memory Interface Data 1
Y15	EXDAT2	I/O	External Memory Interface Data 2
W6	EXDAT3	I/O	External Memory Interface Data 3
AA6	EXDAT4	I/O	External Memory Interface Data 4
Y6	EXDAT5	I/O	External Memory Interface Data 5
W15	EXDAT6	I/O	External Memory Interface Data 6
AA14	EXDAT7	I/O	External Memory Interface Data 7
AA15	EXDAT8	I/O	External Memory Interface Data 8;Host Port Data 0; GPIO
Y16	EXDAT9	I/O	External Memory Interface Data 9;Host Port Data 1; GPIO
AA7	EXDAT10	I/O	External Memory Interface Data 10;Host Port Data 2; GPIO
AA16	EXDAT11	I/O	External Memory Interface Data 11;Host Port Data 3; GPIO
Y7	EXDAT12	I/O	External Memory Interface Data 12;Host Port Data 4; GPIO
W7	EXDAT13	I/O	External Memory Interface Data 13;Host Port Data 5; GPIO

Ball	Symbol	Pad Type	Description
AA8	EXDAT14	I/O	External Memory Interface Data 14;Host Port Data 6; GPIO
Y17	EXDAT15	I/O	External Memory Interface Data 15;Host Port Data 7; GPIO
Y8	EXDAT16	I/O	External Memory Interface Data 16;Host Port Data 8; GPIO
W16	EXDAT17	I/O	External Memory Interface Data 17;Host Port Data 9; GPIO
W8	EXDAT18	I/O	External Memory Interface Data 18;Host Port Data 10; GPIO
AA17	EXDAT19	I/O	External Memory Interface Data 19;Host Port Data 11; GPIO
AA9	EXDAT20	I/O	External Memory Interface Data 20;Host Port Data 12; GPIO
AA18	EXDAT21	I/O	External Memory Interface Data 21;Host Port Data 13; GPIO
Y9	EXDAT22	I/O	External Memory Interface Data 22;Host Port Data 14; GPIO
Y18	EXDAT23	I/O	External Memory Interface Data 23;Host Port Data 15; GPIO
T3	EXADR0	I/O	External Memory Interface Address 0;Host Port Address 0; GPIO
T1	EXADR1	I/O	External Memory Interface Address 1;Host Port Address 1;GPIO
U3	EXADR2	I/O	External Memory Interface Address 2;Host Port Address 2;GPIO
U2	EXADR3	I/O	External Memory Interface Address 3; Host Port Address 3; GPIO
V1	EXADR4	I/O	External Memory Interface Address 4; Host Port Address 4; GPIO
U1	EXADR5	I/O	External Memory Interface Address 5; Host Port Address 5; GPIO
W1	EXADR6	I/O	External Memory Interface Address 6; Host Port Address 6; GPIO
Y1	EXADR7	I/O	External Memory Interface Address 7;Host Port Address 7; GPIO
V2	EXADR8	I/O	External Memory Interface Address 8;Host Port Address 8; GPIO
AA1	EXADR9	I/O	External Memory Interface Address 9;Host Port Address 9; GPIO
V3	EXADR10	I/O	External Memory Interface Address 10;Host Port Address 10; GPIO
V4	EXADR11	I/O	External Memory Interface Address 11;Host Port Address 11; GPIO
Y2	EXADR12	I/O	External Memory Interface Address 12;Host Port Address 12; GPIO
AB1	EXADR13	I/O	External Memory Interface Address 13;Host Port Address 13; GPIO
W2	EXADR14	I/O	External Memory Interface Address 14;Host Port Address 14; GPIO
AA2	EXADR15	I/O	External Memory Interface Address 15;Host Port Address 15; GPIO
W3	EXADR16	I/O	External Memory Interface Address 16;Host Port Address 16; GPIO
Y3	EXADR17	I/O	External Memory Interface Address 17;Host Port Address 17; GPIO
C10	AGND	P	Analog GND
C17		P	
C18		P	
C19		P	
C8		P	
C9		P	
D10		P	
D18		P	
D19		P	
D9		P	
E18		P	
F4		P	

Ball	Symbol	Pad Type	Description
G18	AGND	P	Analog GND
G4		P	
H12		P	
H4		P	
H9		P	
J10		P	
J11		P	
J12		P	
J13		P	
J14		P	
J9		P	
K14		P	
K9		P	
Y19	VSSPLL2_1	P	PLL GND
AA11	VSSPLL2_0	P	
AA13	VSSPLL1_1	P	
AA4	VSSPLL1_0	P	
L20	VSSOSC	P	Digital GND
H10	VDD5IF(2.5V)-0	P	2.5V Analog Supply
G19	VDD5IF(2.5V)-1	P	
D6	LD0_VDDA	P	5.0V Analog Supply
D7		P	
E6		P	
E7		P	
D15	LD1_VDDA	P	
D16		P	
E15		P	
E16		P	
J8	VDD5(DAC)-0	P	
K15	VDD5(DAC)-1	P	
H8	VDD5(REF/SWITCHES)-0	P	5.0V Analog Supply
K18	VDD5(REF/SWITCHES)-1	P	
AA3	VCCPLL1_0	P	1.2V PLL Supply
AA12	VCCPLL1_1	P	
AA10	VCCPLL2_0	P	
AA19	VCCPLL2_1	P	
M14	VDD	P	1.2V Core Supply
M5		P	
M8		P	
N18		P	

Ball	Symbol	Pad Type	Description
P15	VDD	P	1.2V Core Supply
P5		P	
R14		P	
R18		P	
R8		P	
R9		P	
T5		P	
U18		P	
V14		P	
V17		P	
V5		P	
V8		P	
E5	VDD1_3.3_0	P	3.3V Digital I/O Supply
E14	VDD1_3.3_1	P	3.3V Digital I/O Supply
K8	VDD2_3.3_0	P	
J15	VDD2_3.3_1	P	
E9	VDD3_3.3_0	P	
F18	VDD3_3.3_1	P	
E8	VDD4_3.3_0	P	
E17	VDD4_3.3_1	P	
L9	VCCOSC(3V)-0	P	
L19	VCCOSC(3V)-1	P	
L5	VDDPST	P	
N14		P	
N15		P	
N5		P	
R10		P	
R13		P	
R5		P	
T18		P	
V16		P	
V6		P	
A8	VGAVDD(2.5V)-0	P	2.5V Analog Supply
A18	VGAVDD(2.5V)-1	P	
B9	VDD2.5(ADC)-0	P	
B18	VDD2.5(ADC)-1	P	
G5	VDD2.5(DAC)-0	P	
H13	VDD2.5(DAC)-1	P	
H11	VDD2.5_DEC-0	P	
H18	VDD2.5_DEC-1	P	

Ball	Symbol	Pad Type	Description
F5	VDD2.5_INT-0	P	2.5V Analog Supply
E13	VDD2.5_INT-1	P	
J5	VDD2.5(DCXO/PLL30M)-0	P	
H15	VDD2.5(DCXO/PLL30M)-1	P	
H5	VDD2.5(REF/PLL240M)-0	P	
H14	VDD2.5(REF/PLL240M)-1	P	
L8	VSS	P	Digital GND
M10		P	
M11		P	
M12		P	
M13		P	
M18		P	
M4		P	
M9		P	
N10		P	
N11		P	
N12		P	
N13		P	
N17		P	
N6		P	
N8		P	
N9		P	
P10		P	
P13		P	
P17		P	
P18		P	
P4		P	
P6		P	
P8		P	
P9		P	
R17		P	
R6		P	
T17		P	
T4		P	
T6		P	
U10		P	
U11		P	
U12		P	
U13		P	
U14		P	

Ball	Symbol	Pad Type	Description
U15	VSS	P	Digital GND
U16		P	
U17		P	
U5		P	
U6		P	
U7		P	
U8		P	
U9		P	
V13		P	
V18		P	
V9		P	
L4	VSSPST	P	Digital GND
M15		P	
N4		P	
P11		P	
P12		P	
P14		P	
R11		P	
R12		P	
R15		P	
R4		P	
U4		P	
V15		P	
V7		P	
B4	LDGND-0	P	Analog GND
B5		P	
B6		P	
B7		P	
C4		P	
C5		P	
C6		P	
C7		P	
D4		P	
D5		P	
F10		P	
F6		P	
F7		P	
F8		P	
F9		P	
G6		P	

Ball	Symbol	Pad Type	Description
H6	LDGND-0	P	Analog GND
J6		P	
B13	LDGND-1	P	Analog GND
B14		P	
B15		P	
B16		P	
C13		P	
C14		P	
C15		P	
C16		P	
D13		P	
D14		P	
F13		P	
F14		P	
F15		P	
F16		P	
F17		P	
G17		P	
H17		P	
J17		P	
D17	DGND	P	Digital GND
D8		P	
E10		P	
E11		P	
E12		P	
E19		P	
E4		P	
F12		P	
F19		P	
F3		P	
K10		P	
K11		P	
K12		P	
K13		P	
L10		P	
L11		P	
L12		P	
L13		P	
L14		P	

Note:

Term	Description	Term	Description
I	Input	A/O	Ananlog output
O	Output	IPU	Internal pull up
I/O	Input and Output	P	Power
A/I	Ananlog input		

5. Technical Characteristics

5-1 Absolute Maximum Ratings and Environmental Limitations (REFERENCED to VSS)

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage (CMOS I/O)	$VDD_{IO/PLL}$	-0.3	3.9	V	Note 1,4
Supply voltage (Core)	VDD_{CORE}	-0.3	1.32	V	Note 1,4
DC input voltage	V_{IN}	-0.5	5.5	V	Note 1,4,5
Storage temperature range	T_S	-55	+150	℃	Note 1
Ambient operating	T_A	-40	+85	℃	0 ft/min linear airflow
Temperature	ME	5		Level	Per IPC/JEDEC
Moisture exposure level	RH	30	60	%	Note 2
Relative humidity, during assembly	RH	0	100	%	Non-condensing
ESD classification	ESD	2		kV	Note 3

Notes：

1. Operating conditions outside the min-max ranges specified may cause permanent device failure. Exposure to conditions near the min or max limits for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per JEDEC JESD22-A114-B.
4. Device core is 1.2V only.
5. MT5302 is 5 V compatible in the sense that the output logic 1 (VOH) and output logic 0 (VOL) levels of the MT5302 outputs have been specified at the same voltage levels that have been commonly recognized as logic 1 and logic 0 for the 5 V environment. MT5302 can generally be expected to drive 5 V TTL compatible components. However, while MT5302 outputs are able to meet the minimum input logic switching levels (VIH and VIL) of 5 V TTL compatible components, the output logic 1 output voltage of some 5 V components may exceed the maximum input voltage of MT5302. Depending on the technology and circuit implementation, the 5 V TTL compatible components may drive their outputs anywhere from 3 V to their VDD supply level. CAUTION: Before connecting a 5 V component to the MT5302, always check to be sure that the Maximum VOH of the 5 V device does not exceed the specified Maximum VIN listed in the table above.

5-2 Thermal Characteristics

Parameter	Min	Typ	Max	Unit	Conditions
Thermal resistance-junction to ambient		18		℃/W	0 ft/min linear airflow

5-3 Power Requirements

Parameter	Min	Typ	Max	Unit	Conditions
V_{DDIO}	2.67	3.3	3.96	V	
I_{DDIO}	20			mA	See Notes 1and 2
P_{DDIO}	53.4			mW	See Notes 1and 2
V_{DDPLL}	3.15	3.3	3.45	V	
I_{DDPLL}	1	1	1	mA	See Notes 1and 2
P_{DDPLL}	3.2	3.3	3.5	mW	See Notes 1and 2
V_{DDCORE}	1.12	1.2	1.31	V	
I_{DDCORE}	320	320	335	mA	See Notes1and 2
P_{DDCORE}	358.4	384.0	438.9	mW	See Notes 1and 2
Total Power	450	450	550	mW	See Notes 1 and 2

Notes：

1. Typical values estimated with nominal voltages at 25° C.
2. All IDD and PDD values are dependent upon VDD.

5-4 Input, Output and Input/Output Parameters

5-4-1 Input Parameters For LVTTL

Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	2.0			V	$3.14 \leqq V_{DD33} \leqq 3.46$
V_{IL}			0.8	V	$3.14 \leqq V_{DD33} \leqq 3.46$
Input leakage current	-10		10	μA	V_{IN}= V_{DD33} or V_{SS}
Input capacitance		5		pF	

5-4-2 Input Parameters For LVTTLpu (internal pull-up resistor)

Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	2.0			V	$3.14 \leqq V_{DD33} \leqq 3.46$
V_{IL}			0.8	V	$3.14 \leqq V_{DD33} \leqq 3.46$
Input leakage current	-10		10	μA	V_{IN}= V_{DD33} or V_{SS}
Input capacitance		5		pF	

5-4-3 Output Parameters For CMOS 16mA

Parameter	Min	Typ	Max	Unit	Conditions
V_{OH}	2.4			V	1_{OH}=-16mA
V_{OL}		0.2	0.4	V	1_{OL}=16mA
I_{OL}			16.0	mA	
I_{OH}			-16.0	mA	
Leakage tristate	-10		10	µA	

5-4-4 Input/Output Parameters For LVTTL/CMOS 16mA

Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	2.0			V	$3.14 \leqq V_{DD33} \leqq 3.46$
V_{IL}			0.8	V	$3.14 \leqq V_{DD33} \leqq 3.46$
Input leakage current	-10		10	µA	V_{DD33}=3.46
Input capacitance		5		pF	
V_{OH}	2.4			V	1_{OH}=-16mA
V_{OL}		0.2	0.4	V	1_{OL}=16mA
I_{OL}			16.0	mA	
I_{OH}			-16.0	mA	

5-5 Timing Characteristics

This section presents the detailed timing characteristics for the MT5302 in Figure 9 through Figure 10 with values of the timing parameters tabulated below each waveform diagram. Detailed timing diagrams for the MT5302 device are provided in this section, with values for the timing intervals given in tables below the waveform drawings. All output times are measured with a 25 pF load capacitance for Max conditions and 5 pF load capacitance for Min conditions, unless noted otherwise. Timing parameters are measured at voltage levels of (VIH+VIL)/2 and (VOH+VOL)/2, for input and output signals, respectively. All input transition times, 10/90%, used for timing measurements are 1.0 ns for Max conditions and 0.2 ns for Min conditions.

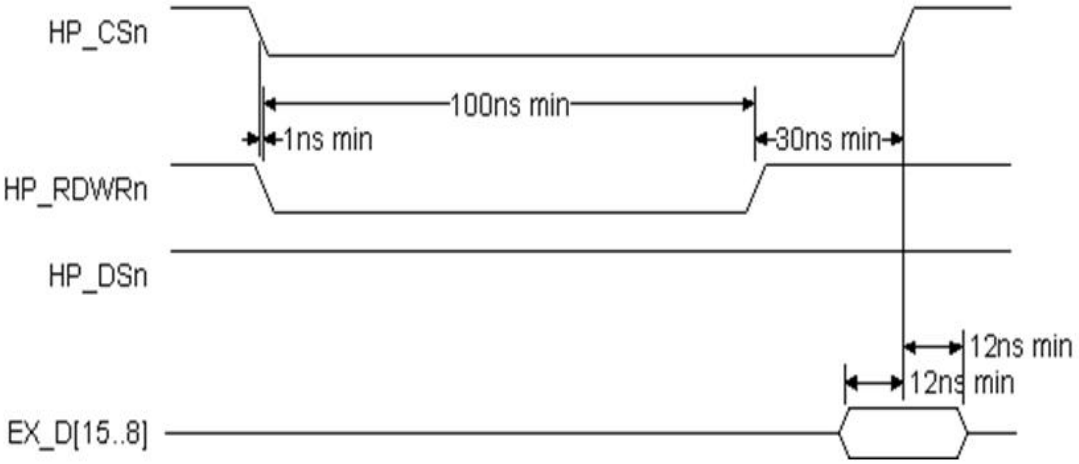


Figure 10 Host Port Read Cycle Timing

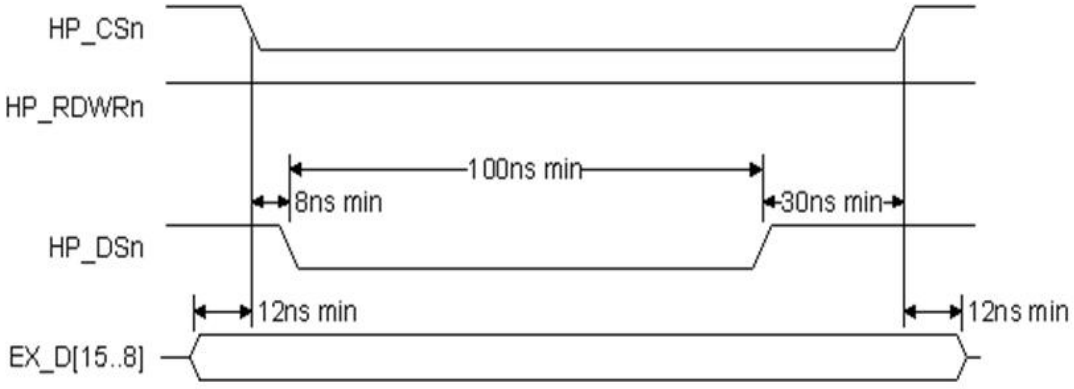


Figure 11 Host Port Write Cycle Timing

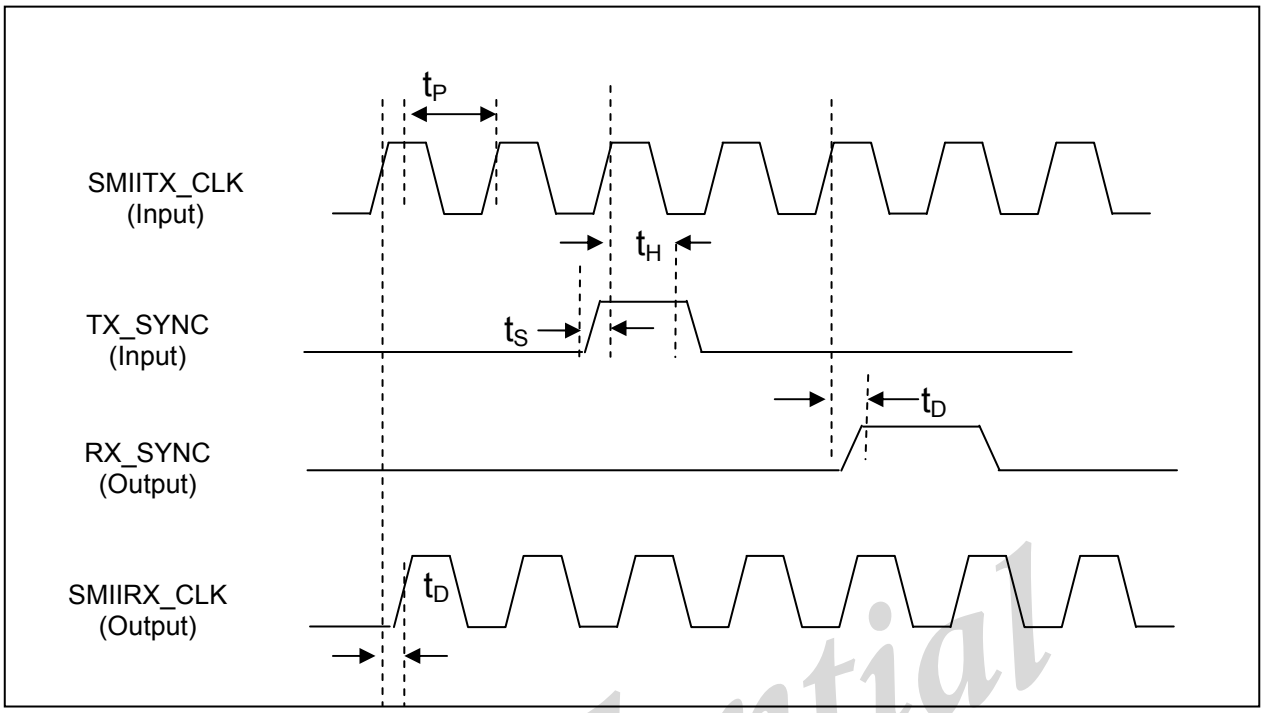


Figure 12 SMII Sync In/Out Timing

Parameter	Symbol	Min	Typ	Max	Unit
SMIITX_CLK and SMIIRX_CLK period	t_P		8.0		ns
SMIITX_CLK and SMIIRX_CLK duty cycle		40		60	%
TX_SYNC setup time to SMIITX_CLK↑	t_S	1.5			ns
TX_SYNC hold time from SMIITX_CLK↑	t_H	1.0			ns
RX_SYNC/SMIIRX_CLK delay from SMIITX_CLK↑	t_D	1.5		4.5	ns

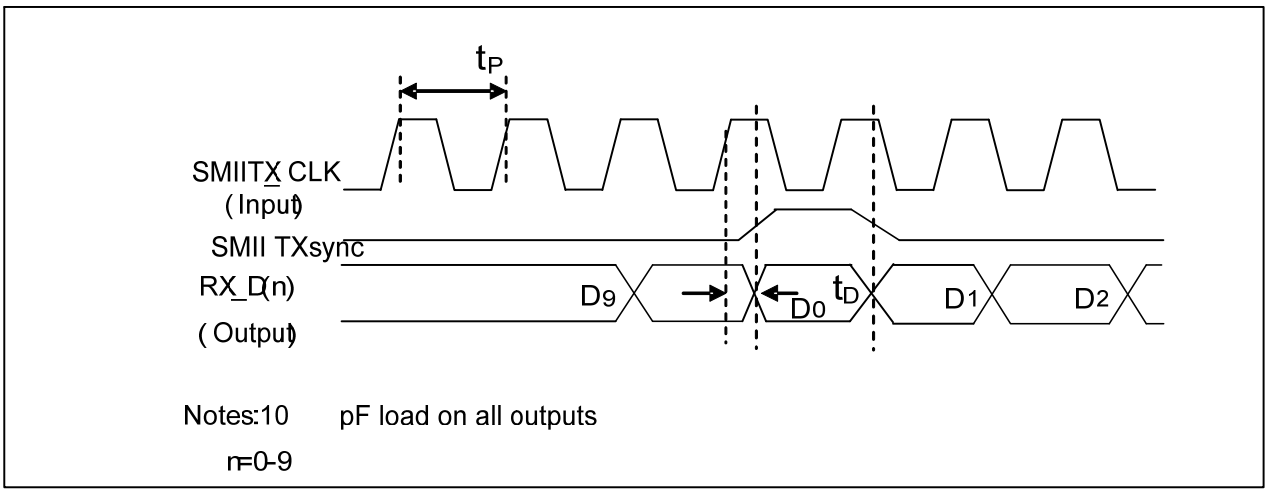


Figure 13 SMII Receive Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
RX_D(n) delay from SMIITX_CLK↑	t_D	1.5		4.5	ns

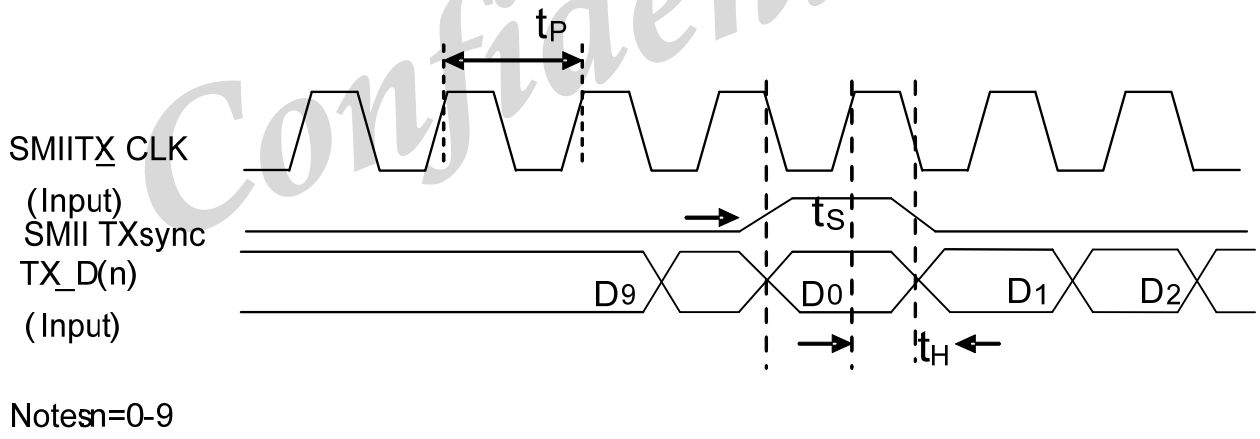


Figure 14 SMII Transmit Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
TX(n) setup to SMIITX_CLK↑	t_S	1.5			ns
TX(n) hold from SMIITX_CLK↑	t_H	1.0			ns

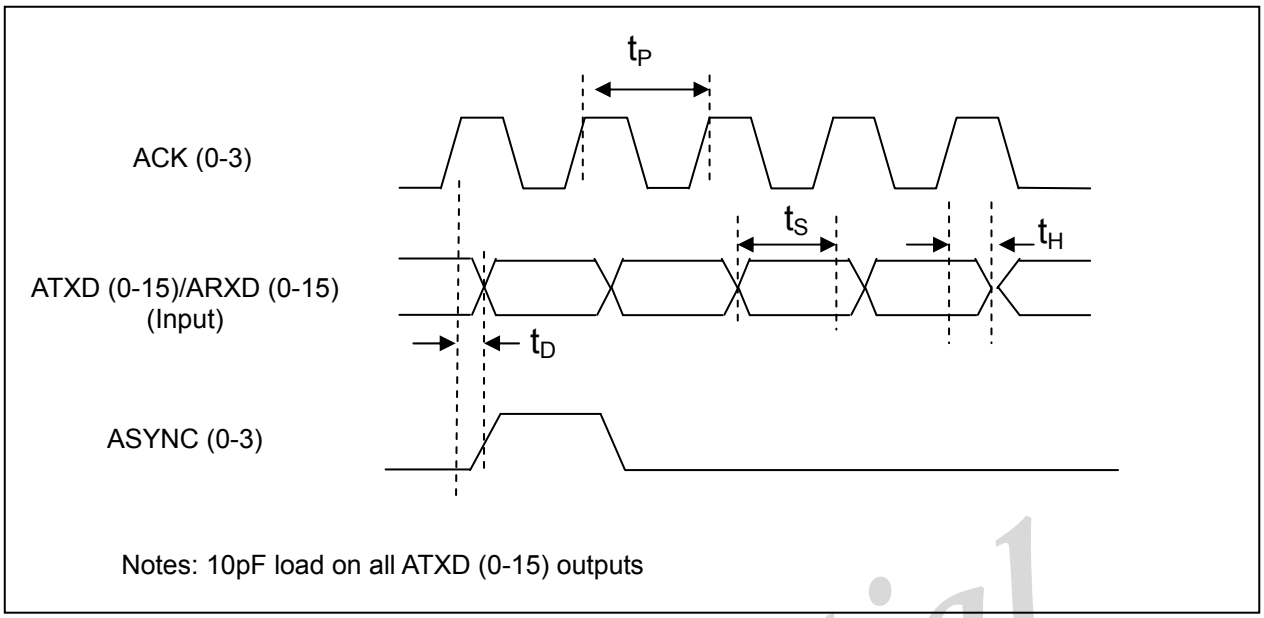


Figure 15 Analog Front End (AFE) Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
ACCLK(0-3) frequency	$1/t_P$		35.328		MHz
ACCLK(0-3) duty cycle	t_P		28.03		ns
ATXD(0-15)/ARXD(0-15) delay from ACLK↑	t_D	10		100	ns
ATXD(0-15)/ARXD(0-15) setup to ACLK↑	t_S	15			ns
ATXD(0-15)/ARXD(0-15) hold from ACLK↑	t_H	0.0			ns

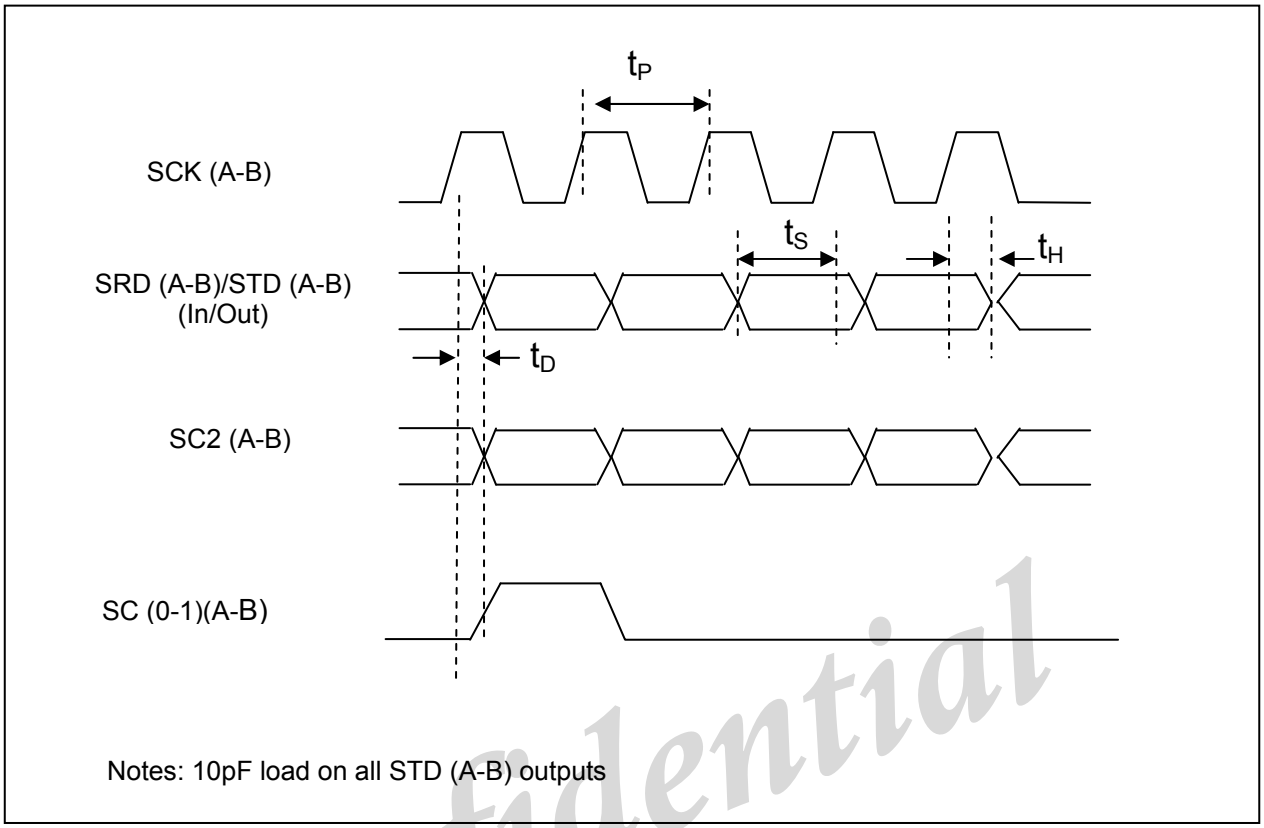


Figure 16 Serial Port A-B Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
SCK(A-B) frequency	$1/t_P$	0.036		37.5	MHz
SCK(A-B) duty cycle	t_P	30		30000	ns
SRD(A-B)/STD(A-B) delay from SCK↑	t_D	10		100	ns
SRD(A-B)/STD(A-B) setup to SCK↑	t_S	15			ns
SRD(A-B)/STD(A-B) hold from SCK↑	t_H	0.0			ns
SC(0-2)(A-B) delay from SCK↑	t_D	10		100	ns

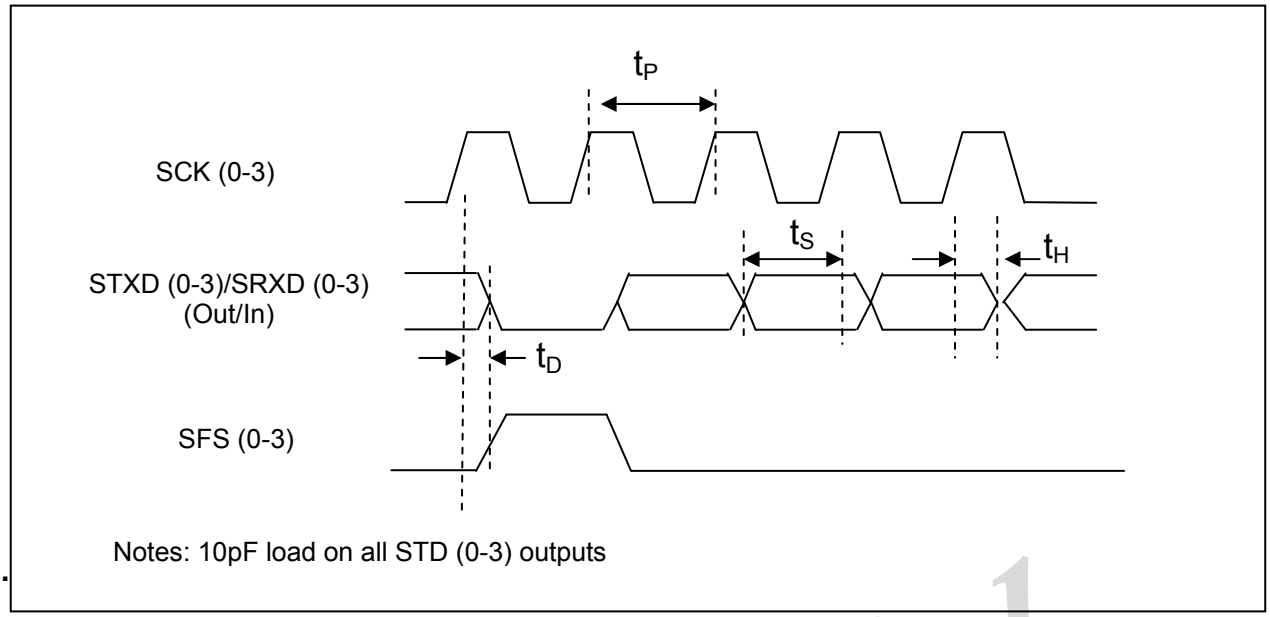


Figure 17 Serial Port 0-3 Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
SCK(0-3) frequency	$1/t_P$	27		33.3	MHz
SCK(0-3) duty cycle	t_P	30		35	ns
STXD(0-15)/SRXD(0-15) delay from SCK↑	t_D	10		100	ns
STXD(0-15)/SRXD(0-15) setup to SCK↑	t_S	15			ns
STXD(0-15)/SRXD(0-15) hold from SCK↑	t_H	0.0			ns

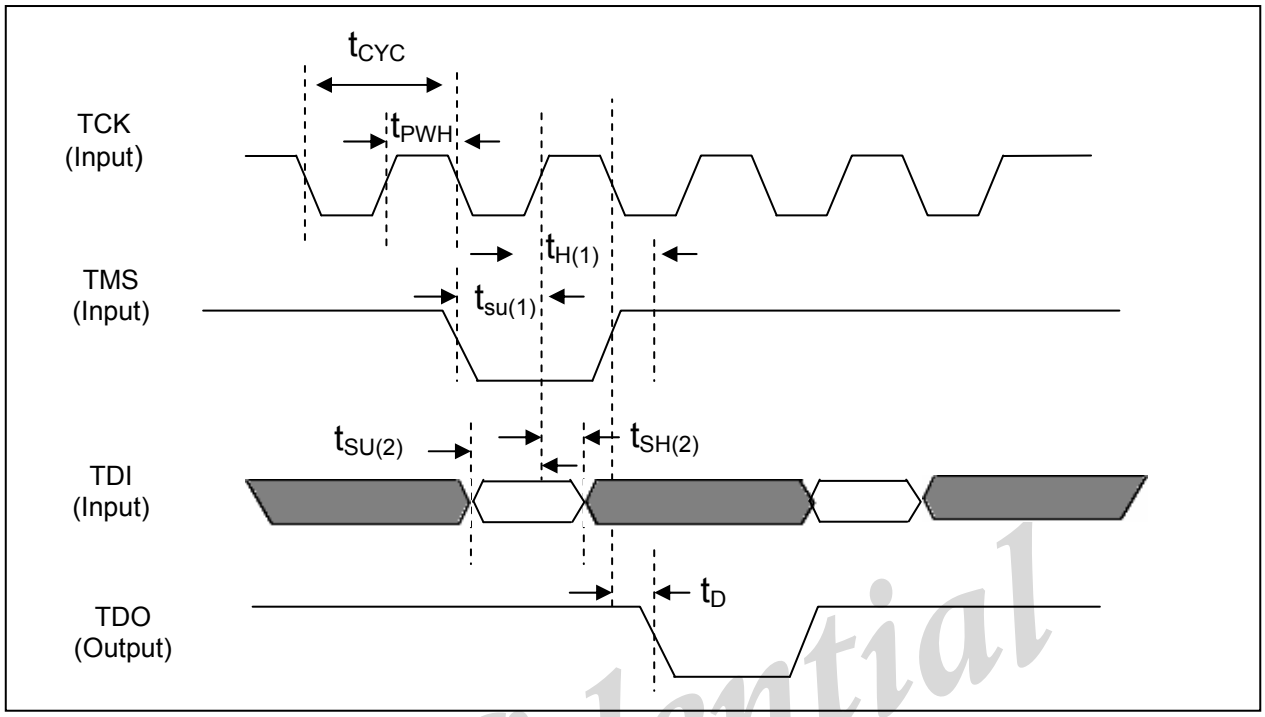
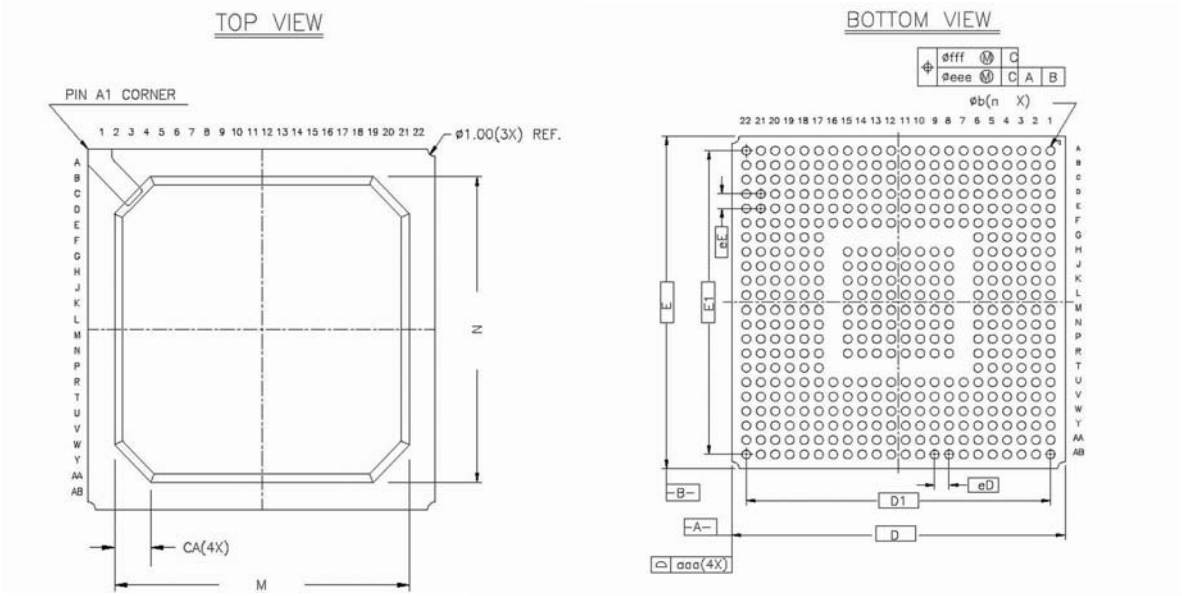
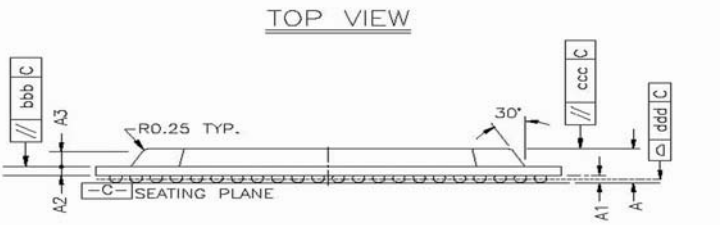


Figure 18 Boundary Scan Timing

Parameter	Symbol	Min	Max	Unit
TCK clock cycle time	t_{CYC}	50		ns
TCK clock duty cycle	t_{PWH}/ t_{CYC}	40	60	%
TMS setup time before TCK↑	$t_{SU(1)}$	4.0		ns
TMS hold time after TCK↑	$t_{H(1)}$	1.0		ns
TDI setup time before TCK↑	$t_{SU(2)}$	6.0		ns
TDI hold time after TCK↑	$t_{H(2)}$	1.0		ns
TDO delay after TCK↑	t_D		15.0	ns

6. Package Information: 448 LBGA 23x23mm





		Symbol	Common Dimensions
Package :			SBS BGA
Body Size:	X	D	23.000
	Y	E	23.000
Ball Pitch :	X	eD	1.000
	Y	eE	1.000
Total Thickness :		A	2.230 +/- 0.136
Mold Thickness :		A3	1.170 Ref.
Substrate Thickness :		A2	0.560 Ref.
Ball Diameter :			0.600
Stand Off :		A1	0.400 ~ 0.600
Ball Width :		b	0.500 ~ 0.700
Mold Area :	X	M	19.500
	Y	N	19.500
Chamfer		CA	2.400 Ref.
Package Edge Tolerance :		aaa	0.200
Substrate Flatness :		bbb	0.250
Mold Flatness :		ccc	0.350
Coplanarity:		ddd	0.200
Ball Offset (Package) :		eee	0.250
Ball Offset (Ball) :		fff	0.100
Ball Count :		n	448
Edge Ball Center to Center :	X	D1	21.000
	Y	E1	21.000

Figure 19 Package

7. Ordering Information

Prefix	Part No. (4 numbers)	Package			Version
		RoHS or Not	Package Type		
MT	5302	G: **Green Product** N: **Pb Product**	N: **QFN** P:**QFP** L: **LQFP** C:**CHIP** B:**BGA**	-	A1

Part Number

- MT5302GB-A1: Dual port VDSL2 DMT+AFE chip with LBGA 448 pin package.