METANOIA

Data sheet MT2301

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Data sheet MT2301

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MT2301 Product Overview

General Description

The MT2301 is part of the Metanoia VDSL2 chipset solution named MT2301. It is a single chip programmable Discrete Multi-Tone (DMT) Digital Subscriber Loop (DSL) digital modulator/ demodulator processor units for broadband access. The Device supports all committee T1E1.4 and ITU-T G.993.2 DSL discrete multi-tone based specifications, as well as IEEE 802.3 10PASS-TS.

Key Features

- Single chip configurable DMT data pump supporting 100Mbps/100Mbps DS/US payload data rate.
- Up to 3072 DMT carriers supported in the downstream and upstream directions.
- All 4096 DMT carriers can be used between U/DS, with four DMT pass-bands per direction
- Conformance to T1E1, ITU-T standards for VDSL2, and current IEEE 802.3ah draft for 10PASS-TS (EFM)
- Configurable band-plan, conforms to NA, EUR and Swedish Band-plans subject to the 3072/4096 and 8-band/4-passband constraints
- Trellis coding support for up to 3072 DMT carriers in any VDSL2 mode.
- Supports Seamless Rate Adaptation (SRA) and D-change
- Flexible QoS classification and queueing supports hardware based latency path routing
- Supports IEEE 802.3 MII single port and SMII dual port
- No external RAM required. Internal RAM booted from EEPROM, Flash, or external uP
- PHY software and management through IEEE 802.3 MDIO serial or a bi-directional octal interface
- Optimized to support low latency applications as required for voice
- 4 KHz and 8 KHz symbol rates allow variable bandwidth per bin
- 128-lead thin quad flat package (LQFP)

Applications

- IP digital Subscriber Loop Access Multiplexer solution
- Multi-Service Access Platforms (MSAP)
- Customer Premise/Located Equipment for Internet Access and VoIP

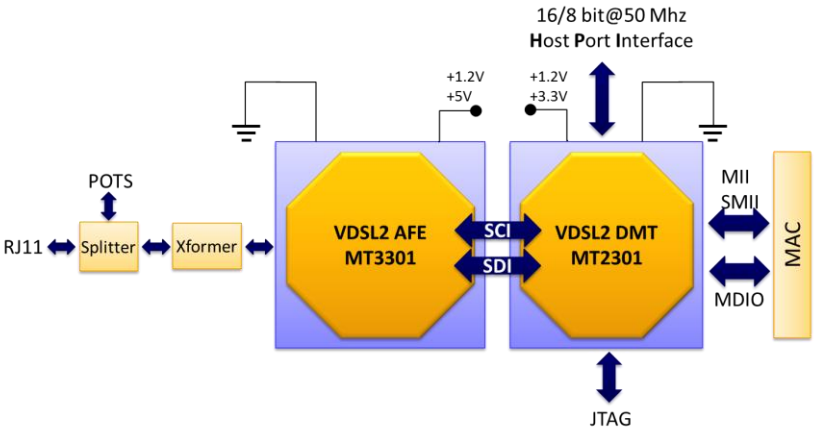

Figure 1: Interface overview

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1 General Description

1.1 MT2301 Key Features

The MT2301 supports the following features.

General Device Level

- Single chip configurable DMT processor
- Up to 3072 DMT carriers downstream
- Up to 3072 DMT carriers upstream
- Total DMT carriers U/D are limited to 4096
- Four DMT pass-bands in each direction
- Conformance to T1E1, ITU-T standards for VDSL2
- Conformance to current IEEE 802.3ah draft for 10PASS-TS (EFM)
- Configurable band-plan, conforms to North America, European and Swedish
- Band-plans subject to the 3072/4096 and 4-band /8-passband constraints
- Trellis coding support for up to 3072 DMT bins in any mode including VDSL2
- Programmable soft error detection and correction improves impulse noise rejection
- Supports Seamless Rate Adaptation (SRA) and D-change
- Programmable Upstream Band-split for DMT VDSL2
- Support for one VDSL2 Analog Front End
- IEEE 802.3 SMII/MII/GMII support for two SMII, one MII, and one GMII Media Access Controller.
- Support quality of service (QoS) classification and queueing based on VLAN and Ethertype
- Internal RAM for software stored in external flash or managed through MAC interface
- PHY software and management through IEEE 802.3 MDIO serial or a bi-directional octal interface
- Optimized to support low latency applications, as required for voice
- 4 KHz and 8 KHz symbol rates allow variable bandwidth per bin
- Advanced power management
- 128-lead LQFP package

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1.2 MT2301 Application examples

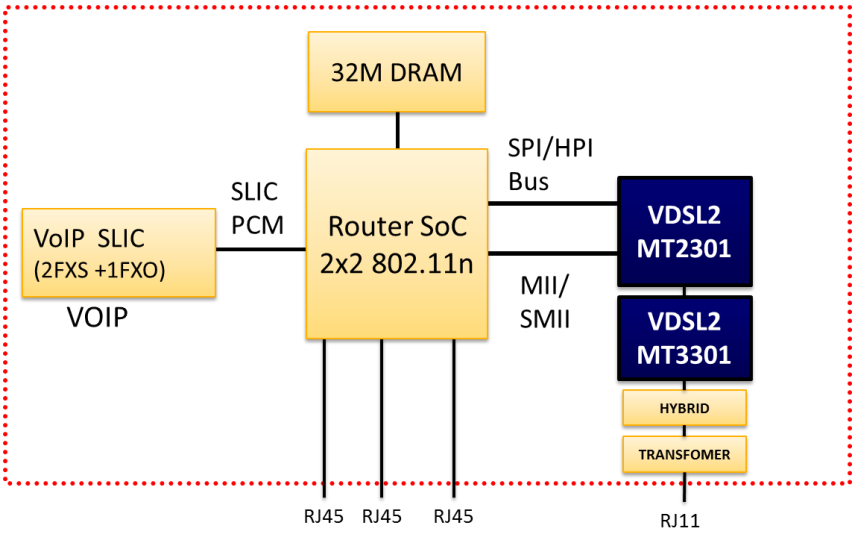

Figure 2: IAD Wifi Gateway

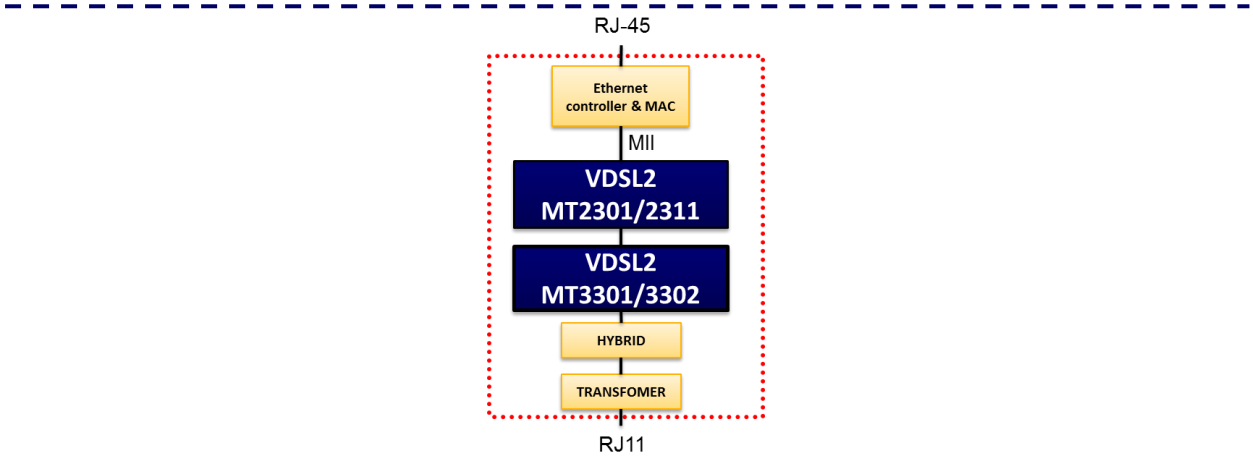

Figure 3: VDSL-Ethernet bridge

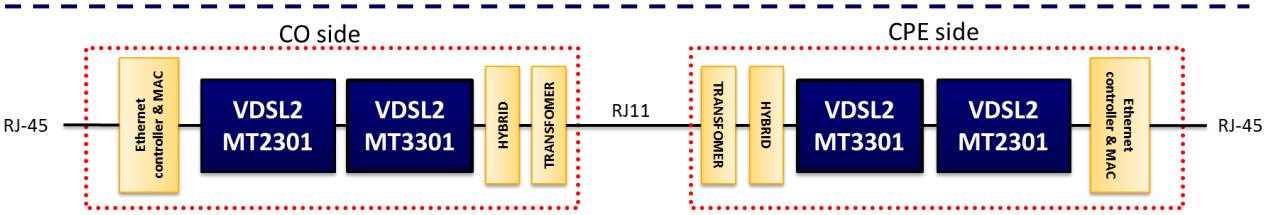

Figure 4: Point-to-point CO & CPE

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2 Device Description

2.1 Block Diagram

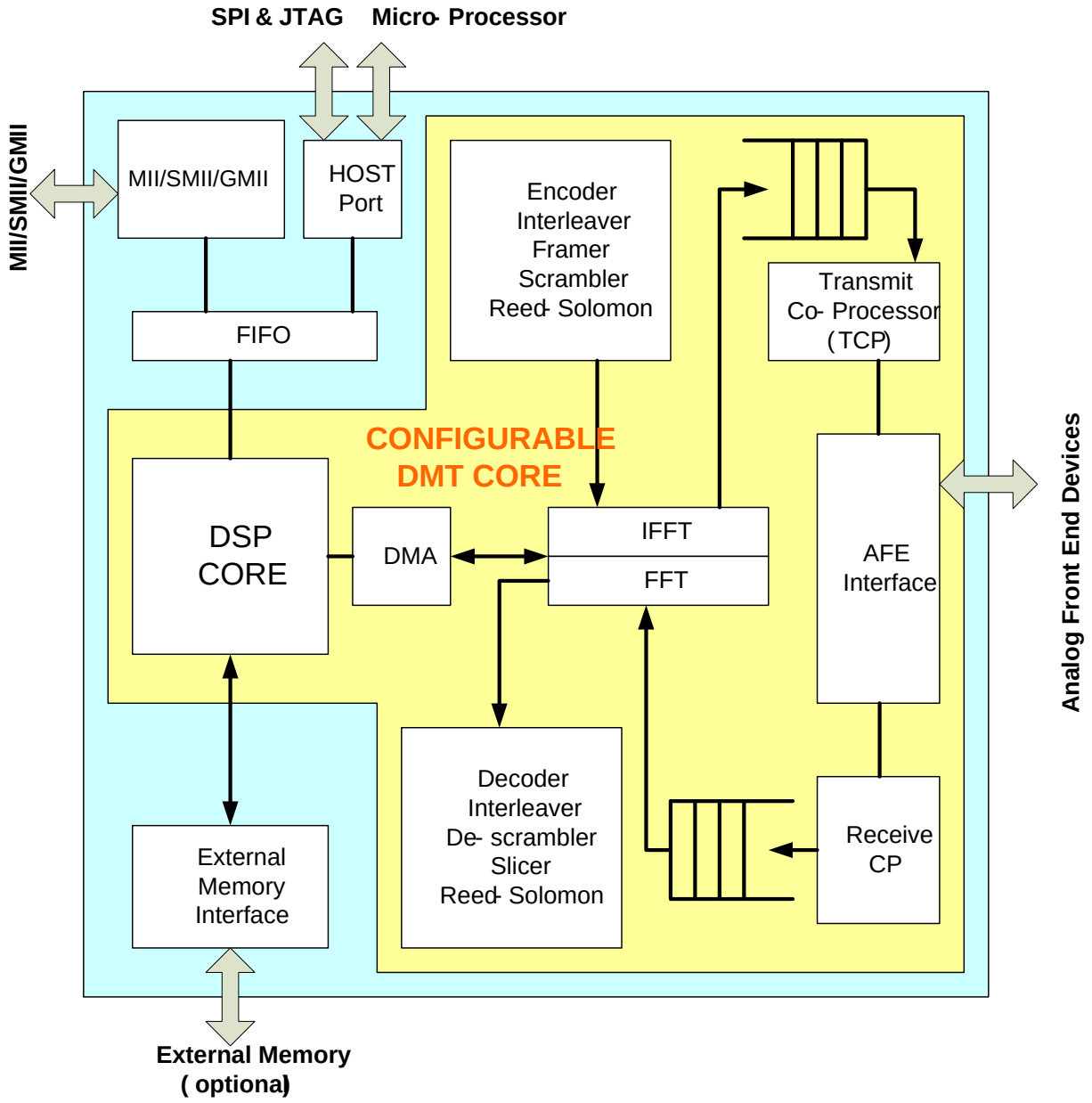

Figure 5 DAC block diagram

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2.2 Block Diagram Description

The MT2301 architecture is an area and power efficient implementation of a DMT data pump supporting all VDSL1/2 standards. To meet the high-speed calculation and dataflow requirements of a DMT VDSL2 engine the design was partitioned into a single DSP with multiple hardware coprocessor blocks. The DSP is used for higher-level functions and control while most DMT calculations and data movement are performed in the hardware blocks.

The MT2301 ASIC performs all of the digital functions of a DMT based VTU-O or VTU-R physical interface. This includes all digital processing below the á and â interfaces in the VDSL2 reference model. The device is designed to be inserted into a system as an ATM or 10/100/1000 Ethernet PHY and Ethernet MII/SMII/GMII interfaces. The device can be controlled using the MDIO interface or a parallel host interface.

The top-level block diagram for the MT2301 chip is shown in Figure 5. The DSP core employed is compatible with a Motorola 56300 and thus contains an X, Y, and P memory space. All of the memory required for VDSL2 operation is provided on chip but an optional off chip memory can be used to support advanced features. The hardware coprocessors include an Encoder, Decoder, FFT coprocessor, TEQ coprocessor, and an AFE interface control processor. These processors perform all DMT operations from framing to cyclic extension and time domain filtering. The coprocessors are flexible enough to handle current and future DSL configurations but do not require a lot of attention from the DSP.

Each hardware block has a set of registers mapped in the X or Y peripheral address space of the DSP. A peripheral bus interface is used for transferring control information between the DSP and the hardware blocks. The local memory within each hardware block is also indirectly mapped into the peripheral address space via a memory port. This mapping gives the DSP the ability to setup DMA transfers of data to and from the distributed memories. Since a DMA interface is present on each block, DMA transfers can occur between any combination of hardware blocks, external memory, and the DSP. Between 1 and 16 wait states will be inserted per transfer when external memory is accessed using DMA. The number of wait states depends on the speed of the external memory. The external memory interface is provided for test, debug, and system expansion. External memory is not be required for normal VDSL2 DMT calculations.

Due to the high bandwidth requirements at various stages of the transmitter and receiver the DSP is not used for data movement. Instead each hardware block transfers data to the next under DSP control. These transfers are self-managing, controlled by DSP initialized parameters. Hardware flags are used to synchronize timing between processes. The data transfers occur on dedicated interfaces between each hardware block and the next logical block in the path. Since these interfaces are point-to-point, they are much simpler than those used for the bi-directional peripheral and DMA buses. The point-to-point buses are designed to efficiently support the dataflow requirements for Showtime operation. Since the requirements are different during training the point-to-point buses are configurable.
The hardware blocks can be triggered to begin performing calculations by the DSP or by a signal from another hardware block.

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2.3 Transmit Path Operation

The data to be transmitted to the remote modem arrives on the MII, SMII, GMII interfaces, and is deposited into a FIFO. Since the Ethernet interfaces aren't normally used simultaneously the FIFO is shared by all interfaces. The FIFO can logically be divided into up to four queues for multichannel operation or to support QoS queueing. The queues can be flexibly mapped into the two available latency paths provided by the VDSL2 datapump. This mechanism provides full support for the VDSL2 bearer channel mapping and also provides a method for routing data to latency paths based on QoS parameters. The queue data can be routed to the DSP memory or any other memory but for normal operation will be routed directly to the encoder.

The encoder performs framing, CRC generation, scrambling, interleaving, bit extraction, constellation encoding, and scaling as defined in the VDSL2 specification. The encoder functions are divided between two hardware modules that share a common DMA, peripheral bus, and local memory: the SRS (Scrambler and Reed-Solomon) and the ICE (Interleaver and Constellation Encoder) module. The encoder is designed to be reasonably generic and programmable by the DSP. This approach provides flexibility for future specification changes and allows for easier reuse of the hardware for training and other non-Showtime functions. The Scrambler/Reed-Solomon (SRS) block receives data either directly from the queues or from DMA and perform framing, CRC generation, scrambling, and Reed-Solomon encoding and then deposits the data in the Interleave memory. The Interleaver/ Constellation Encoder (ICE) block fetches data from the interleave memory and directly from the SRS to perform bit extraction, constellation encoding, rotation, and tone scaling. The complex addressing used for performing the GCI interleave function is normally done by the SRS block as it fills the interleave memory. However, for maximum flexibility the ICE block contains a fully programmable memory interface as well. The encoder fully supports the GCI interleaver function including the ability to perform dynamic interleaver parameter changes for all interleaver profiles up to 128 KB.

After constellation encoding the ICE block performs tone re-ordering and deposits the constellation points into the output FIFO (IFFT input ram). At the correct time the ICE transfers the tones to the FFT/IFFT engine. The per tone gain adjustment is applied as the tones are transfered The FFT/IFFT block is shared between transmit and receive paths but it can simultaneously perform 8192 point FFT and IFFT transforms at up to 8Khz symbol rates. The output of the IFFT is transferred to the TX FIFO. and cyclic extension is applied with full windowing support. The transmit time domain processor extracts the samples from the TX FIFO and performs time domain processing including image supression, POTs filtering, and echo cancellation (long reach VDSL).

The AFE interface block is designed to interface the chip to a VDSL2 AFE. The block is designed to be flexible enough to support existing and future AFEs. Up to 16 bits of data can be driven onto the TX leads and an additional 16 bits received on the RX leads on each 70.656 Mhz sample clock. This interface is flexible enough to support many devices.

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2.4 Receive Path Operation

In the receive direction the AFE interface receives one 16-bit sample per 70.656 MHz clock from the AFE and transfers the data to the Receive Co-Processor (RCP). The RCP performs time domain filtering including sample rate reduction and echo cancellation if necessary. Then it calculates the TEQ filter and transfers the samples to the RX FIFO.
Like the TX FIFO, the RX FIFO read and writes pointers are controllable by the DSP for use in symbol alignment. The FIFO can also be programmed to discard the cyclic prefix. After symbol sync is achieved, the RX FIFO can generate symbol rate timing signal. This signal defines the symbol boundary and can be used to trigger the other hardware blocks.

When the FFT block is available for performing an FFT, a symbol of data is burst transferred into the block. Like the IFFT, the FFT block takes advantage of the idle butterfly hardware to perform scaling during input/output transfers. The FFT/IFFT engine provides two 4096 entry gain tables that are shared between the IFFT input and FFT output. This structure allows all tones to have a separate gain and allows the gain updates to be performed at any time to support bit swap operations. The FFT signals the FCP and/or DSP when the output is ready. The FCP performs the FEQ filtering (including filter training), slicing, Viterbi decoding, SNR calculations, and framing. To save processing time and hardware requirements the FCP only operates on the active bins for the RX direction. The FCP block performs reverse tone ordering as it reads the data out of the FFT Output buffer. To facilitate training symbol recovery, the FCP also has pseudo-random number generator and tone rotator.

The FCP contains a specialized complex data processor that is capable of performing all FEQ, SNR, and slicing operations. The processor contains it s own program space that is written by the DSP. When the FCP has re-assembled the bit stream, it writes the data into the de-interleave memory including erasure information for soft detected errors. The de-interleaver complexity occurs in the DRS module but the FCP also has the ability to perform complex transfers to memory and the DMA bus. The de-interleave memory is shared with the DSP in the same fashion as the interleave memory. Simultaneous accesses by the DSP and hardware will result in hardware wait states. The FCP signals the DRS and/or DSP when enough data is available for de-interleaving to begin.

De-interleaving, Reed-Solomon decoding, CRC check, and de-scrambling are performed by the DRS block. The de-interleave function is performed by the addressing logic as data is fetched for Reed-Solomon decoding. Unlike the Reed-Solomon encoder, the decoder needs to have access to a full code word of data in case it needs to make corrections. Therefore, the Reed-Solomon decoder has a local 255 byte buffer to hold the maximum sized Reed-Solomon code word and an additional 255 bits for erasure information. After any corrections are made the data is de-scrambled, CRC checks are performed at super-frame boundaries, VOC and other the fast bytes are extracted and DMA transferred to DSP memory for DSP access. The de-framing logic has the same degree of programmability as the framer in the SRS block. The final output of the block is either point-to-point or DMA transferred to DSP memory or directly to the MII/SMII/GMII interface FIFO.

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2.5 Analog Front End (AFE) Interface

The AFE Bus interface is designed to support several VDSL2 AFEs.The AFE interface provides analog connectivity between the Analog Front End IC and time domain coprocessors (RCP and TCP) within the MT2301 device. The MT2301 device can be interfaced to multiple Analog Front Ends. The list below provides reference for different vendors and applications.

	AFE	Application
Metanoia	MT3301	Dual channel VDSL2 (CO)
	MT3301	Single channel VDSL2 (CO, RT)

Table 1 AFEs and Their Vendors Already Supported by MT2301

The following signals are sent from the AFE to the MT2301 device:

ADC [15:0] - 14-bits of receive data (clocked on either edge of clock)

DAC [15:0] - 14-bits of transmit data (clock on either edge of clock)

CLK - AFE clocks

SYN - AFE synchronization operation

The RX data received from the AFE is 16-bits wide but internally the MT2301 device supports up to 16 bits. The two LSBs are not bonded out in the 128 pin package. The AFE interface module decodes the combination of clock and sync to determine if valid data is available. The interface packs shorter format data into a 16-bit word register at the input of a four sample fall-through stack (one per channel) for processing by the RCP (receive time coprocessor) module. Samples are passed on a P2P (point-to-point) bus to the RCP channel selected by priority encoding with the deepest stack serviced first.

The TX path is largely the inverse of the RX. Data is fetched from the output of a 8-deep circular queue (one per channel) and then transmitted on the TX interface 16-bits at a time. As a sample is removed from the queue, a request is made to re-supply the queue with a new sample being entered into the TCP (transmit time coprocessor) module. As a sample exits the TCP the sample is added to the queue. As long as a sample is produced soon enough the queue always has data available to transmit. The eight sample queue is needed to smooth out potential sample bursts caused by TCP interpolation.
The 16-bit data paths are configured as 16-bits parallel interfaces to match AFE device but currently only 14 bits appear on the interface. Each sync pulse and clock is associated with a particular ADC and DAC I/O leads for the specified mode of operation.

16-bit parallel:	ADC[15:2], DAC[15:2], CLK0, SYNC0

Table 2 Analog Front End (AFE) Configurations

AFE Interface is controlled by a 24-bit control register which can be configured and modified via API command. The controls provide the flexibility to support many AFE devices.

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Bit	Symbol	Description
23-20	AFE_WCNT_MASK	This is a mask for the word counter. It generates a circular word count for the number of serial words (or bits in serial mode) between sync pulses.
19-16	AFE_WCNT_AOFF	This offsets the ADC word count prior to masking by the word count mask above. It essentially rotates the count to the proper alignment to match the
15-12	AFE_WCNT_DOFF	This offsets the DAC word count prior to masking by the word count mask above. It essentially rotates the count to the proper alignment to match the
11	BIG_ENDIAN	Enables big endian transfers (MSBs first) on Word wide interfaces.
10-8	AFE_WSIZE	Defines the number of bits transferred on the interface in parallel. For each transfer clock edge.
7	DDR	Enables double data rate mode. Data is supplied on both edges of the clock
6	AFE_SYNC_POL	Defines the polarity of the sync pulse. The sync pulse is always sampled on the negative edge of the clock. 0 = positive pulse 1 = negative pulse
5	AFE_ADC_POL	Defines the edge on which the ADC input is sampled. 0 = positive edge 1 = negative edge
4	AFE_DAC_POL	Defines the edge on which the DAC sample is clocked 0 = positive edge 1 = negative edge
3	DAC_CLK_OUT	Enables the DAC interface clock to be driven onto bit 5 of the DAC data bus. The supplied clock is a delayed version of the AFE input clock.
2	DAC_SYNC_OUT	Enables the DAC sync signal to be driven onto bit 6 of the DAC data bus. Depending on the WCNT settings, the DAC sync may or may not match the sync provided by the AFE.
1	Reserved	Reserved
0	AFE_CLK0	Enables AFE#0 clock 0 = Disabled 1 = Enabled

Table 3 AFEFR as Shown in the Following Table

The word count mask specifies the 2^n count value of a circular word counter. This is generally set to the number of data samples between sync pulses.

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For the 16-bit parallel interface, setting the word count mask to anything other than zero creates a multi-channel mode, e.g., word count mask = 1 interleaves samples of channel 0 and channel 1 with the sync0 pulse determining the channel assignment. Setting word count mask = 3 specifies a 4-channel mode. With word count mask = 0 the sync pulse is ignored and the interface is clamped at channel 0. The nibble and byte-serial modes transmit least significant portion of the word first in time. The bit and dibit-serial modes transmit most significant portion of the word first in time. This matches the individual specifications of the AFE devices supported.

Individual word count offsets for both the ADC and DAC allow the sync pulse position to have an arbitrary alignment relative to the channel data. They essentially rotate the word count to match the channel number or word position of the data being transferred by the interface.

The AFE block is equipped with a low-power gated clock mode. Setting the soft reset bit of the CTL register will gate off the clock for the module and reset all logic. This capability is useful for reducing power consumption when MT2301 is not operating.

The AFE interface usessingle clocks: CLK. These clocks are asynchronous to the system clock; however, the minimum period (14.15 ns) must beat least twice the system clock period.Two snapshot registers capture different portions of the ADC input on each of the selected external clock edges. This guarantees proper operation for clock frequencies up to 70 MHz. Each external clock is double delayed and differentiated for both positive and negative edge. Double delayed input data is captured on the selected pos/neg edge. Output data is supplied on the selected pos/neg edge. Sync pulses are always captured on the negative edge since all supported converters provide sync pulses synchronous with the positive edge of their respective clocks.

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2.6 Ethernet Interfaces

The Media Independent Interface (MII ,SMII or GMII) provides Ethernet connectivity between 10/100/1000 Media Access Control (MAC) and Physical Layer (PHY) devices. To support EFM flow control, the MAC/PHY can be configured for half-duplex operation, i.e., as if the PHY were connected to a multi-drop Ethernet coax. This module implements the nibble wide data interfaces and serial control interface defined in the IEEE STD 802.3 clauses 22, 45, 61, 62. It performs the time critical lower level functions of the MII interface. The DSP handles higher-level functions in software.

The module is made up of a transmit path, a receive path, and a control section. To avoid confusion with the Ethernet specification, transmit and receive paths are defined with respect to the Ethernet MAC and the modem itself. Since this interface implements the PHY side of the MII the transmit (tx) path is the input and the receive (rx) path is the output.
Direct input/output FIFO connections avoid DSP assisted data transfers. Extended Management Data register set is visible to DSP and external MAC. Simple interrupt driven software interface saves DSP MIPs. A low power, gated-clock mode is provided. The Figure 6 below shows a block diagram of this interface.

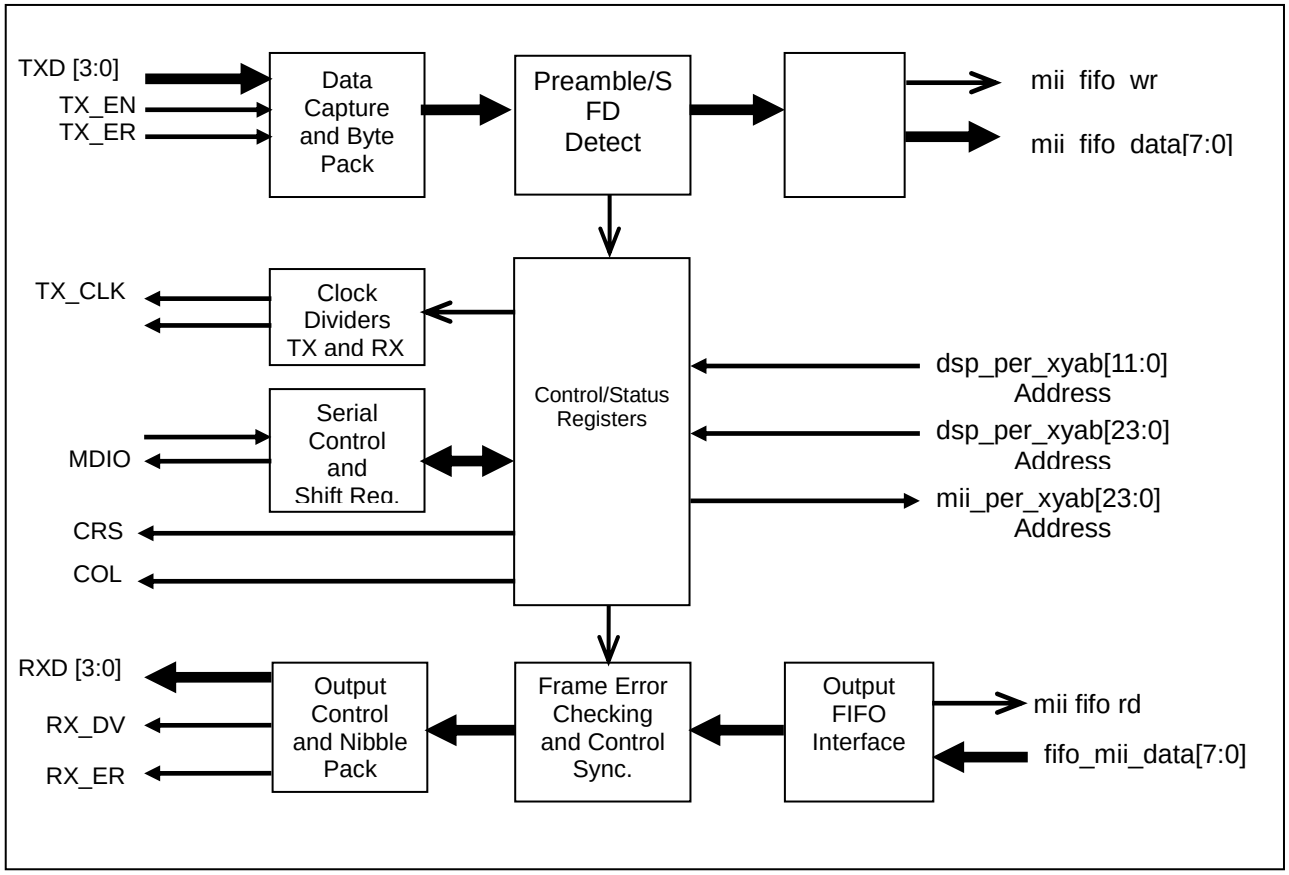

Figure 6 MII Interface Block

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2.6.1 MII Operation

The data received from the Ethernet MAC on the TX interface is four bits wide. The MII module decodes the combination of UT_TXEN, UT_TXER, and UT_TXD to determine if a valid nibble is currently on the interface. The nibble is valid if UT_TXEN is asserted even when UT_TXER is also asserted. The interface packs each pair of input nibbles into a byte (least significant nibble first in time) for use by the framing logic and FIFO interface. The number of nibbles in an Ethernet frame will normally be even so that all bytes are fully packed.

Leads	Description
UT_TXD[3:0]	Nibble transmit data (clocked on positive edge of TX_CLK)
UT_TXEN	Transmit framing (clocked on positive edge of TX_CLK)
UT_TXSOC/UT_TXER	Transmit coding error (clocked on positive edge of TX_CLK)
UT_RXD[3:0]	Nibble receive data (clocked on negative edge of RX_CLK)
UT_RXEN/UT_RXDV	Receive data valid (clocked on negative edge of RX_CLK)
UT_RXSOC/UT_RXER	Receive error (clocked on negative edge of RX_CLK)
UT_TXCLAV/UT_CRS	Carrier sense (asynchronous signal)
UT_RXCLAVUT_COL	Collision (asynchronous signal)
UT_TXCLK	25 MHz transmit clock, ±100ppm local crystal
UT_RXCLK	25 MHz receive clock, ±100ppm local or remote crystal

After the valid nibbles are packed into bytes the byte stream is checked for the Ethernet framing signals: the preamble and the Start Frame Delimiter (SFD). After UT_TXEN goes active, the MAC sends a preamble of seven bytes of 0x55 followed by one byte of 0xd5 followed by up to 1522 bytes of data. After frame detection the byte stream is sent to the aggregation function. The MAC de-asserting UT_TXEN indicates the end of an Ethernet frame.

The RX path is largely the inverse of the TX. Data is fetched from the aggregation function, and then transmitted on the RX interface one nibble at a time. The interface signaling for the RX path uses UT_RXDx, UT_RXDV, and UT_RXER. Similar to the UT_TXEN signal, the rate matching function asserts the UT_RXDV signal for the duration of a packet transfer. After UT_RXDV goes active, the PHY sends one byte of 0xd5 followed by up to 1522 bytes of data. UT_RXDV then goes inactive. While configured for half-duplex operation, this should not preclude receiving data at the same time as transmitting. Output bytes are sent over the nibble wide UT_RXD data bus least significant bits first in time while UT_RXDV is active. The DSP has control of the UT_RXER signal via a register bit and the MII module synchronizes this signal to the interface and frame timing as necessary. This indicates the PHY has detected a data error in the current frame. An error is to be propagated by the MAC into the current frame being sent.

The carrier sense signal (CRS) is inactive in the idle state. It goes active in the 320 ns preamble period following UT_TXEN. Normally it would indicate when the Ethernet is actively passing information, local or another device. Since the MAC knows not to attempt to send a frame when another device is using the Ethernet, CRS is used to flow control the transmit data from the MAC. CRS is not returned to the inactive

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state until the PHY is prepared to accept another 1522 byte frame. Alternatively, the interface can use pause frames for flow control.
The collision signal (COL) is set when the PHY detects multiple devices transmitting at once. Typically this is used to get the MAC to retransmit a frame after a delay period while the PHY jams the Ethernet until detection of a collision causes both devices to drop carrier. Both back off and try again after a delay period. The 320 ns preamble gives the PHY time to detect a collision and report it.

UT_TXCLK and UT_RXCLK are asynchronous signals for a VDSL PHY. VDSL operates on its own time base. These clocks are only used as a means of communicating with the MAC. These clocks are tied to together and provided as a common input/output for MT2301.

The DSP can also control the RXD data bus via MII module register bits. This control allows the DSP to send the False Carrier Indication (UT_RXDV=0, UT_RXER=1, UT_RXD[0,3]=1110) to the external Ethernet MAC.

2.6.2 SMII Operation

The Serial Media Independent Interface (SMII) provides all functions equivalent to the MII interface without the overhead of the external wiring of the more parallel form of the interface. This section describes all the differences between SMII and MII interfaces for the signals, functionalities, and other specific information related to the SMII operation.

The data received from the Ethernet MAC on the TX interface is bit serial, eight bits of data and two status bits: TX_EN and TX_ER. Using TX_SYNC for frame alignment the SMII module converts the serial data (least significant bit first in time) to 10-bit parallel data. The TX_EN bit determines if a valid byte is currently available. The byte is valid if TX_EN is asserted even when TX_ER is also asserted. The framing logic passes valid bytes to the FIFO interface. When two SMII channels are used, the SYNC and CLK signals are used for both channels.

If TX_ER is asserted while TX_EN is also active the MAC is indicating that there is an error in the current Ethernet packet. The SMII module stores this error condition in the high bit of the next tag register. It can also generate an interrupt for this condition. The error is propagated into the current frame being sent. The second CRC byte (FCS in the encoder) is complemented to indicate an error frame. When the TX_EN bit is not active both TXD and TX_ER are ignored.

The valid byte stream process remains similar to the MII interface.

The RX path is largely the inverse of the TX. As with the MII module, the SMII module indicates the PHY has detected a data error in the idle status following an active frame. Status indicated by the eight data bits when the link is idle (RX_DV = 0):

RXD0 - RX_ER from previous frame

RXD1 - always 1 = 100 Mbps

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RXD2 - full-duplex operation programmable under software control

RXD3 - link active state of the interface (channel specific)

RXD4 - always 0 = jabber OK

RXD5 - always 1 = upper nibble valid

RXD6 - always 0 = false carrier not detected

RXD7 - always 1

The 125 MHz TX_CLK (for SMII) is supplied externally to prevent unusual amounts of clock skew. MT2301 uses a PLL to lock to the phase of this clock when generating the RX signals. The TX_CLK will be looped back to the interface as RX_CLK but with timing that matches the other RX signals. Optionally, MT2301 can generate the 125 Mhz RX_CLK using the PLL.

Received data and control information are signaled in ten bit segments. In 100 MBit mode, each segment represents a new byte of data. As defined in the 802.3 EFM standard, there is no 10 Mbit support.

2-6-4 Other Ethernet Related Operations

MT2301 also has support for two SMII (4 leads) or SSMII (6 leads) interfaces. The TC sub-layer uses a 65th sync byte for every 64 bytes transmitted to encapsulate the framed data but also supports HDLC encapsulation. The TC sub-layer also includes a G(x) = 1 + x^39 + x^58 scrambler/descrambler combination. Protocol is incorporated for mapping the following data types: idle, in-frame, idle->in-frame, in-frame->idle, in-frame->idle->in-frame. For packets containing data a 32-bit CRC is appended. After coding the byte stream is written to the input FIFO. This FIFO is located outside of the MII module.

The RX path is largely the inverse of the TX. Data is fetched from the output FIFO and passed through a decoder. Sync byte detection is performed in the receive path according to a well-defined state machine. The transmit path uses a 64-byte pipeline.

The serial control portion of the MII module implements the management data interface defined in the IEEE Std 802.3 specification. This interface supports dual standard clause 22 and clause 45 operations. Clause 22 is considered to be obsolete, but is included for backwards compatibility with older equipment. This standard defines a Management Data Input/Output (MDIO) interface between Station Management (STA) devices and the sub-layers that form the Physical Layer (PHY). The sub-layers are composed of individually manageable entities known as MDIO Manageable Devices (MMDs). The management data interface uses a data frame to transmit read or write commands to the PHY and to receive response data for reads. Control information is sent by STA in the initial portion of a management frame that determines the data transaction type to execute. The PHY can only return status or accept command as requested by the STA. Protocols must be defined to accomplish the reverse. Three fields control the type of transaction:

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OP - the op-code (refer to clause 22/45 for definition)

PRTAD (PHYAD) - the port address (or clause 22 physical address)

DEVAD (REGAD) - the device address (or clause 22 register address)

The MII block is equipped with a low-power gated clock mode. Setting the soft reset bit of the CSR will gate off the clock for the module and reset all logic. This capability is useful for reducing power consumption.

The MII interface uses two clocks: MDC and MII_CLK. The MDC clock is asynchronous to the system clock; however, its minimum period (400 ns) is much longer than the system clock (7ns). Therefore, the clock is sampled by the system clock for the purpose of capturing data on the MDIO lead and no MDC clock domain is needed.
The MII_CLK is 25 MHz and is also asynchronous to the system clock. Clause 22 specifies the synchronous RX signals be valid ±10 ns with respect to the rising edge of the RX clock. By clocking on the negative edge of a relatively square input clock we guarantee proper operation for clock frequencies up to 35 MHz. The MII_CLK is double delayed and differentiated for both positive and negative edge. Double delayed input data is captured on the positive edge. Output data is supplied on the negative edge. The module also includes a hard and soft reset. A CTL bit controls soft reset and doubles as the clock gating signal.

2.6.3 Quality of Service Feature

The following list defines the features of the QoS implementation in MT2301. These features allow the device to route packets between the two VDSL2 latency paths based on priority and to perform scheduling within each path. The QoS function can be applied to any Ethernet interface.

1. For TX, sort Ethernet packets into two latency paths based on the defined packet sorting mode. The packets within each latency path are also be queued based on priority.
2. For RX, Ethernet packets from two latency paths are combined before transmitting on MII. Priority queueing is not required in the RX path.
3. A maximum of four priority queues are supported for one Ethernet channel. Multiple Ethernet bearer channels are not supported when QoS is enabled
4. The QoS engine supports four mutually exclusive packet sorting modes:
    a. No sorting. All packets go to the default latency path.(disable QoS function)
    b. Sorting based on ethertype field of Ethernet headers. Up to 8 ethertype values can be specified. Each can be routed to either latency path and priority queue.
    c. Sorting based on VLAN ID range. Up to 8 VID/Netmask pairs can be defined. VIDs matching the range specified by each VID/Netmask pair can be routed to either latency path. Packets within a latency path can also be placed in a high or low priority queue can based on the VLAN priority field.
    d. Sorting based on VLAN priority field. Each of the 8 possible VLAN priority values can be routed to either latency path. Packets within a latency path can also be placed in a high or low priority queue based on the VLAN priority field.

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5. A configurable default latency path and queue is provided . Any packet that does not match one of the sorting filters will be sent to this path/queue. Also, in mode c., VLAN packets that do not match one of the VLAN ID filters can be dropped (configuration option) instead of being sent to the default latency path.
6. The Ethertype used for VLAN detection is configurable to support single and multi-tag (Q-in-Q) traffic.
7. Packets are routed based on the outer most VLAN tag. When multiple layers of VLAN are employed MT2301 will sort based on the outer layer and ignore the any inner layers.
8. Pause/Resume frame backpressure is normally used to avoid FIFO overflows. However, each queue can also be configured to drop packets before an overflow occurs. This mechanism allows low priority packets to be dropped without affecting high priority flows. The QoS logic maintains counters keep track of the number of dropped packets.

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2.7 Serial Port Interface

The Serial Port Interface (SPI) provides multiple ports that can be used for various purposes. One port will usually be used to control the external AFE while another may be used for EEPROM booting or some other purpose. The ports are all full-duplex serial ports with a lot of flexibility in their programming for communicating with a variety of serial devices.

All Serial Ports include comprise independent transmitter and receiver sections and a common serial clock generator.

2.7.1 Serial Port Rates

The Serial Port interface maximum communication rate is 1/4 of the master clock. Since MT2301 can operate up to 150 MHz, the maximum serial rate is 37.5Mbit per second. All Serial Port Interfaces need four system clocks to operate on a single bit of data. When the serial port is the clock master, The minimum data rate is equal to the DSP clock frequency divided by 4096.Therefore, 36.6Kbit per second is the minimum speed for clock master mode with a 150 MHz DSP clock

2.7.2 Serial Port Operation

Words transferred by the SCI are characterized by word length, shift direction, and word alignment. This section describes these characteristics and the programming associated with them.

2.7.3 Word Length

The Serial Port provides full control of the number of bits per word or the word length. The SCI transmit and receive data registers are 24-bits long, so 32-bits words cannot be transmitted or received. For 32-bit words, the first 24 bits contain valid data and the last bits are not defined.

2.7.4 Shift Direction

The Serial Port presents two options for shift direction: most significant bit (MSB) first or least significant bit (LSB) first. To select shift direction, set bit 6 in Control Register B, SHFD. If SHFD is set, the data is shifted into the receive shift register from the SRD lead and out of the transmit shift register to the STD lead with the LSB first. If SHFD is clear, the data is shifted into the receive shift register from the SRD lead and out of the transmit shift register to the STD lead with the MSB first.

2.7.5 Synchronization Signals

Because the Serial Port is a synchronous interface, it requires clock and frame sync signals to define when the data changes and when a new frame begins. In certain modes, the Serial Port also has the option of two flag signals to use for device selection.

2.7.6 Synchronous versus Asynchronous

The Serial Port includes both synchronous and asynchronous modes. In synchronous mode, the transmitters and receiver use the same clock and frame sync; in asynchronous mode, the transmitters and receiver use different clocks and frame syncs. The Serial Port data transfers are synchronized to a clock in both modes. The choice of synchronous versus asynchronous mode is determined by API command. Setting SYN puts the Serial Port is in synchronous mode; clearing SYN puts it in asynchronous mode.

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In synchronous mode: SCK is an input or an output that both the transmitter and receiver use as the clock signal. SC2 is an input or an output that both the transmitter and receiver use as the frame sync signal. SC0 and SC1 can be used as flag signals.

2.7.7 In Asynchronous Mode

SCK is an input or an output that the transmitter uses as the clock signal.

SC2 is an input or an output that the transmitter uses as the frame sync signal.

SC0 is an input or an output that the receiver uses as the clock signal.

SC1 is an input or an output that the receiver uses as the frame sync signal.

The direction of the SC0, SC1, SC2, and SCK leads is determined by the SCD0, SCD1, SCD2, and SCKD bits, respectively, CRB [3:0]. If one of these bits is clear, the corresponding lead is an input. If one of these bits is set, the corresponding lead is an output.

2.7.8 Serial Clock

SCK's direction can be controlled via API command.

2.7.9 Frame Sync

The frame sync signal indicates when a new frame begins. In synchronous mode, the SC2 lead is the frame sync for the receiver and transmitter. In asynchronous mode, SC2 is the frame sync signal for the receiver and SC0 is the frame sync signal for transmitter 0.

Frame sync is generated only when data is ready to be transmitted, i.e., data is written to a transmit data register. This mode requires that the transmit frame sync be internal (output) and the receive frame sync be external (input) for proper operation. Transmit under-runs are impossible in on-demand mode because there are no transmit time slots, thus they are disabled.

2.7.10 Flags

When the Serial Port is in synchronous mode, the SC0 and SC1 leads are available for use as flags.

2.7.11 SPI Protocol: Clock Stop Mode

A system conforming to this protocol has a master-slave configuration. SPI protocol is a 4-wire interface composed of serial data in (master in slave out), serial data out (master out slave in), shift clock (SCK), and an active (low) slave enable signal. Communication between the master and the slave is determined by the presence or absence of the master clock. Data transfer is initiated by the detection of the master clock and is terminated on absence of the master clock. The slave has to be enabled during this period of transfer. When the SPI is the master, the slave enable is derived from the master transmit frame sync pulse, SC2.

The clock stop mode of the Serial Port provides compatibility with the SPI protocol. The SPI supports two SPI transfer formats specified by the clock stop mode field (CKST) in Control Register B. The clock stop

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mode in conjunction with the CKP bit allows serial clocks to be stopped between transfers using one of four possible timing variations.

2.7.12 SPI Protocol: Start Bit Mode

Some devices require a start bit to indicate the arrival of a data frame. When configured in this mode (SBIT = 1 in Control Register B) an active low start bit precedes the data followed by an active high stop bit. No frame sync is required since the receiving device frames the data. The word length control (WL [4:0]) is adjusted to specify the number of bits.

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2.8 Host Port Interface

The host port interface (HPI) is an eight/sixteen bit parallel interface. It supports both master and slave mode operation and provides a DMA interface to the DSP memory for block transfers of up to 512 bytes. The HPI can interface with most of the Microprocessor and DSP available on the market with no external components

MT2301 employs a message interface API for command and response. The command and response message format uses HDLC-like framing, similar to the one used in G.997.1. Each command is followed by an acknowledge response typically within 1 ms. If a command is not acknowledged within 10 ms the command can be assumed to be not understood or some other error condition preventing the command can be assumed. Some commands will be acknowledged and then will be followed by a status frame sent from MT2301 to the host at a later time.

2.9 Boundary Scan (JTAG) Operation

When boundary scan testing is not being performed, the boundary scan register is transparent, allowing the input and output signals at the device leads to pass to and from the device's internal logic. During boundary scan testing, the boundary scan register disables the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. Data is read out from internal test registers LSB first.

The following boundary scan test instructions are supported

-SAMPLE/PRELOAD
-BYPASS
-IDCODE
-EXTEST

EXTEST Test Instruction: One of the required boundary scan tests is the external boundary test (EXTEST) instruction. When this instruction is shifted in, the device is forced into an off-line test mode. While in this test mode, the test bus can shift data through the boundary scan registers to control the external input and output leads. The MT3201 is NOT held in Reset.

SAMPLE/PRELOAD Test Instruction: When the SAMPLE/PRELOAD instruction is shifted in, the device remains fully operational. While in this test mode, input data, and data destined for device outputs, can be captured and shifted out for inspection. The data is captured in response to control signals sent to the TAP controller.

BYPASS Test Instruction: There is no explicit decode for bypass instruction. It is always selected by default. Thus any invalid instruction opcode will map to the bypass instruction. When the BYPASS instruction is shifted in, the device remains fully operational. While in this test mode, a scan operation will transfer serial data from the TDI input, through an internal scan cell, to the TDO lead. The purpose of this instruction is to abbreviate the scan path through the circuits that are not being tested to only a single clock delay.

IDCODE Instruction: When the IDCODE instruction is shifted in, the device remains fully operational. The purpose of this instruction is to output the device ID code register on the TDO lead.

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3 Pin Description

3.1 LQFP 128 Pin Description

Pin	Symbol	Pad Type	Description
1	STXCLK	I	SMII TX CLK
2	STXSYNC	I	SMII TX SYNC
3	STXDAT_D1	I	SMII Tx data 1
4	STXDAT_D0	I	SMII Tx data 0
5	MII_CRS	O	MII carrier sense
6	MII_COL	O	MII collision
7	GMII/RGMII/MII_RXD3	O	MII/GMII/RGMII receive data 3
8	GMII/RGMII/MII_RXD2	O	MII/GMII/RGMII receive data 2
9	GMII/RGMII/MII_RXD1	O	MII/GMII/RGMII receive data 1
10	GMII/RGMII/MII_RXD0	O	MII/GMII/RGMII receive data 0
11	GMII/RGMII/MII_RXDV	I/O	MII RX data valid (O)
12	GMII/RGMII/MII_RXCLK	I/O	MII RX clock (I)/GMII RX clock (O)
13	GMII/MII_RXER	O	MII RX error
14	GMII/MII_TXER	I	MII TX error
15	GMII/RGMII/MII_TXCLK	I/O	MII TX clock (O)/GMII TX clock (I)
16	GMII/RGMII/MII_TXEN	I	MII transmit enable
17	VDDPST	VDD I/O	VDD digital I/O supply
18	VSSPST	VSS I/O	VSS digital I/O supply
19	GMII/RGMII/MII_TXD0	I	MII/GMII/RGMII transmit data 0
20	GMII/RGMII/MII_TXD1	I	MII/GMII/RGMII transmit data 1
21	VDD	VDD core	VDD digital core supply
22	VSS	VSS core	VSS digital core supply
23	GMII/RGMII/MII_TXD2	I	MII/GMII/RGMII transmit data 2
24	VDD	VDD core	VDD digital core supply
25	VSS	VSS core	VSS digital core supply
26	GMII/RGMII/MII_TXD3	I	MII/GMII/RGMII transmit data 2
27	VDDPST	VDD I/O	VDD digital I/O supply
28	VSSPST	VSS I/O	VSS digital I/O supply
29	SRXDAT0/GMII_TXD4	O	SMII RX data 0/GMII_TXD4
30	SRXDAT1/GMII_TXD5	O	SMII RX data 1/GMII_TXD5
31	SRXCLK/GMII_TXD6	O	SMII Rx CLK/GMII_TXD6
32	SRXSYNC/GMII_TXD7	O	SMII Rx SYNC/GMII_TXD7
33	MDC	I	MDC
34	MDIO	I/O	MDIO
35	VCCOSC(3.3V)	VCC OSC	OSC 3.3v supply
36	XTALI	I	Master crystal oscillator input
37	XTALO	O	Master crystal oscillator output

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Pin	Symbol	Pad Type	Description
38	VSSOSC	VSS OSC	OSC supply
39	STDA	O	SPI serial port A transmit data/GPIO(Output only)
40	SRDA	I	SPI serial port A receive data/GPIO(Input only)
41	SCKA	I/O	SPI serial port A clock/GPIO
42	TESTMODE	I	For internal use only/ Tie to ground
43	NMI	I	Non-maskable interrupt/PLL bypass lead strap
44	VDD	VDD core	VDD digital core supply
45	VSS	VSS core	VSS digital core supply
46	ARXD2	I	AFE interface receive data 2
47	VDDPST	VDD I/O	VDD digital I/O supply
48	VSSPST	VSS I/O	VSS digital I/O supply
49	ARXD3	I	AFE interface receive data 3
50	ARXD4	I	AFE interface receive data 4
51	ARXD5	I	AFE interface receive data 5
52	ARXD6	I	AFE interface receive data 6
53	VDD	VDD core	VDD digital core supply
54	VSS	VSS core	VSS digital core supply
55	ARXD7	I	AFE interface receive data 7
56	ARXD8	I	AFE interface receive data 8
57	ACK0	I	AFE interface clock 0
58	ARXD9	I	AFE interface receive data 9
59	ARXD10	I	AFE interface receive data 10
60	ARXD11	I	AFE interface receive data 11
61	ARXD12	I	AFE interface receive data 12
62	ARXD13	I	AFE interface receive data 13
63	ARXD14	I	AFE interface receive data 14
64	ARXD15	I	AFE interface receive data 15
65	ATXD15	O	AFE interface transmit data 15
66	ATXD14	O	AFE interface transmit data 14
67	ATXD13	O	AFE interface transmit data 13
68	ATXD12	O	AFE interface transmit data 12
69	ATXD11	O	AFE interface transmit data 11
70	ATXD10	O	AFE interface transmit data 10
71	ATXD9	O	AFE interface transmit data 9
72	ATXD8	O	AFE interface transmit data 8
73	ATXD7	O	AFE interface transmit data 7
74	ATXD6	O	AFE interface transmit data 6
75	ATXD5	O	AFE interface transmit data 5
76	ATXD4	O	AFE interface transmit data 4
77	VSS	VSS core	VSS digital core supply

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Pin	Symbol	Pad Type	Description
78	VDD	VDD core	VDD digital core supply
79	ATXD3	O	AFE interface transmit data 3
80	ATXD2	O	AFE interface transmit data 2
81	SCKB	I/O	SPI serial port B clock
82	STDB	O	SPI serial port B transmit data/GPIO(Output only)
83	SRDB	I	SPI serial port B receive data/GPIO(Input only)
84	SC2B	I/O	SPI serial port B control 2/GPIO
85	VSSPST	VSS I/O	VSS IO supply
86	VDDPST	VDD I/O	VDDD IO supply
87	TMS	IPU	ONCE/JTAG test mode select
88	DEN	I	ONCE/JTAG debug enable
89	TDI	I	ONCE/JTAG serial test data in
90	VSS	VSS core	VSS Digital core supply
91	VDD	VDD core	VDD Digital core supply
92	TDO	O	ONCE/JTAG serial test data out
93	TCK	I	ONCE/JTAG test clock
94	TRSTN	IPU	ONCE/JTAG reset
95	EX_A11/GPIO0	I/O	Ext memory address 11/GPIO
96	EX_A16/GPIO1	I/O	Ext memory address 16/GPIO
97	VCCPLL1	VCC PLL1	1.2v VCC supply for PLL1
98	VSSPLL1	VSS PLL2	VSS for PLL1
99	EX_A17/GPIO2	I/O	Ext memory address 17/GPIO
100	EX_AA0	I/O	Ext memory address attribute 0/GPIO
101	EX_AA1	I/O	Ext memory address attribute 1/GPIO
102	EX_AA2	I/O	Ext memory address attribute 2/GPIO
103	EX_AA3	I/O	Ext memory address attribute 3/GPIO
104	RESET	I	System reset signal, active low
105	VSS	VSS core	VSS Digital core supply
106	VDD	VDD core	VDD Digital core supply
107	HP_DY	I/O	Host port slave ready
108	HP_CS	I/O	Host port chip select
109	HP_RDWRn	I/O	Host port read/write#
110	HP_DS	I/O	Host port data strobe
111	EX_D0/8	I/O	Ext memory data 8/Host port data 0/GPIO
112	EX_D1/9	I/O	Ext memory data 9/Host port data 1/GPIO
113	EX_D2/10	I/O	Ext memory data 10/Host port data 2/GPIO
114	VSSPST	VSS I/O	VSS IO Supply
115	VDDPST	VDD I/O	VDD IO Supply
116	EX_D3/11	I/O	Ext memory data 11/Host port data 3/GPIO
117	EX_D4/12	I/O	Ext memory data 12/Host port data 4/GPIO

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Pin	Symbol	Pad Type	Description
118	EX_D5/13	I/O	Ext memory data 13/Host port data 5/GPIO
119	VSS	VSS core	VSS digital core supply
120	VDD	VDD core	VDD digital core supply
121	EX_D6/14	I/O	Ext memory data 14/Host port data 6/GPIO
122	EX_D7/15	I/O	Ext memory data 15/Host port data 7/GPIO
123	IRQA	I	External interrupt A/Test mode 0 lead strap
124	IRQB	I	External interrupt B/Test mode 1 lead strap
125	IRQC	I	External interrupt C/Test mode 2 lead strap
126	IRQD	I	External interrupt D/Test mode 3 lead strap
127	VCCPLL2	VCC PLL2	1.2v VCC supply for PLL2
128	VSSPLL2	VSS PLL2	VSS supply for PLL2

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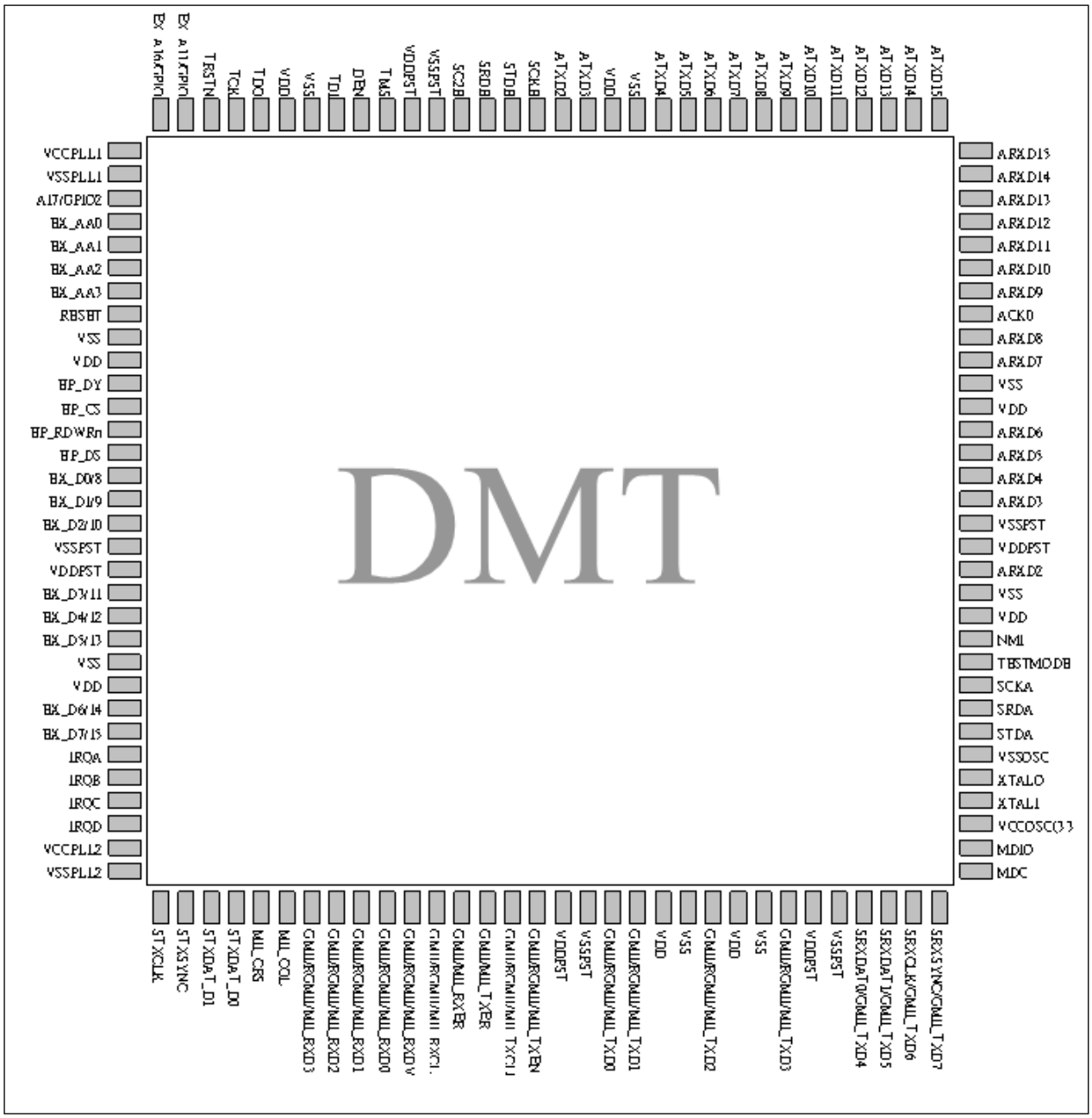

Figure 7 Pin Diagrams

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4 Technical Characteristics

4.1 Absolute Maximum Ratings and Environmental Limitations

(REFERENCED to VSS)

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage (CMOS I/O)	$VDD_{IO/PLL}$	-0.3	3.9	V	Note 1,4
Supply voltage (Core)	VDD_{CORE}	-0.3	1.32	V	Note 1,4
DC input voltage	V_{IN}	-0.5	5.5	V	Note 1,4,5
Storage temperature range	T_S	-55	+150	℃	Note 1
Ambient operating	T_A	-40	+85	℃	0 ft/min linear airflow
Temperature	ME	5		Level	Per IPC/JEDEC
Moisture exposure level	RH	30	60	%	Note 2
Relative humidity, during assembly	RH	0	100	%	Non-condensing
ESD classification	ESD	2		kV	Note 3

Notes：

1. Operating conditions outside the min-max ranges specified may cause permanent device failure. Exposure to conditions near the min or max limits for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per JEDEC JESD22-A114-B.
4. Device core is 1.2V only.
5. MT2301 is 5 V compatible in the sense that the output logic 1 (VOH) and output logic 0 (VOL) levels of the MT2301 outputs have been specified at the same voltage levels that have been commonly recognized as logic 1 and logic 0 for the 5 V environment. MT2301 can generally be expected to drive 5 V TTL compatible components. However, while MT2301 outputs are able to meet the minimum input logic switching levels (VIH and VIL) of 5 V TTL compatible components, the output logic 1 output voltage of some 5 V components may exceed the maximum input voltage of MT2301. Depending on the technology and circuit implementation, the 5 V TTL compatible components may drive their outputs anywhere from 3 V to their VDD supply level. CAUTION: Before connecting a 5 V component to the MT2301, always check to be sure that the Maximum VOH of the 5 V device does not exceed the specified Maximum VIN listed in the table above.

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4.2 Thermal Characteristics

Parameter	Min	Typ	Max	Unit	Conditions
Thermal resistance-junction to ambient		18		℃/W	0 ft/min linear airflow

4.3 Power Requirements

Parameter	Min	Typ	Max	Unit	Conditions
V_{DDIO}	2.67	3.3	3.96	V	
I_{DDIO}	20			mA	See Notes 1and 2
P_{DDIO}	53.4			mW	See Notes 1and 2
V_{DDPLL}	3.15	3.3	3.45	V	
I_{DDPLL}	1	1	1	mA	See Notes 1and 2
P_{DDPLL}	3.2	3.3	3.5	mW	See Notes 1and 2
V_{DDCORE}	1.12	1.2	1.31	V	
I_{DDCORE}	320	320	335	mA	See Notes1and 2
P_{DDCORE}	358.4	384.0	438.9	mW	See Notes 1and 2
Total Power	450	450	550	mW	See Notes 1 and 2

Notes：

1. Typical values estimated with nominal voltages at 25° C.

2. All IDD and PDD values are dependent upon VDD.

4.4 Input, Output and Input/Output Parameters

4.4.1 Input Parameters For LVTTL

Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	2.0			V	$3.14 \leqq V_{DD33} \leqq 3.46$
V_{IL}			0.8	V	$3.14 \leqq V_{DD33} \leqq 3.46$
Input leakage current	-10		10	μA	$V_{IN}= V_{DD33}$ or V_{SS}
Input capacitance		5		pF	

4.4.2 Input Parameters For LVTTLpu (internal pull-up resistor)

Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	2.0			V	$3.14 \leqq V_{DD33} \leqq 3.46$
V_{IL}			0.8	V	$3.14 \leqq V_{DD33} \leqq 3.46$
Input leakage current	-10		10	μA	$V_{IN}= V_{DD33}$ or V_{SS}
Input capacitance		5		pF	

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4.4.3 Output Parameters For CMOS 16mA

Parameter	Min	Typ	Max	Unit	Conditions
V_{OH}	2.4			V	1_{OH}=-16mA
V_{OL}		0.2	0.4	V	1_{OL}=16mA
I_{OL}			16.0	mA	
I_{OH}			-16.0	mA	
Leakage tristate	-10		10	µA	

4.4.4 Input/Output Parameters For LVTTL/CMOS 16mA

Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	2.0			V	$3.14 \leqq V_{DD33} \leqq 3.46$
V_{IL}			0.8	V	$3.14 \leqq V_{DD33} \leqq 3.46$
Input leakage current	-10		10	µA	V_{DD33}=3.46
Input capacitance		5		pF	
V_{OH}	2.4			V	1_{OH}=-16mA
V_{OL}		0.2	0.4	V	1_{OL}=16mA
I_{OL}			16.0	mA	
I_{OH}			-16.0	mA	

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4.5 Timing Characteristics

This section presents the detailed timing characteristics for the MT2301 in Figure 11 through Figure 22 with values of the timing parameters tabulated below each waveform diagram. Detailed timing diagrams for the MT2301 device are provided in this section, with values for the timing intervals given in tables below the waveform drawings. All output times are measured with a 25 pF load capacitance for Max conditions and 5 pF load capacitance for Min conditions, unless noted otherwise. Timing parameters are measured at voltage levels of (VIH+VIL)/2 and (VOH+VOL)/2, for input and output signals, respectively. All input transition times, 10/90%, used for timing measurements are 1.0 ns for Max conditions and 0.2 ns for Min conditions.

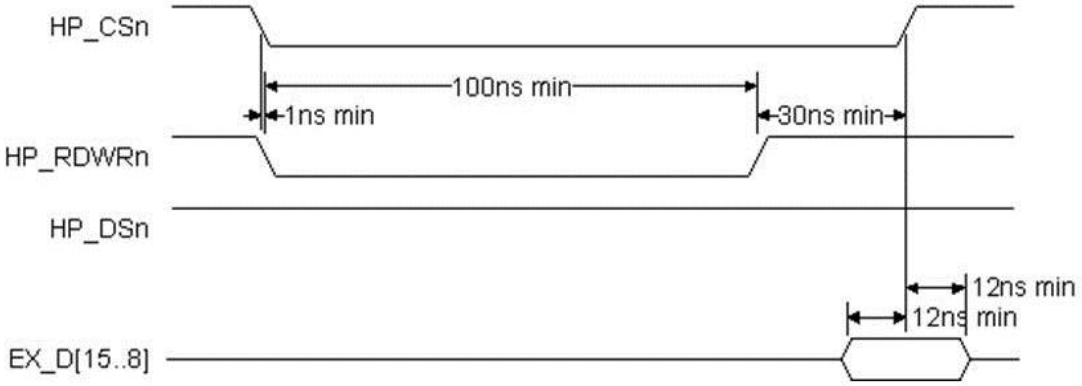

Figure 8 Host Port Read Cycle Timing

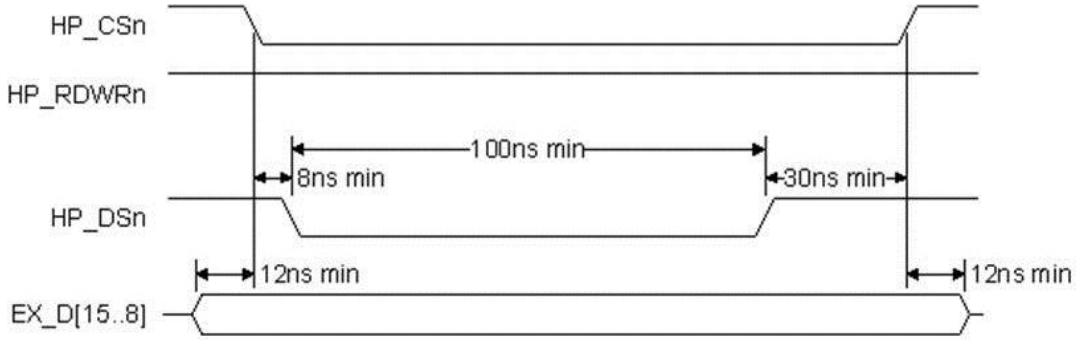

Figure 9 Host Port Write Cycle Timing

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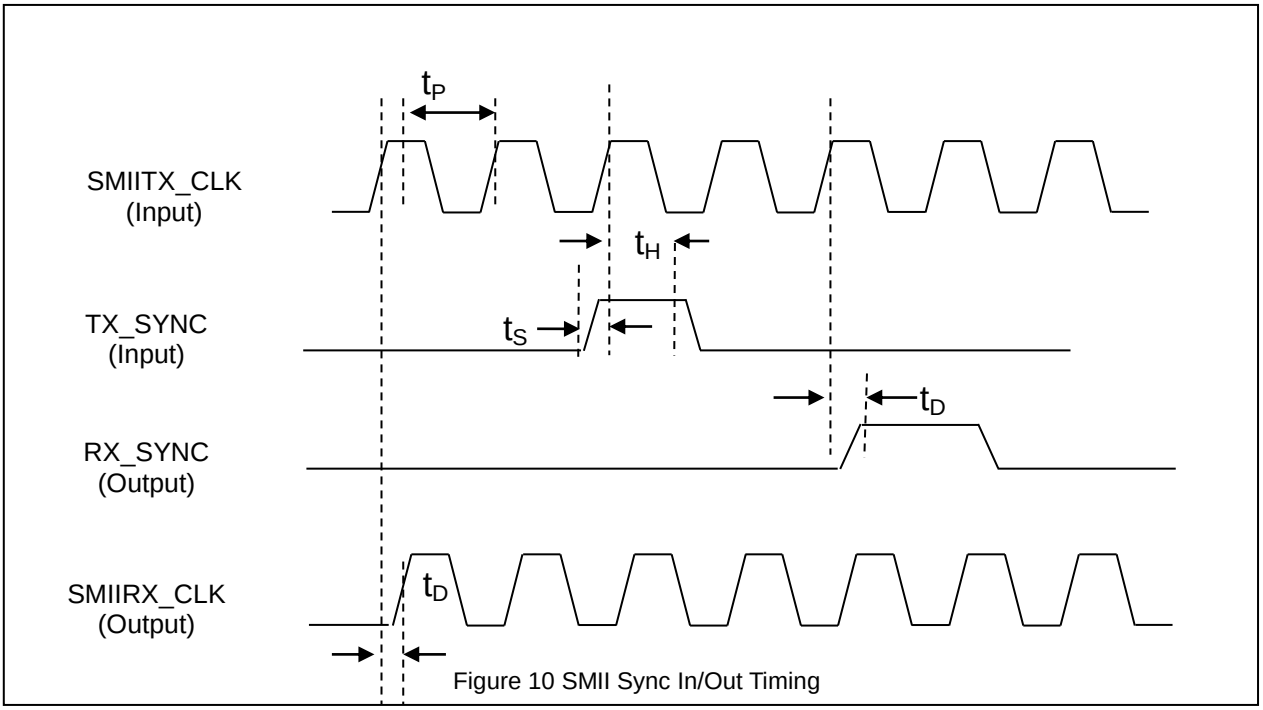

Figure 10 SMII Sync In/Out Timing

Parameter	Symbol	Min	Typ	Max	Unit
SMIITX_CLK and SMIIRX_CLK period	t_P		8.0		ns
SMIITX_CLK and SMIIRX_CLK duty cycle		40		60	%
TX_SYNC setup time to SMIITX_CLK↑	t_S	1.5			ns
TX_SYNC hold time from SMIITX_CLK↑	t_H	1.0			ns
RX_SYNC/SMIIRX_CLK delay from SMIITX_CLK↑	t_D	1.5		4.5	ns

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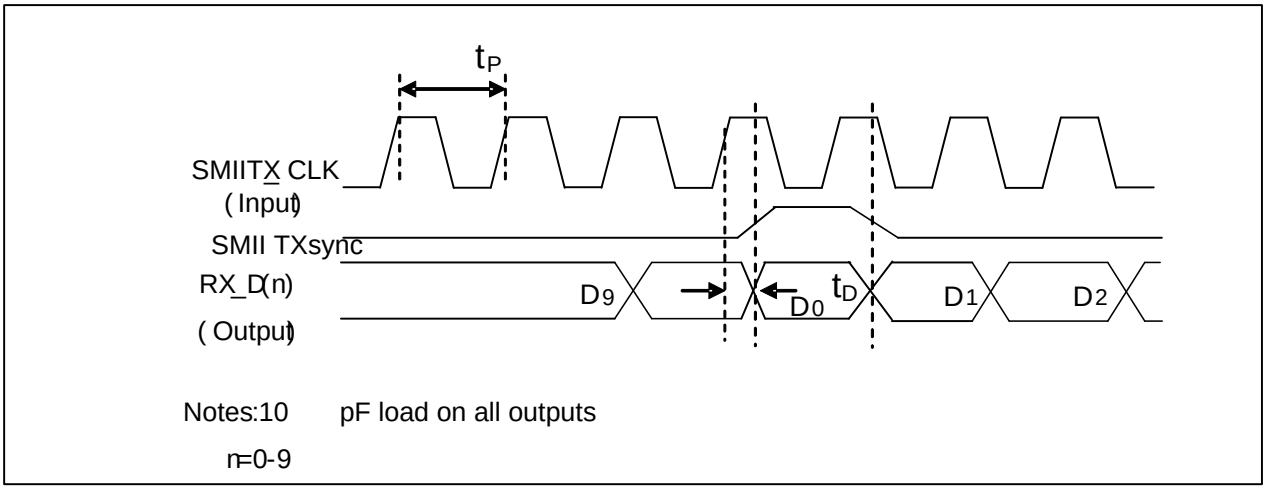

Figure 11 SMII Receive Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
RX_D(n) delay from SMIITX_CLK↑	t_D	1.5		4.5	ns

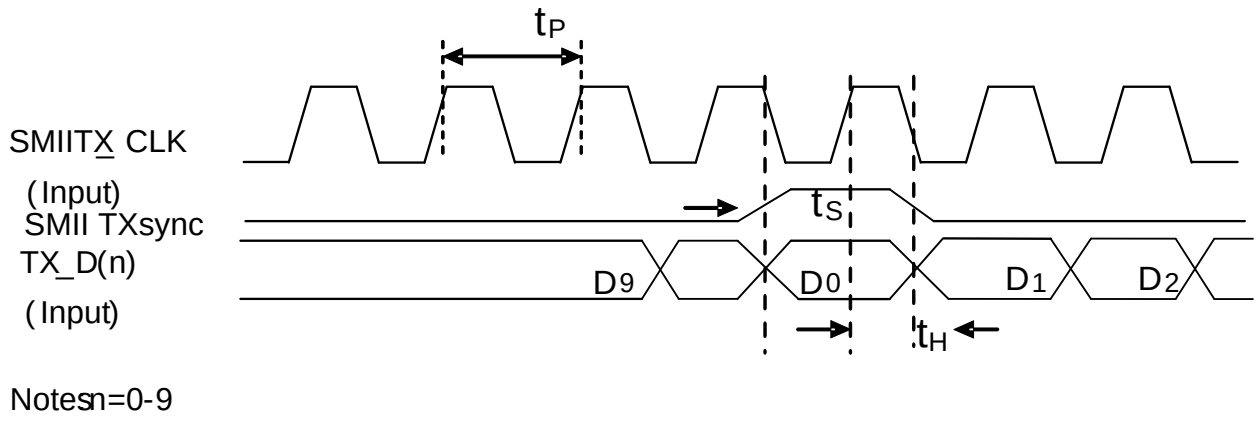

Figure 12 SMII Transmit Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
TX(n) setup to SMIITX_CLK↑	t_S	1.5			ns
TX(n) hold from SMIITX_CLK↑	t_H	1.0			ns

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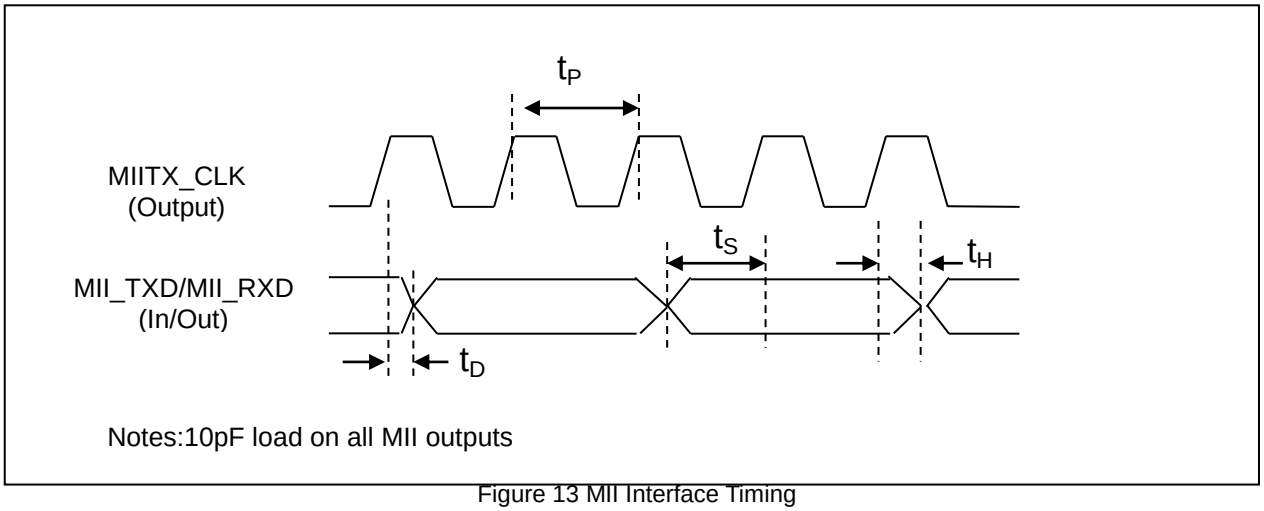

Figure 13 MII Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
MII_CLK frequency	$1/t_P$	16.66		25	MHz
MII_CLK duty cycle	t_P	40		60	ns
MII_TXD/MII_RXD delay from MII_CLK↑	t_D	10		100	ns
MII_TXD/MII_RXD setup to MII_CLK↑	t_S	15			ns
MII_TXD/MII_RXD hold from MII_CLK↑	t_H	0.0			ns

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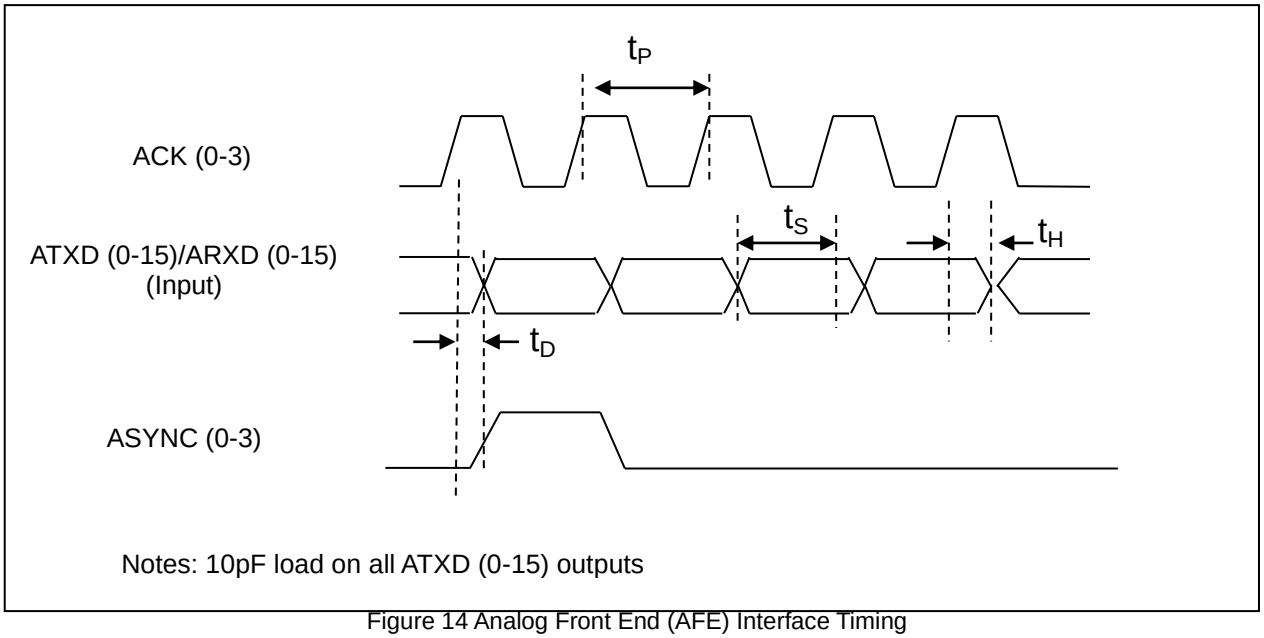

Figure 14 Analog Front End (AFE) Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
ACCLK(0-3) frequency	$1/t_P$		35.328		MHz
ACCLK(0-3) duty cycle	t_P		28.03		ns
ATXD(0-15)/ARXD(0-15) delay from ACLK↑	t_D	10		100	ns
ATXD(0-15)/ARXD(0-15) setup to ACLK↑	t_S	15			ns
ATXD(0-15)/ARXD(0-15) hold from ACLK↑	t_H	0.0			ns

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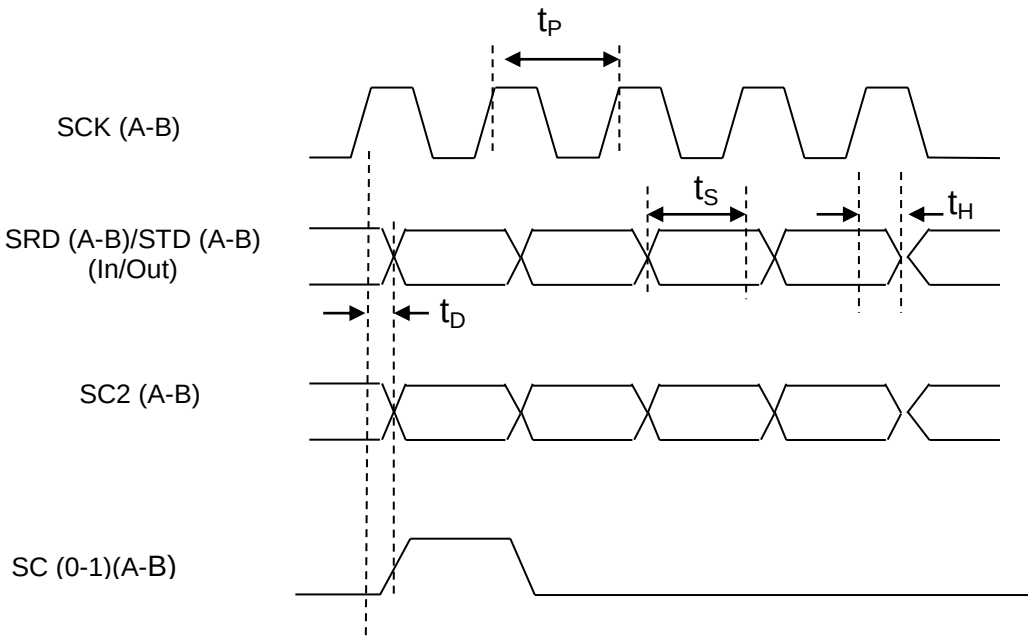

Notes: 10pF load on all STD (A-B) outputs

Figure 15 Serial Port A-B Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
SCK(A-B) frequency	$1/t_P$	0.036		37.5	MHz
SCK(A-B) duty cycle	t_P	30		30000	ns
SRD(A-B)/STD(A-B) delay from SCK↑	t_D	10		100	ns
SRD(A-B)/STD(A-B) setup to SCK↑	t_S	15			ns
SRD(A-B)/STD(A-B) hold from SCK↑	t_H	0.0			ns
SC(0-2)(A-B) delay from SCK↑	t_D	10		100	ns

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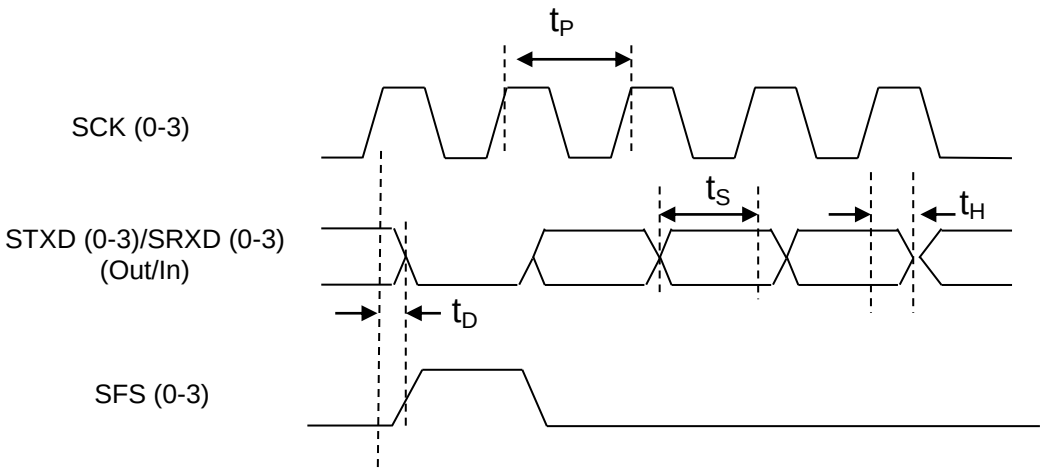

Notes: 10pF load on all STD (0-3) outputs

Figure 16 Serial Port 0-3 Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
SCK(0-3) frequency	$1/t_P$	27		33.3	MHz
SCK(0-3) duty cycle	t_P	30		35	ns
STXD(0-15)/SRXD(0-15) delay from SCK↑	t_D	10		100	ns
STXD(0-15)/SRXD(0-15) setup to SCK↑	t_S	15			ns
STXD(0-15)/SRXD(0-15) hold from SCK↑	t_H	0.0			ns

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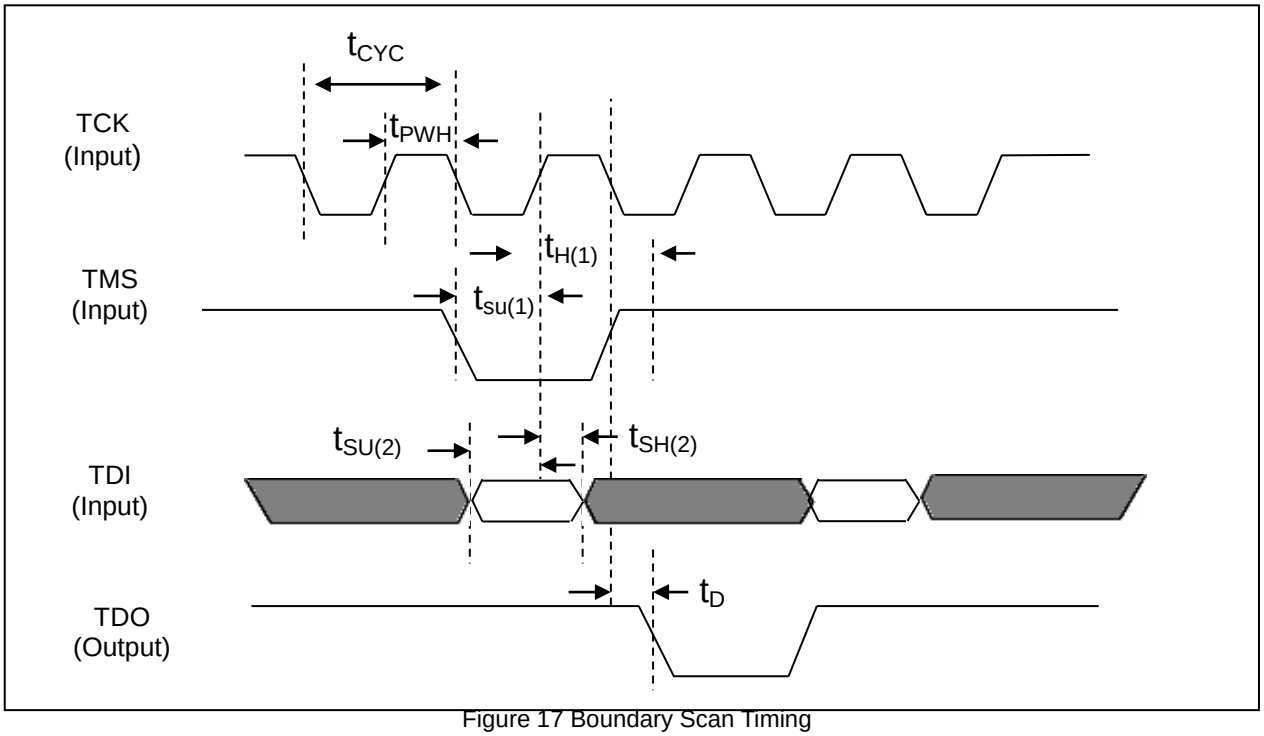

Figure 17 Boundary Scan Timing

Parameter	Symbol	Min	Max	Unit
TCK clock cycle time	t_{CYC}	50		ns
TCK clock duty cycle	t_{PWH}/ t_{CYC}	40	60	%
TMS setup time before TCK↑	$t_{SU(1)}$	4.0		ns
TMS hold time after TCK↑	$t_{H(1)}$	1.0		ns
TDI setup time before TCK↑	$t_{SU(2)}$	6.0		ns
TDI hold time after TCK↑	$t_{H(2)}$	1.0		ns
TDO delay after TCK↑	t_D		15.0	ns

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5 Package Information

The MT2301 device is packaged in a 14mm×14mm (3.20 mm), 128-lead thin-profile quad flat package (LQFP) suitable for surface mounting, as shown in Figure 17

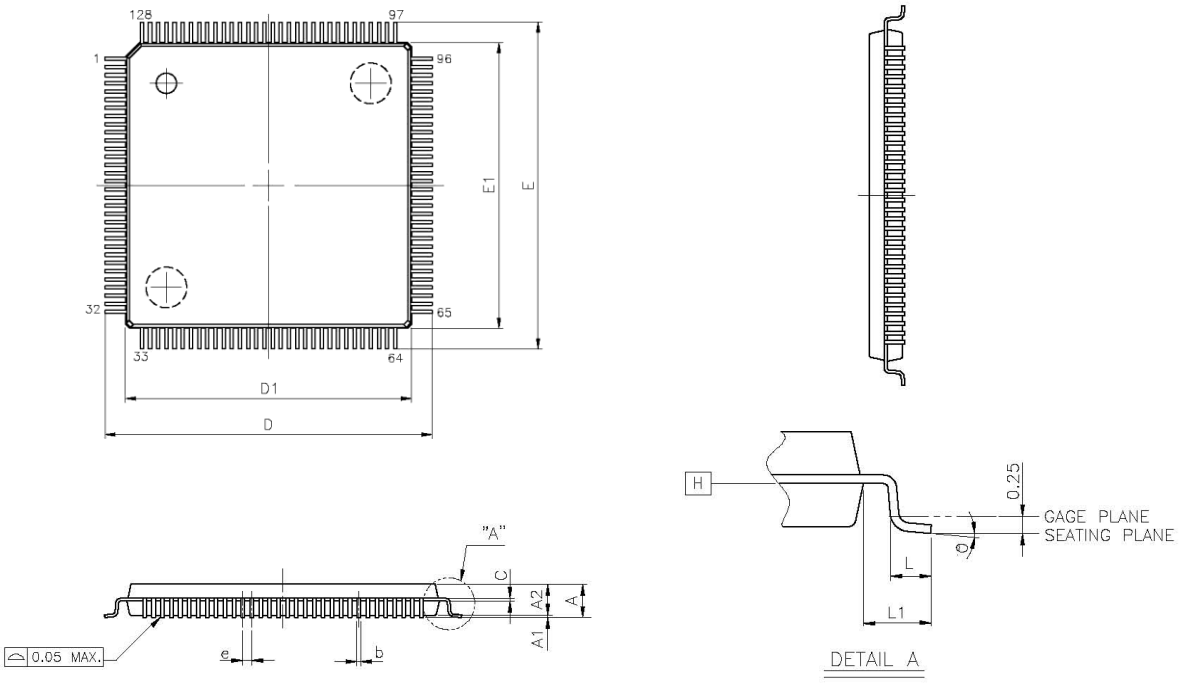

Figure 18 MT2301 LQFP Package Diagram

VARIATIONS (ALL DEMINSIONS SHOW IN MM)

SYMBOLS	Min	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.13	0.16	0.23
c	0.09	--	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Notes:

1. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

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6 Ordering Information

Prefix	Part No. (4 numbers)	Package		-	Version
		RoHS or Not	Package Type		
MT	2301	G: **Green Product** N: **Pb Product**	N: **QFN** P:**QFP** L: **LQFP** C:**CHIP** B:**BGA**	-	A1

Part Number

- MT2301GL-A1: 1 port VDSL2 DMT chip with 128-LQFP package.

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