

LISA-U2 series

3.75G HSPA+ Wireless Modules

Data Sheet

Abstract

Technical data sheet describing LISA-U2 series HSPA+ wireless modules.

These modules are a complete and cost efficient 3.75G solution offering up to six-band high-speed HSPA+ and quad-band GSM/EGPRS voice and/or data transmission technology in a compact form factor.



33.2 x 22.4 x 2.6 mm

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Document status information	
Objective Specification	This document contains target values. Revised and supplementary data will be published later.
Advance Information	This document contains data based on early testing. Revised and supplementary data will be published later.
Preliminary	This document contains data from product verification. Revised and supplementary data may be published later.
Released	This document contains the final product specification.

This document applies to the following products:

Name	Type number	Firmware version	PCN / IN
LISA-U200	LISA-U200-00S-00	21.21	UBX-TN-12009
	LISA-U200-01S-00	22.40	UBX-TN-12040
LISA-U230	LISA-U230-01S-00	22.40	UBX-TN-12040
LISA-U260	LISA-U260-01S-00	22.61	UBX-TN-12061
LISA-U270	LISA-U270-01S-00	22.61	UBX-TN-12061

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Contents

Contents.....	3
1 Functional description.....	5
1.1 Overview	5
1.2 Product features	5
1.3 Block diagram.....	6
1.4 Product description.....	7
1.5 AT command support.....	8
1.6 Supported features	9
2 Interfaces	11
2.1 Power Management	11
2.1.1 Module supply (VCC)	11
2.1.2 RTC supply (V_BCKP).....	11
2.1.3 Digital I/O interfaces supply (V_INT)	11
2.2 RF antenna interface.....	11
2.3 System functions	11
2.3.1 Module power-on	11
2.3.2 Module power-off.....	12
2.3.3 Module reset	12
2.4 (U)SIM interface.....	12
2.5 Serial communication	13
2.5.1 Asynchronous serial interface (UART).....	13
2.5.2 Universal Serial Bus (USB)	14
2.5.3 Serial Peripheral Interface (SPI).....	15
2.5.4 Multiplexer protocol	15
2.6 DDC (I ² C) bus interface	15
2.7 Audio	16
2.8 GPIO.....	16
3 Pin definition	18
3.1 Pin assignment	18
4 Electrical specifications	24
4.1 Absolute maximum rating	24
4.1.1 Maximum ESD.....	25
4.2 Operating conditions	26
4.2.1 Operating temperature range.....	26
4.2.2 Module thermal resistance	26
4.2.3 Supply/Power pins	27
4.2.4 Power consumption	28

4.2.5	RF Performance	29
4.2.6	PWR_ON pin	31
4.2.7	RESET_N pin	31
4.2.8	(U)SIM pins	31
4.2.9	Generic Digital Interfaces pins	32
4.2.10	USB pins	44
4.2.11	DDC (I ² C) pins	44
5	Mechanical specifications	45
6	Reliability tests and approvals	46
6.1	Reliability tests	46
6.2	Approvals	46
7	Product handling & soldering	47
7.1	Packaging	47
7.1.1	Reels	47
7.1.2	Tapes	48
7.2	Moisture Sensitivity Levels	49
7.3	Reflow soldering	49
7.4	ESD precautions	49
8	Default settings	50
9	Labeling and ordering information	51
9.1	Product labeling	51
9.2	Explanation of codes	51
9.3	Ordering information	52
	Appendix	53
A	Glossary	53
	Related documents	54
	Revision history	55
	Contact	56

1 Functional description

1.1 Overview

LISA-U2 modules are a 3.75G solution providing up to six-band HSPA+ and quad-band GSM/EDGE data transmission in a compact form factor. These modules feature low power consumption and HSUPA category 6, HSDPA up to category 14, GPRS/EDGE up to class 33 data transmission with voice capability. They also combine baseband, RF transceiver, power management unit, and power amplifier in a single, easy-to-integrate solution.

LISA-U2 modules are complete, fully qualified and certified solutions, which reduces cost and enables short time to market. They are ideally suited to M2M and automotive applications such as: mobile Internet terminals and applications, car infotainment and telematics, Automatic Meter Reading (AMR), Remote Monitoring Automation and Control (RMAC), surveillance and security, road pricing, asset tracking, fleet management, anti theft systems, and Point of Sales (PoS) terminals.

LISA-U2 modules support full access to u-blox GPS/GNSS receivers via serial port. Thus WCDMA/GSM and GPS/GNSS can be controlled through a single serial port from any host processor. The compact LISA form factor and SMT pads allow fully automated assembly with standard pick & place and reflow soldering equipment for cost-efficient, high-volume production.

1.2 Product features

Module	Technology		Bands		Interface					Audio		Functions										
	HSUPA [Mb/s]	HSDPA [Mb/s]	UMTS/HSPA bands [MHz]	GSM/GPRS/EDGE quad-band	UART	SPI (5 wires)	USB	DDC for u-blox GPS/GNSS	GPIO	Analog Audio	Digital Audio	Network indication	Antenna Supervisor	Jamming detection	Embedded TCP/UDP stack	HTTP, SSL	GPS/GNSS via Modem	Embedded AssistNow Software	FW update over AT (FOAT)	Rx diversity	CellLocate	SIM Access Profile (SAP)
LISA-U200-00S	5.76	7.2	800/850/1900/2100	•	1	1	1	1	9			•	•	•	•	•		•				
LISA-U200-01S	5.76	7.2	800/850/900/1700/1900/2100	•	1	1	1	1	14	2		•	•	•	•	•	•	•		•	•	
LISA-U230-01S	5.76	21.1	800/850/900/1700/1900/2100	•	1	1	1	1	14	2		•	•	•	•	•	•	•	•	•	•	
LISA-U260-01S	5.76	7.2	850/1900	•	1	1	1	1	14	2		•	•	•	•	•	•	•		•	•	
LISA-U270-01S	5.76	7.2	900/2100	•	1	1	1	1	14	2		•	•	•	•	•	•	•		•	•	

Table 1: LISA-U2 series main features summary

Figure 1: LISA-U2 series block diagram (for available options refer to the product features table in Table 1)

1.4 Product description

3G UMTS/HSDPA/HSUPA Characteristics	2G GSM/GPRS/EDGE Characteristics
Class A User Equipment ¹	Class B Mobile Station ²
UMTS Terrestrial Radio Access (UTRA) Frequency Division Duplex (FDD) 3GPP Release 7 Evolved High Speed Packet Access (HSPA+) Rx Diversity for LISA-U230	GSM EDGE Radio Access (GERA) 3GPP Release 7 Rx Diversity for LISA-U230
Dual-band support: - Band II (1900 MHz), Band V (850 MHz) for LISA-U260 - Band I (2100 MHz), Band VIII (900 MHz) for LISA-U270 Quad-band support for LISA-U200-00S: - Band I (2100 MHz), Band II (1900 MHz), Band V (850 MHz), Band VI (800 MHz) Six-band support for LISA-U200 (except for LISA-U200-00S), LISA-U230: - Band I (2100 MHz), Band II (1900 MHz), Band IV (1700 MHz), Band V (850 MHz), Band VI (800 MHz), Band VIII (900 MHz)	Quad-band support GSM 850 MHz, E-GSM 900 MHz, DCS 1800 MHz, PCS 1900 MHz
WCDMA/HSDPA/HSUPA Power Class Power Class 3 (24 dBm) for WCDMA/HSDPA/HSUPA mode	GSM/GPRS Power Class - Power Class 4 (33 dBm) for GSM/E-GSM bands - Power Class 1 (30 dBm) for DCS/PCS bands EDGE Power Class - Power Class E2 (27 dBm) for GSM/E-GSM bands - Power Class E2 (26 dBm) for DCS/PCS bands
PS (Packet Switched) Data Rate - HSUPA category 6, up to 5.76 Mb/s UL - HSDPA category 8 up to 7.2 Mb/s DL for LISA-U200/U260/U270 - HSDPA category 14 up to 21.1 Mb/s DL for LISA-U230 - WCDMA PS data up to 384 kb/s DL/UL	PS (Packet Switched) Data Rate ³ - GPRS multi-slot class 33⁴, coding scheme CS1-CS4, up to 107 kb/s DL, 85.6 kb/s UL for LISA-U200-00S - GPRS multi-slot class 12⁵, coding scheme CS1-CS4, up to 85.6 kb/s DL/UL for all products except LISA-U200-00S - EDGE multi-slot class 33⁴, coding scheme MCS1-MCS9, up to 296 kb/s DL, 236.8 kb/s UL for LISA-U200-00S - EDGE multi-slot class 12⁵, coding scheme MCS1-MCS9, up to 236.8 kb/s DL/UL for all products except LISA-U200-00S
CS (Circuit Switched) Data Rate WCDMA CS data up to 64 kb/s DL/UL	CS (Circuit Switched) Data Rate GSM CS data up to 9.6 kb/s DL/UL supported in transparent/non transparent mode

Table 2: LISA-U2 series UMTS/HSDPA/HSUPA and GSM/GPRS/EDGE characteristics

Operation modes I to III are supported on GSM/GPRS network, with user-defined preferred service selectable from GSM to GPRS. Paging messages for GSM calls can be optionally monitored during GPRS data transfer in not-coordinating NOM II-III.

Direct Link mode is supported for TCP and UDP sockets.

¹ Device can work simultaneously in Packet Switch and Circuit Switch mode: voice calls are possible while the data connection is active without any interruption in service.

² Device can be attached to both GPRS and GSM services (i.e. Packet Switch and Circuit Switch mode) using one service at a time. If for example during data transmission an incoming call occurs, the data connection is suspended to allow the voice communication. Once the voice call has terminated, the data service is resumed.

³ GPRS/EDGE multi-slot class determines the number of timeslots available for upload and download and thus the speed at which data can be transmitted and received, with higher classes typically allowing faster data transfer rates.

⁴ GPRS/EDGE multi-slot class 33 implies a maximum of 5 slots in DL (reception) and 4 slots in UL (transmission) with 6 slots in total.

⁵ GPRS/EDGE multi-slot class 12 implies a maximum of 4 slots in DL (reception) and 4 slots in UL (transmission) with 5 slots in total.

Basic features	Supplementary services	Short Message Service (SMS)
Display of Called Number	Call Hold/Resume (CH)	SMS Classes 1, 2, 3
Indication of Call Progress Signals	Call Waiting (CW)	Mobile-Originating SMS (MO SMS)
Country/PLMN Indication	Multi-Party (MTPY)	Mobile-Terminating SMS (MT SMS)
International Access Function	Call Forwarding (CF)	SMS Cell Broadcast (SMS CB)
Service Indicator	Call Divert	Text and PDU mode supported
Dual Tone Multi Frequency (DTMF)	Explicit Call Transfer (ECT)	SMS during circuit-switched calls
Subscription Identity Management	Call Barring (CB)	SMS over PSD or CSD
Service Provider Indication	Advice of Charge Charging (AOCC)	SMS storage on SIM and memory module
Abbreviated Dialing	Calling Line Identification Presentation (CLIP)	
SIM Toolkit	Calling Line Identification Restriction (CLIR)	
SIM Access Profile ⁶	Connected Line Identification Presentation (COLP)	
	Connected Line Identification Restriction (COLR)	
	Unstructured Supplementary Services Data (USSD)	
	Network Identify and Time Zone (NITZ)	

Table 3: LISA-U2 series Mobile Station basic Features, Supplementary services and SMS services summary⁷

1.5 AT command support

The module supports AT commands according to 3GPP standards: TS 27.007 [1], 27.005 [2], 27.010 [3], and the u-blox AT command extension.



For the complete list of the supported AT commands and their syntax refer to the u-blox AT Commands Manual [5].

RIL (Radio Interface Layer) is provided with LISA-U2 modules and is compatible with following deliveries:

- Android 2.3 (Gingerbread)
- Android 4.0 (Ice Cream Sandwich)
- Android 4.1 (Jelly Bean)
- Windows Embedded CE 6.0
- Windows Embedded Compact 7

⁶ Supported by all LISA-U2 modules versions except LISA-U200-005

⁷ All these functionalities are supported via AT commands (for more details see the u-blox AT Commands Manual [5]).

1.6 Supported features

Table 4 lists the main features supported by LISA-U2 modules. For more details refer to LISA-U Series System Integration Manual [6] and u-blox AT commands manual [5].

Feature	Description
Network Indication	GPIO configured to indicate the network status: registered home network, registered roaming, voice or data call enabled, no service. The feature can be enabled through the +UGPIOC AT command.
Antenna Detection	Antenna presence detection capability is provided, evaluating the resistance from the ANT pin to GND by means of an internal antenna detection circuit. The antenna detection feature can be enabled through the +UANTR AT command.
Jamming detection	Detects some "artificial" interference that obscure the operator's carriers entitled to give access to the GSM/UMTS service and reports the start and stop of such conditions to the application processor (AP). The AP can react appropriately by e.g. switching off the radio transceiver to reduce power consumption and monitoring the environment at constant periods. The feature can be enabled and configured through the +UCD AT command.
Embedded TCP and UDP stack	Embedded TCP/IP and UDP/IP stack including direct link mode for TCP and UDP sockets. Sockets can be set in Direct Link mode to establish a transparent end to end communication with an already connected TCP or UDP socket via serial interface.
FTP, FTPS	File Transfer Protocol as well as Secure File Transfer Protocol (SSL encryption of FTP control channel) functionalities are supported via AT commands.
HTTP, HTTPS	Hyper-Text Transfer Protocol as well as Secure Hyper-Text Transfer Protocol (SSL encryption) functionalities are supported via AT commands. HEAD, GET, POST, DELETE and PUT operations are available. Up to 4 client contexts can be simultaneously used.
GPS / GNSS via Modem	Full access to u-blox positioning chips and modules is available through a dedicated DDC (I ² C) interface. This means that from any host processor a single serial port can control the wireless module and the positioning chip or module. For more details see the GPS Implementation Application Note [12].
Embedded AssistNow Software	Embedded AssistNow Online and AssistNow Offline clients to provide better GPS / GNSS performance and faster Time-to-First-Fix. An AT command can enable / disable the clients.  Not supported by LISA-U200-00S version.
CellLocate™	Enables the estimation of device position based on the parameters of the mobile network cells visible to the specific device based on the CellLocate database: - Normal scan: only the parameters of the visible home network cells are sent - Deep scan: the parameters of all surrounding cells of all mobile operators are sent CellLocate™ is implemented using a set of AT commands for CellLocate service configuration and position request.  Not supported by LISA-U200-00S version.
Hybrid Positioning	The module current position is provided using a u-blox positioning chip or module or the estimated position from CellLocate depending by which positioning method provides the best and fastest solution according to the user configuration Hybrid positioning is implemented through a set of AT commands that allow the configuration and the position request.  Not supported by LISA-U200-00S version.
Firmware update Over AT commands (FOAT)	Firmware module upgrade over UART, USB and SPI interface using AT command.

Feature	Description
Rx Diversity	Improved wireless link quality and reliability on all 2G and 3G operating bands except 2G DCS 1800.  Not supported by LISA-U200, LISA-U260 and LISA-U270.
SIM Access Profile (SAP)	Allows access and use of a remote (U)SIM card instead of the local SIM card directly connected to the module (U)SIM interface. The module acts as an SAP Client establishing a connection and performing data exchange to an SAP Server directly connected to the remote SIM. The modules provide a dedicated USB SAP channel and dedicated multiplexer SAP channel over UART and SPI for communication with the remote (U)SIM card.
Smart Temperature Supervisor	Constant monitoring of the module board temperature: - Warning notification when the temperature approaches an upper or lower predefined threshold - Shutdown notified and forced when the temperature value is outside the specified range (shutdown suspended in case of an emergency call in progress) An AT command can enable or disable the Smart Temperature Supervisor feature (for more details refer to the u-blox AT commands manual [5], +USTS AT command).  The sensor measures board temperature, which can differ from ambient temperature.

Table 4: LISA-U2 series main supported features


u-blox is extremely mindful of user privacy. When a position is sent to the CellLocate™ server u-blox is unable to track the SIM used or the specific device.

2 Interfaces

2.1 Power Management

2.1.1 Module supply (VCC)

Modules must be supplied through the **VCC** pin by a DC power supply. Voltages must be stable: during operation, the current drawn from **VCC** can vary by some order of magnitude, especially due to the surging consumption profile of the GSM system (described in the LISA-U System Integration Manual [6]). It is important that the system power supply circuit is able to support peak power.

2.1.2 RTC supply (V_BCKP)

V_BCKP is the Real Time Clock (RTC) supply. When **VCC** voltage is within the valid operating range, the internal Power Management Unit (PMU) supplies the RTC and the same supply voltage is available on **V_BCKP** pin. If the **VCC** voltage is under the minimum operating limit (e.g. during not powered mode), the **V_BCKP** pin can externally supply the RTC.

2.1.3 Digital I/O interfaces supply (V_INT)

LISA-U2 modules provide an internally generated supply rail output for digital interfaces (**V_INT**). This can be used in place of an external discrete regulator to supply pull-up resistors on the DDC interface. This optimizes the bill of material for various applications, e.g. with u-blox GPS/GNSS receivers operating at 1.8 V.

2.2 RF antenna interface

The **ANT** pin has an impedance of 50 Ω and represents the main Tx/Rx antenna interface.

The **ANT_DIV** pin, provided only by LISA-U230 modules, has an impedance of 50 Ω and represents the Rx diversity antenna interface. The integrated diversity receiver provides improved wireless link quality and reliability on all 2G and 3G operating bands except 2G DCS 1800.

2.3 System functions

2.3.1 Module power-on

LISA-U2 modules can be switched on in one of the following ways:

- Rising edge on the **VCC** pin to a valid voltage for module supply, i.e. applying module supply
- Low pulse on the **PWR_ON** pin, i.e. forcing the pin (normally high with external pull-up) to a low level for a valid time period: **PWR_ON** pin requires an external pull-up resistor to set its value to logic high and may not be left floating
- Rising edge on the **RESET_N** pin, i.e. releasing the pin from the low level, normally high with internal pull-up
- RTC alarm, i.e. pre-programmed scheduled time by AT+CALA command

2.3.2 Module power-off

LISA-U2 modules can be switched off, with proper storage of current parameter settings and network detach, in one of these ways:

- AT+CPWROFF command
- Low level on the **PWR_ON** pin for at least 1 s (not supported by LISA-U200-00S version)

An under-voltage shutdown occurs when the **VCC** supply drops below the extended operating range minimum limit, but in this case it is not possible to perform the storing of the current parameter settings in the module's non-volatile memory as well as the proper network detach.

An over-temperature or an under-temperature shutdown occurs when the temperature measured within the wireless module reaches the dangerous area, if the optional Smart Temperature Supervisor feature is enabled and configured by the dedicated AT command. For more details refer to LISA-U System Integration Manual [6] and u-blox AT commands manual [5], +USTS AT command.

2.3.3 Module reset

LISA-U2 modules can be reset in one of these ways:

- Forcing to the low level the **RESET_N** pin, normally high with internal pull-up. This causes an "external" or "hardware" reset of the entire module, including the integrated power management unit, except for the RTC internal block: the **V_INT** interfaces supply is switched off and all the digital pins are tri-stated, but the **V_BCKP** supply and the RTC block are enabled. Forcing an "external" or "hardware" reset, the current parameter settings are not saved in the module's non-volatile memory and a proper network detach is not performed
- By the AT+CFUN command (refer to u-blox AT Commands Manual [5]). This causes an "internal" or "software" reset of the baseband processor, excluding the integrated power management unit and the RTC internal block: the **V_INT** interfaces supply is enabled and each digital pin is set to its internal reset state (reported in Table 6), the **V_BCKP** supply and the RTC block are enabled. When an "internal" or "software" reset is forced, the current parameter settings are saved in the module's non-volatile memory and a proper network detach is performed

2.4 (U)SIM interface

A (U)SIM card interface is provided on the SMT pads of the LISA-U2 modules: the high-speed SIM/ME interface is implemented as well as automatic detection of the required SIM supporting voltage.

Both 1.8 V and 3 V SIM types are supported (1.8 V and 3 V ME). Activation and deactivation with automatic voltage switch from 1.8 V to 3 V is implemented, according to ISO-IEC 7816-3 specifications. The SIM driver supports the PPS (Protocol and Parameter Selection) procedure for baud-rate selection, according to the values proposed by the SIM Card.

2.5 Serial communication

LISA-U2 modules provide the following serial communication interfaces where AT command interface and Packet-Switched / Circuit-Switched Data communication are concurrently available:

- One asynchronous serial interface (UART)
- One Inter Processor Communication (IPC) interface: two handshake signals added to a SPI interface
- One high-speed USB 2.0 compliant interface

When used as AT command interface, all the serial communication interfaces listed above can be used for firmware upgrade using AT command (+UFWUPD, for more details refer to u-blox AT Commands Manual [5]), but only the following serial communication interfaces can be used for firmware upgrade using the u-blox Easy Flash tool:

- The UART interface, using the **RxD** and **TxD** lines only (the other UART lines are not needed)
- The USB interface, using all the provided lines (**VUSB_DET**, **USB_D+** and **USB_D-**)

2.5.1 Asynchronous serial interface (UART)

The UART interface is a 9-wire unbalanced asynchronous serial interface provided for all communications with LISA-U2 modules.

UART features are:

- Complete serial port with RS-232 functionality conforming to the ITU-T V.24 Recommendation [4], with CMOS compatible signal levels (0 V for low data bit or ON state and 1.8 V for high data bit or OFF state)
- Data lines (**RxD** as output, **TxD** as input), hardware flow control lines (**CTS** as output, **RTS** as input), modem status and control lines (**DTR** as input, **DSR** as output, **DCD** as output, **RI** as output) are provided
- Hardware flow control (default value), software flow control, or none flow control are supported
- Power saving indication available⁸ on the hardware flow control output (**CTS** line): the line is driven to the OFF state when the module is not prepared to accept data by the UART interface
- 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800 and 921600 b/s baud rates are supported for the AT interface
- Autobauding is by default enabled
- Frame format can be:
 - 8N2 (8 data bits, no parity, 2 stop bits)
 - 8N1 (8 data bits, no parity, 1 stop bit)
 - 8E1 (8 data bits, even parity, 1 stop bit)
 - 8O1 (8 data bits, odd parity, 1 stop bit)
 - 7E1 (7 data bits, even parity, 1 stop bit)
 - 7O1 (7 data bits, odd parity, 1 stop bit)
- Default frame configuration is 8N1

UART serial interface can be conveniently configured through AT commands. For more details refer to u-blox AT Commands Manual [5] (+IPR, +ICF, +IFC, &K, \Q, +UPSV AT command) and LISA-U series System Integration Manual [6].



921600 b/s baud rate is not supported by LISA-U200-00S version.

⁸ If enabled

2.5.1.1 Autobauding feature

Only one shot autobauding is supported. This means that the baud rate detection is performed once, at module start up.

After detection the module works at the fixed baud rate (the detected one) and the baud rate can only be changed via the appropriate AT command (+IPR, for more details refer to u-blox AT Commands Manual [5]).

- The module detects the followings baud rates (b/s): 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400
- The only detectable frame configurations are: 7E1, 7O1, 8N1, 8E1, 8O1



Autobauding is not supported by LISA-U200-00S. The default baud rate is 115200 b/s.

2.5.2 Universal Serial Bus (USB)

LISA-U2 modules include a high-speed USB 2.0 compliant interface with maximum throughput of 480 Mb/s. The module itself acts as a USB device and can be connected to any USB host.

The USB is the main interface for transferring high speed data between LISA-U2 series and a host processor.

Signals **USB_D+/USB_D-** carry the USB serial data and signaling. The USB interface is automatically enabled by a valid USB VBUS supply voltage (5.0 V typical) on **VUSB_DET** pin.

LISA-U2 modules provide 6 USB CDCs (Communications Device Class) with this configuration:

- USB1: AT commands / data connection
- USB2: AT commands / data connection
- USB3: AT commands / data connection
- USB4: GPS tunneling
- USB5: Primary TraceLog (debug purpose)
- USB6: Secondary TraceLog (debug purpose)

All LISA-U2 modules versions except LISA-U200-00S provide an additional USB CDC:

- USB7: SAP (SIM Access Profile)

The user can concurrently use AT command interface on one CDC and Packet-Switched / Circuit-Switched Data communication on another CDC.

USB CDC/ACM drivers are available for the following operating system platforms:

- Windows 2000
- Windows XP
- Windows Vista
- Windows 7
- Windows CE 5.0
- Windows Embedded CE 6.0
- Windows Embedded Compact 7
- Windows Embedded Automotive 7
- Windows Mobile 5
- Windows Mobile 6
- Windows Mobile 6.1
- Windows Mobile 6.5

LISA-U2 modules are compatible with standard Linux/Android USB kernel drivers.

2.5.3 Serial Peripheral Interface (SPI)

The LISA-U2 modules provide a 5-wire Inter Processor Communication (IPC) interface that includes two handshake signals (**SPI_MRDY** and **SPI_SRDY**) added to a standard 3-wire SPI-compatible serial interface (**SPI_MOSI**, **SPI_MISO**, **SPI_SCLK**). The LISA-U2 modules run natively as an SPI slave.

The SPI / IPC interface can be used for high speed data transfer (UMTS/HSPA) between LISA-U2 modules and the host processor. The high speed communication (up to 26 Mb/s) between the two processors is possible only if both sides follow the same Inter Processor Communication (IPC) specifications.

Refer to LISA-U series System Integration Manual [6] and SPI Interface Application Note [10] for a detailed description of the implementation of the SPI / IPC protocol.

2.5.4 Multiplexer protocol

LISA-U2 module has a software layer with MUX functionality, 3GPP TS 27.010 Multiplexer Protocol [3], available either on the UART or on the SPI physical link.



The multiplexer protocol is not supported by the USB interface.

This is a data link protocol (layer 2 of OSI model) which uses HDLC-like framing and operates between the module (DCE) and the application processor (DTE) and allows simultaneous sessions over the used physical link (UART or SPI): the user can concurrently use AT command interface on one MUX channel and Packet-Switched / Circuit-Switched Data communication on another MUX channel. The multiplexer protocol can be used on one serial interface (UART or SPI) at a time. Each session consists of a stream of bytes transferring various kinds of data such as SMS, CBS, PSD, GPS, AT commands in general.

LISA-U2 modules provide the following virtual channels:

- Channel 0: control channel
- Channel 1 – 5: AT commands / data connection
- Channel 6: GPS tunneling

All LISA-U2 modules versions except LISA-U200-00S provide an additional virtual channel:

- Channel 7: SAP (SIM Access Profile)

For more details refer to the GSM Mux Implementation Application Note [7].

2.6 DDC (I²C) bus interface

All LISA-U2 modules versions except LISA-U200-00S version include an I²C compatible DDC interface that is available to communicate with a u-blox GPS/GNSS receiver and at the same time with an external I²C device as an audio codec: the LISA-U2 module acts as an I²C master which can communicate with two I²C slaves in accordance to the I²C bus specifications [9].

2.7 Audio



Not supported by LISA-U200-00S version.

LISA-U2 modules have two 4-wire I²S digital audio interfaces:

- First 4-wire I²S digital audio interface (**I2S_CLK**, **I2S_RXD**, **I2S_TXD** and **I2S_WA**)
- Second 4-wire I²S digital audio interface (**I2S1_CLK**, **I2S1_RXD**, **I2S1_TXD** and **I2S1_WA**)

These audio paths are selected by parameters <main_uplink> and <main_downlink> in AT+USPM command (for more details refer to u-blox AT Commands Manual [5]).

LISA-U2 modules provide a digital clock output (**CODEC_CLK**) for an external audio codec.

For further details about the hardware integration of the audio interface in an application design, refer to the LISA-U series System Integration Manual [6].

For further details about the possible settings of the audio interface, as well as the allowed input/output audio path combinations and as the default values related to the uplink/downlink path, refer to u-blox AT Commands Manual [5], +USPM AT command.

2.8 GPIO

LISA-U2 modules provide up to 14 GPIO pins (**GPIO1-GPIO14**) which can be configured for general purpose input/output, or to provide the custom functions listed in Table 5 via u-blox AT commands (for further details refer to LISA-U series System Integration Manual [6] and u-blox AT Commands Manual [5], +UGPIOC, +UGPIOR, +UGPIOW, +UGPS, +UGPRF, +USPM, +UDCONF).

Function	Description	Module	Default GPIO	Configurable GPIOs
GSM Tx-burst indication	GSM transmit slot indication	All	--	GPIO1
GPS supply enable	Enable/disable the supply of u-blox GPS/GNSS receiver connected to wireless module	All except LISA-U200-00S	GPIO2	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5
		LISA-U200-00S	--	--
GPS data ready	Sense when u-blox GPS/GNSS receiver connected to wireless module is ready for sending data by the DDC (I ² C)	All except LISA-U200-00S	GPIO3	GPIO3
		LISA-U200-00S	--	--
GPS RTC sharing	RTC (Real Time Clock) synchronization signal to u-blox GPS/GNSS receiver connected to wireless module	All except LISA-U200-00S	GPIO4	GPIO4
		LISA-U200-00S	--	--
SIM card detection	SIM card presence	All	GPIO5	GPIO5
SIM card hot insertion/removal	SIM card hot insertion/removal	All except LISA-U200-00S	--	GPIO5
		LISA-U200-00S	--	--
Network status indication	Network status: registered 2G / 3G home network, registered 2G / 3G roaming, 2G / 3G data transmission, no service	All	--	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5
Module status indication	Module status: power off mode, i.e. module switched off, versus idle, active or connected mode, i.e. module switched on	All except LISA-U200-00S	--	GPIO1, GPIO13
		LISA-U200-00S	--	--

Function	Description	Module	Default GPIO	Configurable GPIOs
Module operating mode indication	Module operating mode: idle mode versus active or connected mode	All except LISA-U200-00S	--	GPIO5, GPIO14
		LISA-U200-00S	--	--
I ² S digital audio interface	Second I2S digital audio interface (I2S1_RXD , I2S1_TXD , I2S1_CLK , I2S1_WA respectively)	All except LISA-U200-00S	GPIO6, GPIO7, GPIO8, GPIO9	GPIO6, GPIO7, GPIO8, GPIO9
		LISA-U200-00S	--	--
SPI serial interface	SPI / IPC serial interface (SPI_SCLK , SPI_MOSI , SPI_MISO , SPI_SRDY and SPI_MRDY respectively)	All	GPIO10, GPIO11, GPIO12, GPIO13, GPIO14	GPIO10, GPIO11, GPIO12, GPIO13, GPIO14
General purpose input	Input to sense high or low digital level	All except LISA-U200-00S	--	All
		LISA-U200-00S	--	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, GPIO9
General purpose output	Output to set the high or the low digital level	All except LISA-U200-00S	--	All
		LISA-U200-00S	--	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, GPIO9
Pad disabled	Tri-state with an internal active pull-down enabled	All except LISA-U200-00S	GPIO1	All
		LISA-U200-00S	GPIO1, GPIO2, GPIO3, GPIO4, GPIO6, GPIO7, GPIO8, GPIO9	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, GPIO9

Table 5: GPIO custom functions configuration

3 Pin definition

3.1 Pin assignment

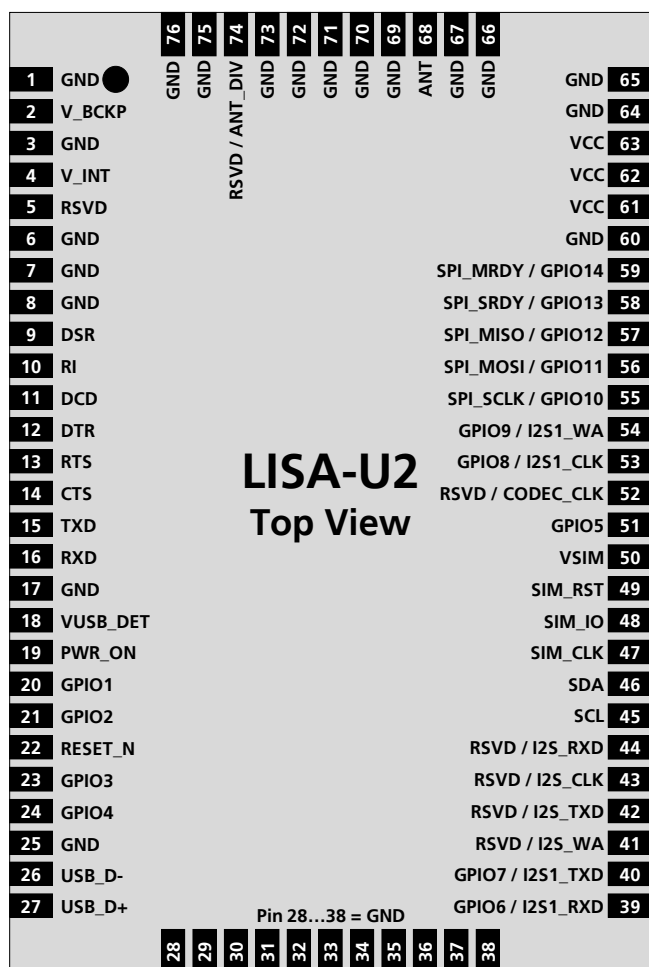


Figure 2: LISA-U2 series pin assignment

No	Module	Name	Power domain	I/O	Description	Remarks
1	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
2	All	V_BCKP	-	I/O	Real Time Clock supply input/output	V_BCKP = 1.8 V (typical) generated by the module to supply the Real Time Clock when VCC supply voltage is within valid operating range. A backup battery can be connected to this pin to supply the Real Time Clock when VCC supply voltage is not within valid operating range. See section 4.2.3 for detailed electrical specs.
3	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
4	All	V_INT	-	O	Digital I/O Interfaces supply output	V_INT = 1.8V (typical) generated by the module when it is switched-on and the RESET_N (external reset input pin) is not forced to the low level. See section 4.2.3 for detailed electrical specs.

No	Module	Name	Power domain	I/O	Description	Remarks
5	All	RSVD	-	N/A	RESERVED pin	This pin has special function: it must be connected to GND to allow module to work properly.
6	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
7	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
8	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
9	All	DSR	GDI	O	UART data set ready	Circuit 107 (DSR) in ITU-T V.24. Output driver class D. PU/PD class a. Value at internal reset: T/PU. See section 4.2.9 for detailed electrical specs.
10	All	RI	GDI	O	UART ring indicator	Circuit 125 (RI) in ITU-T V.24. Output driver class C ₀ . PU/PD class c. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
11	All	DCD	GDI	O	UART data carrier detect	Circuit 109 (DCD) in ITU-T V.24. Output driver class C ₀ . PU/PD class c. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
12	All	DTR	GDI	I	UART data terminal ready	Circuit 108/2 (DTR) in ITU-T V. 24. Internal active pull-up to V _{INT} enabled. PU/PD class c. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
13	All	RTS	GDI	I	UART ready to send	Circuit 105 (RTS) in ITU-T V.24. Internal active pull-up to V _{INT} enabled. PU/PD class a. Value at internal reset: T/PU. See section 4.2.9 for detailed electrical specs.
14	All	CTS	GDI	O	UART clear to send	Circuit 106 (CTS) in ITU-T V.24. Output driver class A. PU/PD class a. Value at internal reset: T/PU. See section 4.2.9 for detailed electrical specs.
15	All	TXD	GDI	I	UART transmitted data	Circuit 103 (TxD) in ITU-T V.24. Internal active pull-up to V _{INT} enabled. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
16	All	RXD	GDI	O	UART received data	Circuit 104 (Rx) in ITU-T V.24. Output driver class A. PU/PD class a. Value at internal reset: T/PU. See section 4.2.9 for detailed electrical specs.
17	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
18	All	VUSB_DET	USB	I	USB detect input	Input for VBUS (5 V typical) USB supply sense. See section 4.2.10 for detailed electrical specs.
19	All	PWR_ON	POS	I	Power-on input	The PWR_ON pin has high input impedance: don't leave it floating in noisy environment (an external pull-up resistor is required) See section 4.2.6 for detailed electrical specs.
20	All	GPIO1	GDI	I/O	GPIO	Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
21	All	GPIO2	GDI	I/O	GPIO	Output driver class E. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
22	All	RESET_N	ERS	I	External reset input	Internal 10 kΩ pull-up resistor to V _{BCKP} . See section 4.2.7 for detailed electrical specs.
23	All	GPIO3	GDI	I/O	GPIO	Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.

No	Module	Name	Power domain	I/O	Description	Remarks
24	All	GPIO4	GDI	I/O	GPIO	Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
25	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
26	All	USB_D-	USB	I/O	USB Data Line D-	90 Ω nominal differential impedance Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 high-speed specification [8] are part of the USB pin driver and need not be provided externally. Value at internal reset: T. See section 4.2.10 for detailed electrical specs.
27	All	USB_D+	USB	I/O	USB Data Line D+	90 Ω nominal differential impedance Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 high-speed specification [8] are part of the USB pin driver and need not be provided externally. Value at internal reset: T. See section 4.2.10 for detailed electrical specs.
28	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
29	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
30	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
31	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
32	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
33	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
34	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
35	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
36	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
37	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
38	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
39	LISA-U200-00S	GPIO6	GDI	I/O	GPIO	Can be configured as GPIO. Output driver class E. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
	All except LISA-U200-00S	I2S1_RXD / GPIO6	GDI	I / I/O	2 nd I ² S receive data / GPIO	Can be configured as receive data input of the second digital audio interface (with internal active pull-down to GND enabled), or as GPIO. Output driver class E. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
40	LISA-U200-00S	GPIO7	GDI	I/O	GPIO	Can be configured as GPIO. Output driver class E. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
	All except LISA-U200-00S	I2S1_TXD / GPIO7	GDI	O / I/O	2 nd I ² S transmit data / GPIO	Can be configured as transmit data output of the second digital audio interface, or as GPIO. Output driver class E. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
41	LISA-U200-00S	RSVD	-	N/A	RESERVED pin	Pin disabled.
	All except LISA-U200-00S	I2S_WA	GDI	I/O	1 st I ² S word alignment	Input with internal active pull-down to GND enabled in slave mode, Output in master mode. Output driver class C. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.

No	Module	Name	Power domain	I/O	Description	Remarks
42	LISA-U200-00S	RSVD	-	N/A	RESERVED pin	Pin disabled.
	All except LISA-U200-00S	I2S_TXD	GDI	O	1 st I ² S transmit data	Output driver class C. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
43	LISA-U200-00S	RSVD	-	N/A	RESERVED pin	Pin disabled.
	All except LISA-U200-00S	I2S_CLK	GDI	I/O	1 st I ² S clock	Input with internal active pull-down to GND enabled in slave mode, Output in master mode. Output driver class C. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
44	LISA-U200-00S	RSVD	-	N/A	RESERVED pin	Pin disabled.
	All except LISA-U200-00S	I2S_RXD	GDI	I	1 st I ² S receive data	Internal active pull-down to GND enabled. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
45	All	SCL	DDC	O	I ² C bus clock line	Fixed open drain. No internal pull-up. Value at internal reset: T. See section 4.2.11 for detailed electrical specs.
46	All	SDA	DDC	I/O	I ² C bus data line	Fixed open drain. No internal pull-up. Value at internal reset: T. See section 4.2.11 for detailed electrical specs.
47	All	SIM_CLK	SIM	O	SIM clock	Value at internal reset: L. See section 4.2.8 for detailed electrical specs.
48	All	SIM_IO	SIM	I/O	SIM data	Internal 4.7 k Ω pull-up resistor to VSIM. Value at internal reset: L/PD. See section 4.2.8 for detailed electrical specs.
49	All	SIM_RST	SIM	O	SIM reset	Value at internal reset: L. See section 4.2.8 for detailed electrical specs.
50	All	VSIM	-	O	SIM supply output	VSIM = 1.80 V typical or 2.90 V typical generated by the module according to the SIM card type. See section 4.2.3 for detailed electrical specs.
51	All	GPIO5	GDI	I/O	GPIO	Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
52	LISA-U200-00S	RSVD	-	N/A	RESERVED pin	Pin disabled.
	All except LISA-U200-00S	CODEC_CLK	GDI	O	Clock output	Output driver class B. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
53	LISA-U200-00S	GPIO8	GDI	I/O	GPIO	Can be configured as GPIO. Output driver class E. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
	All except LISA-U200-00S	I2S1_CLK / GPIO8	GDI	I/O / I/O	2 nd I ² S clock / GPIO	Can be configured as clock (Input with internal active pull-down to GND enabled in slave mode, Output in master mode) of the second digital audio interface, or as GPIO. Output driver class E. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.

No	Module	Name	Power domain	I/O	Description	Remarks
54	LISA-U200-00S	GPIO9	GDI	I/O	GPIO	Can be configured as GPIO. Output driver class E. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
	All except LISA-U200-00S	I2S1_WA / GPIO9	GDI	I/O / I/O	2 nd I ² S word alignment / GPIO	Can be configured as word alignment (Input with internal active pull-down to GND enabled in slave mode, Output in master mode) of the second digital audio interface, or as GPIO. Output driver class E. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
55	LISA-U200-00S	SPI_SCLK	GDI	I	SPI Serial Clock Input	SPI Serial Clock Input: - Idle low (CPOL=0) - Internal active pull-down to GND enabled. Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
	All except LISA-U200-00S	SPI_SCLK / GPIO10	GDI	I / I/O	SPI Serial Clock Input / GPIO	Can be set as SPI Serial Clock Input, or as GPIO When configured as SPI Serial Clock: - Idle low (CPOL=0) - Internal active pull-down to GND enabled. Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
56	LISA-U200-00S	SPI_MOSI	GDI	I	SPI Data Line Input	SPI Data Line Input: - Shift data on rising clock edge (CPHA=1) - Latch data on falling clock edge (CPHA=1) - Idle high. - Internal active pull-up to V_INT enabled. Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
	All except LISA-U200-00S	SPI_MOSI / GPIO11	GDI	I / I/O	SPI Data Line Input / GPIO	Can be set as SPI Data Line Input, or as GPIO When configured as SPI Data Line Input: - Shift data on rising clock edge (CPHA=1) - Latch data on falling clock edge (CPHA=1) - Idle high. - Internal active pull-up to V_INT enabled. Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
57	LISA-U200-00S	SPI_MISO	GDI	O	SPI Data Line Output	SPI Data Line Output: - Shift data on rising clock edge (CPHA=1) - Latch data on falling clock edge (CPHA=1) - Idle high Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
	All except LISA-U200-00S	SPI_MISO / GPIO12	GDI	O / I/O	SPI Data Line Output / GPIO	Can be set as SPI Data Line Output, or as GPIO When configured as SPI Data Line Output: - Shift data on rising clock edge (CPHA=1) - Latch data on falling clock edge (CPHA=1) - Idle high Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.

No	Module	Name	Power domain	I/O	Description	Remarks
58	LISA-U200-00S	SPI_SRDY	GDI	O	SPI Slave Ready Output	SPI Slave Ready Output: Idle low Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
	All except LISA-U200-00S	SPI_SRDY / GPIO13	GDI	O / I/O	SPI Slave Ready Output / GPIO	Can be set as SPI Slave Ready Output, or as GPIO When configured as SPI Slave Ready Output: Idle low Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
59	LISA-U200-00S	SPI_MRDY	GDI	I	SPI Master Ready Input	SPI Master Ready Input: - Idle low - Internal active pull-down to GND enabled Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
	All except LISA-U200-00S	SPI_MRDY / GPIO14	GDI	I / I/O	SPI Master Ready Input / GPIO	Can be set as SPI Master Ready Input, or as GPIO When configured as SPI Master Ready Input: - Idle low - Internal active pull-down to GND enabled Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
60	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
61	All	VCC	-	I	Module supply input	All VCC pins must be connected to external supply
62	All	VCC	-	I	Module supply input	All VCC pins must be connected to external supply
63	All	VCC	-	I	Module supply input	All VCC pins must be connected to external supply
64	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
65	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
66	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
67	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
68	All	ANT	-	I/O	RF input/output for main Tx/Rx antenna	50 Ω nominal impedance
69	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
70	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
71	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
72	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
73	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
74	All except LISA-U230	RSVD	-	N/A	RESERVED pin	Leave unconnected.
	LISA-U230	ANT_DIV	-	I	RF input for Rx diversity antenna	50 Ω nominal impedance
75	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
76	All	GND	-	N/A	Ground	All GND pins must be connected to ground.

Table 6: Pinout


For more information about pinout refer to LISA-U series System Integration Manual [6].

Explanation of abbreviations and terms used is reported in Appendix A.

4 Electrical specifications

 **Stressing the device above one or more of the ratings listed in the Absolute Maximum Rating section may cause permanent damage. These are stress ratings only. Operating the module at these or at any conditions other than those specified in the Operating Conditions sections (chapter 4.2) of the specification should be avoided. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.**

 Operating conditions ranges define those limits within which the functionality of the device is guaranteed.

 Where application information is given, it is advisory only and does not form part of the specification.

4.1 Absolute maximum rating

 Limiting values given below are in accordance with the Absolute Maximum Rating System (IEC 134).

Symbol	Description	Condition	Min.	Max.	Unit
VCC	Module supply voltage	Input DC voltage at VCC pin	-0.30	5.50	V
ICC	Module supply current	Input DC current at VCC pin		2.50	A
VUSB_DET	USB detection pin	Input DC voltage at VUSB_DET	-0.30	5.35	V
USB	USB D+/D- pins	Input DC voltage at USB_D+ and USB_D-	-1.00	5.35	V
V_BCKP	RTC supply voltage	Input DC voltage at V_BCKP pin	-0.15	2.00	V
GDI	Generic digital interfaces	Input DC voltage at Generic digital interfaces pins	-0.30	3.60	V
DDC	DDC interface	Input DC voltage at DDC interface pins	-0.30	3.60	V
SIM	SIM interface	Input DC voltage at SIM interface pin	-0.30	3.60	V
ERS	External reset signal	Input DC voltage at External reset signal pin	-0.15	2.10	V
POS	Power-on input	Input DC voltage at Power-on signal pin	-0.30	5.50	V
V_ANT	Antenna voltage	Input DC voltage at ANT pin	-0.15	3.00	V
P_ANT	Antenna power	Input RF power at ANT pin		-8	dBm
Rho_ANT	Antenna ruggedness	Output RF load mismatch ruggedness at ANT pin		10:1	VSWR
Tstg	Storage Temperature		-40	90	°C

Table 7: Absolute maximum ratings

 **The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification, given in table above, must be limited to values within the specified boundaries by using appropriate protection devices.**

4.1.1 Maximum ESD

Parameter	Module	Min.	Typ.	Max.	Unit	Remarks
ESD sensitivity for all pins except ANT and ANT_DIV pins	All			1000	V	Human Body Model according to JESD22-A114F
ESD sensitivity for ANT pin	All			1000	V	Human Body Model according to JESD22-A114F
ESD sensitivity for ANT_DIV pin	LISA-U230			1000	V	Human Body Model according to JESD22-A114F
ESD immunity for ANT pin	All			1000	V	Contact Discharge according to IEC 61000-4-2
				1000	V	Air Discharge according to IEC 61000-4-2
ESD immunity for ANT_DIV pin	LISA-U230			4000	V	Contact Discharge according to IEC 61000-4-2
				8000	V	Air Discharge according to IEC 61000-4-2

Table 8: Maximum ESD ratings

 **LISA-U2 modules are Electrostatic Sensitive Devices (ESD) and require special precautions when handling.**

4.2 Operating conditions



Unless otherwise indicated, all operating condition specifications are at an ambient temperature of 25°C.



Operation beyond the operating conditions is not recommended and extended exposure beyond them may affect device reliability.

4.2.1 Operating temperature range

Symbol	Parameter	Min.	Typ.	Max.	Units	Remarks
Topr	Operating temperature range	-40		+85	°C	
		-20		+65	°C	Normal operating temperature range See chapter 4.2.1.1
		-40		-20	°C	Extended operating temperature range 1 See chapter 4.2.1.2
		+65		+85	°C	Extended operating temperature range 2 See chapter 4.2.1.3

Table 9: Environmental conditions

4.2.1.1 Normal operating temperature range

The wireless module is fully functional and meets the 3GPP specification across the specified temperature range.

4.2.1.2 Extended operating temperature range 1

The wireless module is fully functional across the specified temperature range. Occasional deviations from the 3GPP specification may occur.

4.2.1.3 Extended operating temperature range 2

The wireless module is functional across the specified temperature range. Occasional deviations from the 3GPP specification may occur. Thermal protection including automatic shutdown is implemented for protection against overheating. Thermal protection is disabled for emergency calls. For more details, refer to u-blox AT Commands Manual [5], +USTS AT command).

4.2.2 Module thermal resistance

Symbol	Parameter	Min.	Typ.	Max.	Units	Remarks
Rth,M-A	Module-to-Ambient thermal resistance	7		12	°C/W	Thermal resistance from the module internal temperature sensor to the ambient, with the module mounted on a 90 mm x 70 mm x 1.46 mm 4-Layers PCB with a high coverage of copper in still air conditions
Rth,M-C	Module-to-Case thermal resistance	1.5		3.5	°C/W	Thermal resistance from the module internal temperature sensor to the module case, evaluated as the thermal resistance from the module internal temperature sensor to the ambient, with the module mounted on a 90 mm x 70 mm x 1.46 mm 4-Layers PCB with a high coverage of copper, with a robust aluminum heat-sink on the back of the application board, with forced air ventilation

Table 10: Module thermal resistance

4.2.3 Supply/Power pins

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Module supply normal operating input voltage ⁹	3.30	3.80	4.40	V
	Module supply extended operating input voltage ¹⁰	3.10		4.50	V
ICC_PEAK	Module supply peak current consumption: peak of current consumption through the VCC pad during a GSM transmit burst, at VCC = 3.8 V, with a matched antenna (typ. value) or with a mismatched antenna (max. value) ¹¹		2.00	2.50	A
V_BCKP	RTC supply input voltage	1.00	1.80	1.90	V
I_BCKP	RTC supply average current consumption, at V_BCKP = 1.8 V		2.00		μA

Table 11: Input characteristics of Supply/Power pins

Symbol	Parameter	Min.	Typ.	Max.	Unit
VSIM	SIM supply output voltage	1.76	1.80	1.83	V
		2.84	2.90	2.94	V
V_BCKP	RTC supply output voltage	1.71	1.80	1.89	V
I_BCKP	RTC supply output current capability			3	mA
V_INT	Digital I/O Interfaces supply output voltage	1.73	1.80	1.87	V
I_INT	Digital I/O Interfaces supply output current capability			50	mA

Table 12: Output characteristics of Supply/Power pins

⁹ Input voltage at **VCC** must be above the normal operating range minimum limit to switch-on the module.

¹⁰ Occasional deviations from the 3GPP specifications may occur. Ensure that input voltage at **VCC** never drops below the extended operating range minimum limit during module operation: the wireless module may switch-off when the **VCC** voltage value drops below the extended operating range minimum limit.

¹¹ Use this figure to dimension maximum current capability of power supply.

4.2.4 Power consumption

Table 13 reports power consumption of LISA-U2 module¹².

Mode	Band	Condition	Power Consumption ¹³
Power Off Mode		Module is switched off by AT+CPWROFF	< 60 µA
2G Cyclic Idle/Active-Mode (Power Saving enabled by AT+UPSV)	All 2G bands	DRX = 9 ¹⁴ , AT+UPSV=2, USB interface not attached to a USB host	< 1.0 mA
	All 2G bands	DRX = 5 ¹⁵ , AT+UPSV=1, USB interface not attached to a USB host	< 1.5 mA
	All 2G bands	DRX = 5 ¹⁵ , AT+UPSV=1, USB interface in the suspend state	< 2.0 mA
GSM Connected (Talk) Mode	850 / 900	1 Tx + 1 Rx slot (voice call) Maximum Tx power (32.5 dBm typ.)	< 260 mA
	1800 / 1900	1 Tx + 1 Rx slot (voice call) Maximum Tx power (29.5 dBm typ.)	< 220 mA
GPRS Connected Mode	850 / 900	4 Tx + 2 Rx slots (up to 85.6 kb/s UL, 42.8 kb/s DL) Maximum Tx power (30.5 dBm typ.)	< 600 mA
	1800 / 1900	4 Tx + 2 Rx slots (up to 85.6 kb/s UL, 42.8 kb/s DL) Maximum Tx power (27.5 dBm typ.)	< 450 mA
EDGE Connected Mode	850 / 900	4 Tx + 2 Rx slots (up to 236.8 kb/s UL, 118.4 kb/s DL) Maximum Tx power (25.0 dBm typ.)	< 510 mA
	1800 / 1900	4 Tx + 2 Rx slots (up to 236.8 kb/s UL, 118.4 kb/s DL) Maximum Tx power (24.0 dBm typ.)	< 500 mA
3G Cyclic Idle/Active-Mode (Power Saving enabled by AT+UPSV)	All 3G bands	DRX = 9 ¹⁶ , AT+UPSV=2, USB interface not attached to a USB host	< 1.2 mA
	All 3G bands	DRX = 7 ¹⁷ , AT+UPSV=1, USB interface not attached to a USB host	< 1.5 mA
	All 3G bands	DRX = 7 ¹⁷ , AT+UPSV=1, USB interface in the suspend state	< 2.0 mA
UMTS Connected (Talk) Mode	Band I	12.2 kb/s UL, 12.2 kb/s DL Maximum Tx power (23.0 dBm typ.)	< 600 mA
	Band II	12.2 kb/s UL, 12.2 kb/s DL Maximum Tx power (23.0 dBm typ.)	< 750 mA
	Band IV	12.2 kb/s UL, 12.2 kb/s DL Maximum Tx power (23.0 dBm typ.)	< 600 mA
	Band V / VI	12.2 kb/s UL, 12.2 kb/s DL Maximum Tx power (23.0 dBm typ.)	< 450 mA
	Band VIII	12.2 kb/s UL, 12.2 kb/s DL Maximum Tx power (23.0 dBm typ.)	< 450 mA
HSDPA Connected Mode	Band I	384 kb/s UL, 7.2 Mb/s / 21.1 Mb/s DL Maximum Tx power (23.0 dBm typ.)	< 700 mA
	Band II	384 kb/s UL, 7.2 Mb/s / 21.1 Mb/s DL Maximum Tx power (23.0 dBm typ.)	< 850 mA
	Band IV	384 kb/s UL, 7.2 Mb/s / 21.1 Mb/s DL Maximum Tx power (23.0 dBm typ.)	< 700 mA
	Band V / VI	384 kb/s UL, 7.2 Mb/s / 21.1 Mb/s DL Maximum Tx power (23.0 dBm typ.)	< 550 mA
	Band VIII	384 kb/s UL, 7.2 Mb/s / 21.1 Mb/s DL Maximum Tx power (23.0 dBm typ.)	< 550 mA

¹² It is assumed that no significant load is connected to any digital and analog pin except for antenna

¹³ Maximum values for module average current consumption through **VCC** pins in the listed modes/conditions, at 25°C, with **VCC** = 3.8 V, with a matched antenna.

¹⁴ Module is registered with the network, with a paging period of 2.12 s (2G network DRX setting = 9), with none neighbour cell.

¹⁵ Module is registered with the network, with a paging period of 1.18 s (2G network DRX setting = 5), with 16 neighbour cells.

¹⁶ Module is registered with the network, with a paging period of 5.12 s (3G network DRX setting = 9).

¹⁷ Module is registered with the network, with a paging period of 1.28 s (3G network DRX setting = 7).

Mode	Band	Condition	Power Consumption ¹³
HSPA Connected Mode	Band I	5.76 Mb/s UL, 384 kb/s DL Maximum Tx power (21.0 dBm typ.)	< 650 mA
	Band II	5.76 Mb/s UL, 384 kb/s DL Maximum Tx power (21.0 dBm typ.)	< 800 mA
	Band IV	5.76 Mb/s UL, 384 kb/s DL Maximum Tx power (21.0 dBm typ.)	< 650 mA
	Band V / VI	5.76 Mb/s UL, 384 kb/s DL Maximum Tx power (21.0 dBm typ.)	< 500 mA
	Band VIII	5.76 Mb/s UL, 384 kb/s DL Maximum Tx power (21.0 dBm typ.)	< 500 mA
HSPA Connected Mode	Band I	5.76 Mb/s UL, 7.2 Mb/s / 21.1 Mb/s DL Maximum Tx power (21.0 dBm typ.)	< 650 mA
	Band II	5.76 Mb/s UL, 7.2 Mb/s / 21.1 Mb/s DL Maximum Tx power (21.0 dBm typ.)	< 800 mA
	Band IV	5.76 Mb/s UL, 7.2 Mb/s / 21.1 Mb/s DL Maximum Tx power (21.0 dBm typ.)	< 650 mA
	Band V / VI	5.76 Mb/s UL, 7.2 Mb/s / 21.1 Mb/s DL Maximum Tx power (21.0 dBm typ.)	< 500 mA
	Band VIII	5.76 Mb/s UL, 7.2 Mb/s / 21.1 Mb/s DL Maximum Tx power (21.0 dBm typ.)	< 500 mA

Table 13: Power consumption

4.2.5 RF Performance

Parameter		Min.	Max.	Unit	Remarks
Frequency range GSM 850	Uplink	824	849	MHz	Module transmit
	Downlink	869	894	MHz	Module receive
Frequency range E-GSM 900	Uplink	880	915	MHz	Module transmit
	Downlink	925	960	MHz	Module receive
Frequency range DCS 1800	Uplink	1710	1785	MHz	Module transmit
	Downlink	1805	1880	MHz	Module receive
Frequency range PCS 1900	Uplink	1850	1910	MHz	Module transmit
	Downlink	1930	1990	MHz	Module receive
Frequency range UMTS 800 (band VI)	Uplink	830	840	MHz	Module transmit
	Downlink	875	885	MHz	Module receive
Frequency range UMTS 850 (band V)	Uplink	824	849	MHz	Module transmit
	Downlink	869	894	MHz	Module receive
Frequency range UMTS 900 (band VIII)	Uplink	880	915	MHz	Module transmit
	Downlink	925	960	MHz	Module receive
Frequency range UMTS 1700 (band IV)	Uplink	1710	1755	MHz	Module transmit
	Downlink	2110	2155	MHz	Module receive
Frequency range UMTS 1900 (band II)	Uplink	1850	1910	MHz	Module transmit
	Downlink	1930	1990	MHz	Module receive
Frequency range UMTS 2100 (band I)	Uplink	1920	1980	MHz	Module transmit
	Downlink	2110	2170	MHz	Module receive

Table 14: Operating RF frequency bands

Parameter	Min.	Typ.	Max.	Unit	Remarks
Receiver input sensitivity GSM 850 / E-GSM 900	-102.0	-110.0		dBm	Downlink RF level @ BER Class II < 2.4 %
Receiver input sensitivity DCS 1800 / PCS 1900	-102.0	-109.0		dBm	Downlink RF level @ BER Class II < 2.4 %
Receiver input sensitivity UMTS 800 (band VI)	-106.7	-111.0		dBm	Downlink RF level for RMC @ BER < 0.1 %
Receiver input sensitivity UMTS 850 (band V)	-104.7	-112.0		dBm	Downlink RF level for RMC @ BER < 0.1 %
Receiver input sensitivity UMTS 900 (band VIII)	-103.7	-111.0		dBm	Downlink RF level for RMC @ BER < 0.1 %
Receiver input sensitivity UMTS 1700 (band IV)	-106.7	-111.0		dBm	Downlink RF level for RMC @ BER < 0.1 %
Receiver input sensitivity UMTS 1900 (band II)	-104.7	-111.0		dBm	Downlink RF level for RMC @ BER < 0.1 %
Receiver input sensitivity UMTS 2100 (band I)	-106.7	-111.0		dBm	Downlink RF level for RMC @ BER < 0.1 %
Condition: 50 Ω source					

Table 15: Receiver sensitivity performance

Parameter	Min.	Typ.	Max.	Unit	Remarks
Maximum output power GSM 850 / E-GSM 900		32.5		dBm	Uplink burst RF power for GSM or GPRS 1-slot TCH at PCL 5 or Gamma 3
		32.5		dBm	Uplink burst RF power for GPRS 2-slot TCH at Gamma 3
		31.7		dBm	Uplink burst RF power for GPRS 3-slot TCH at Gamma 3
		30.5		dBm	Uplink burst RF power for GPRS 4-slot TCH at Gamma 3
		27.0		dBm	Uplink burst RF power for EDGE 8PSK 1-slot TCH at PCL 8 or Gamma 6
		27.0		dBm	Uplink burst RF power for EDGE 8PSK 2-slot TCH at Gamma 6
		26.2		dBm	Uplink burst RF power for EDGE 8PSK 3-slot TCH at Gamma 6
		25.0		dBm	Uplink burst RF power for EDGE 8PSK 4-slot TCH at Gamma 6
Maximum output power DCS 1800 / PCS 1900		29.5		dBm	Uplink burst RF power for GSM or GPRS 1-slot TCH at PCL 0 or Gamma 3
		29.5		dBm	Uplink burst RF power for GPRS 2-slot TCH at Gamma 3
		28.7		dBm	Uplink burst RF power for GPRS 3-slot TCH at Gamma 3
		27.5		dBm	Uplink burst RF power for GPRS 4-slot TCH at Gamma 3
		26.0		dBm	Uplink burst RF power for EDGE 8PSK 1-slot TCH at PCL 2 or Gamma 5
		26.0		dBm	Uplink burst RF power for EDGE 8PSK 2-slot TCH at Gamma 5
		25.2		dBm	Uplink burst RF power for EDGE 8PSK 3-slot TCH at Gamma 5
		24.0		dBm	Uplink burst RF power for EDGE 8PSK 4-slot TCH at Gamma 5
Maximum output power UMTS 800 (Band VI)		23.0		dBm	Uplink continuous RF power for RMC at maximum power
Maximum output power UMTS 850 (Band V)		23.0		dBm	Uplink continuous RF power for RMC at maximum power
Maximum output power UMTS 900 (Band VIII)		23.0		dBm	Uplink continuous RF power for RMC at maximum power
Maximum output power UMTS 1700 (Band IV)		23.0		dBm	Uplink continuous RF power for RMC at maximum power
Maximum output power UMTS 1900 (Band II)		23.0		dBm	Uplink continuous RF power for RMC at maximum power
Maximum output power UMTS 2100 (Band I)		23.0		dBm	Uplink continuous RF power for RMC at maximum power

Condition for all parameters: 50 Ω output load

Condition for GPRS/EDGE multi-slot output power: Multi-Slot Power Reduction profile 2 (+UDCONF AT command default value)

Table 16: Transmitter maximum output power

4.2.6 PWR_ON pin

Pin Name	Parameter	Min.	Typ.	Max.	Unit	Remarks
PWR_ON	Internal supply for Power-On Input Signal	1.71	1.80	1.89	V	RTC supply (V_BCKP)
	L-level input	-0.30		0.65	V	High input impedance (no internal pull-up)
	H-level input	1.50		4.40	V	High input impedance (no internal pull-up)
	L-level input current		-6		μA	
	PWR_ON low time to switch-on the module	50		80	μs	
	PWR_ON low time to switch-off the module	1000			ms	Not supported by LISA-U200-00S

Table 17: PWR_ON pin characteristics (POS domain)

4.2.7 RESET_N pin

Pin Name	Parameter	Min.	Typ.	Max.	Unit	Remarks
RESET_N	Internal supply for External Reset Input Signal	1.71	1.80	1.89	V	RTC supply (V_BCKP)
	L-level input	-0.30		0.51	V	
	H-level input	1.32		2.01	V	
	L-level input current		-180		μA	
	Pull-up resistance		10		kΩ	Internal pull-up to RTC supply (V_BCKP)
	RESET_N low time to perform a proper reset	50			ms	

Table 18: RESET_N pin characteristics (ERS domain)

4.2.8 (U)SIM pins

The SIM pins are a dedicated interface to the (U)SIM chip card/IC. The electrical characteristics fulfill regulatory specification requirements. The values in Table 19 are for information only.

Parameter	Min.	Typ.	Max.	Unit	Remarks
Low-level input	0.00		0.35	V	VSIM = 1.80 V
	0.00		0.57	V	VSIM = 2.90 V
High-level input	1.29		3.30	V	VSIM = 1.80 V
	2.07		3.30	V	VSIM = 2.90 V
Low-level output		0.00	0.35	V	VSIM = 1.80 V, Max value at I _{OL} = +1.0 mA
		0.00	0.35	V	VSIM = 2.90 V, Max value at I _{OL} = +1.0 mA
High-level output	1.26	1.80		V	VSIM = 1.80 V, Min value at I _{OH} = -1.0 mA
	2.03	2.90		V	VSIM = 2.90 V, Min value at I _{OH} = -1.0 mA
Input/Output leakage current			0.7	μA	0.2V < V _{IN} < 3.3V
Internal pull-up resistor on SIM_IO to VSIM		4.7		kΩ	
Clock frequency on SIM_CLK		3.25		MHz	

Table 19: (U)SIM pins characteristics (SIM domain)

4.2.9 Generic Digital Interfaces pins

Parameter	Min.	Typ.	Max.	Unit	Remarks
Internal supply for GDI domain	1.73	1.80	1.87	V	Digital I/O Interfaces supply (V_INT)
Input characteristic: L-level input	-0.20		0.35	V	
Input characteristic: H-level input	1.31		1.93	V	
Output characteristics: L-level output		0.00	0.20	V	Max value at $I_{OL} = +0.1$ mA for driver class A
		0.00	0.35	V	Max value at $I_{OL} = +6.0$ mA for driver class A
		0.00	0.20	V	Max value at $I_{OL} = +0.1$ mA for driver class B
		0.00	0.35	V	Max value at $I_{OL} = +4.0$ mA for driver class B
		0.00	0.20	V	Max value at $I_{OL} = +0.1$ mA for driver class C
		0.00	0.35	V	Max value at $I_{OL} = +2.0$ mA for driver class C
		0.00	0.45	V	Max value at $I_{OL} = +2.0$ mA for driver class C_0
		0.00	0.20	V	Max value at $I_{OL} = +0.1$ mA for driver class D
		0.00	0.35	V	Max value at $I_{OL} = +1.0$ mA for driver class D
		0.00	0.20	V	Max value at $I_{OL} = +0.1$ mA for driver class E
Output characteristics: H-level output	1.45	1.80		V	Min value at $I_{OH} = -6.0$ mA for driver class A
	1.60	1.80		V	Min value at $I_{OH} = -0.1$ mA for driver class A
	1.45	1.80		V	Min value at $I_{OH} = -4.0$ mA for driver class B
	1.60	1.80		V	Min value at $I_{OH} = -0.1$ mA for driver class B
	1.45	1.80		V	Min value at $I_{OH} = -2.0$ mA for driver class C
	1.60	1.80		V	Min value at $I_{OH} = -0.1$ mA for driver class C
	1.35	1.80		V	Min value at $I_{OH} = -2.0$ mA for driver class C_0
	1.45	1.80		V	Min value at $I_{OH} = -1.0$ mA for driver class D
	1.60	1.80		V	Min value at $I_{OH} = -0.1$ mA for driver class D
Pull-up input current			0.7	μ A	$0.2 \text{ V} < V_{IN} < 1.93 \text{ V}$
			-240	μ A	PU Class a
			-150	μ A	PU Class b
Pull-down input current			-125	μ A	PU Class c
			+200	μ A	PD Class a
			+150	μ A	PD Class b
			+45	μ A	PD Class c

Table 20: Generic Digital Interfaces pins characteristics (GDI domain)

4.2.9.1 AC characteristics of digital audio interfaces pins

The 4-wire I²S digital audio interfaces can be configured in 4 different modes:

- Normal I²S mode – Master mode
- Normal I²S mode – Slave mode
- PCM mode – Master mode
- PCM mode – Slave mode

AC characteristics of the 4 different modes of the I²S digital audio interfaces are reported as follows.

Normal I²S mode – Master mode

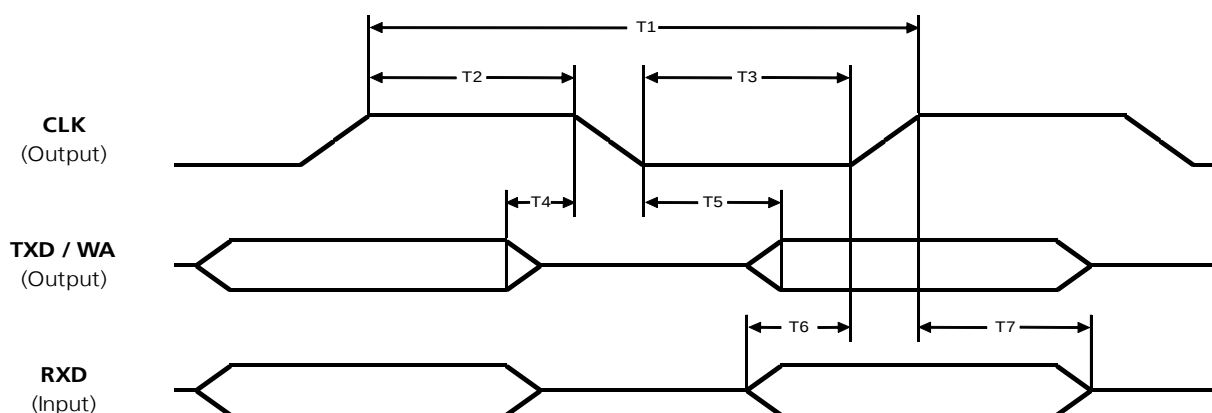


Figure 3: AC characteristics of digital audio interface in Normal I²S mode (<I2S_mode> = 2,4,6,8,10,12) and Master mode enabled

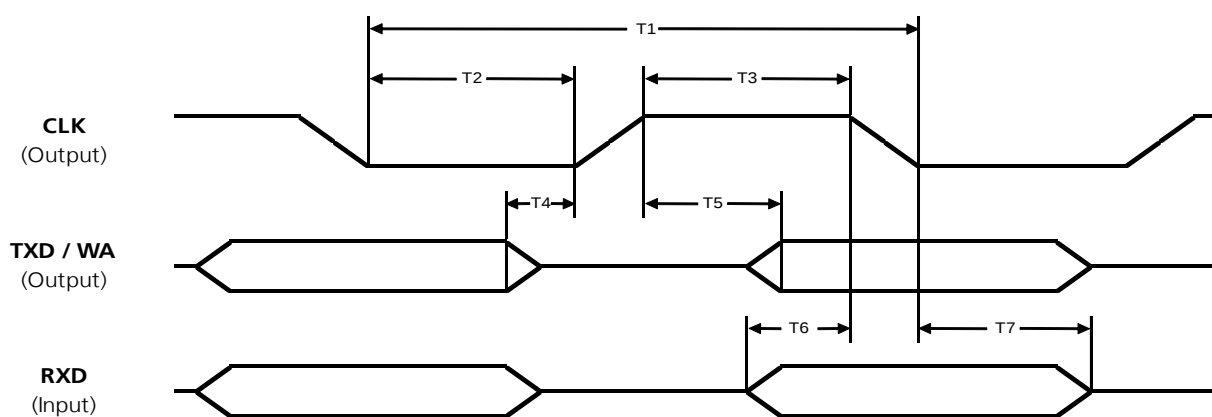


Figure 4: AC characteristics of digital audio interface in Normal I²S mode (<I2S_mode> = 3,5,7,9,11,13) and Master mode enabled

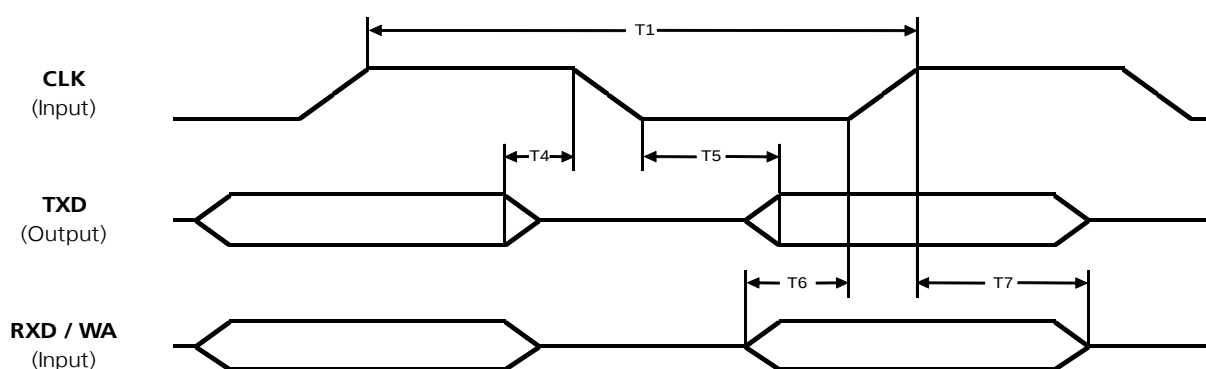
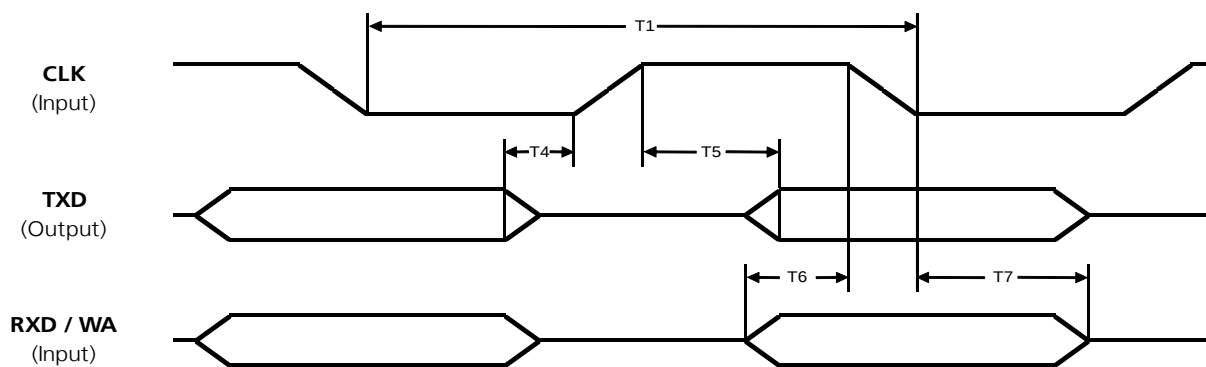
Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T1	I ² S clock period	3.902	3.906		μs	<I2S_sample_rate>=0
		2.830	2.834		μs	<I2S_sample_rate>=1
		2.600	2.604		μs	<I2S_sample_rate>=2
		1.949	1.953		μs	<I2S_sample_rate>=3
		1.413	1.417		μs	<I2S_sample_rate>=4
		1.298	1.302		μs	<I2S_sample_rate>=5
		0.973	0.977		μs	<I2S_sample_rate>=6
		0.705	0.709		μs	<I2S_sample_rate>=7
		0.647	0.651		μs	<I2S_sample_rate>=8
1/T1	I ² S clock frequency		256.0	256.3	kHz	<I2S_sample_rate>=0
			352.8	353.3	kHz	<I2S_sample_rate>=1
			384.0	384.6	kHz	<I2S_sample_rate>=2
			512.0	513.1	kHz	<I2S_sample_rate>=3
			705.6	707.6	kHz	<I2S_sample_rate>=4
			768.0	770.4	kHz	<I2S_sample_rate>=5

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T2	I ² S clock high time		1024	1028	kHz	<I2S_sample_rate>=6
			1411	1419	kHz	<I2S_sample_rate>=7
			1536	1545	kHz	<I2S_sample_rate>=8
		1.933	1.953		µs	<I2S_sample_rate>=0
		1.397	1.417		µs	<I2S_sample_rate>=1
		1.282	1.302		µs	<I2S_sample_rate>=2
		0.957	0.977		µs	<I2S_sample_rate>=3
		0.689	0.709		µs	<I2S_sample_rate>=4
		0.631	0.651		µs	<I2S_sample_rate>=5
T3	I ² S clock low time				µs	<I2S_sample_rate>=6
					µs	<I2S_sample_rate>=7
					µs	<I2S_sample_rate>=8
		1.933	1.953		µs	<I2S_sample_rate>=0
		1.397	1.417		µs	<I2S_sample_rate>=1
		1.282	1.302		µs	<I2S_sample_rate>=2
		0.957	0.977		µs	<I2S_sample_rate>=3
		0.689	0.709		µs	<I2S_sample_rate>=4
		0.631	0.651		µs	<I2S_sample_rate>=5
	I ² S word alignment period				µs	<I2S_sample_rate>=6
					µs	<I2S_sample_rate>=7
					µs	<I2S_sample_rate>=8
			125.0		µs	<I2S_sample_rate>=0
			90.70		µs	<I2S_sample_rate>=1
			83.33		µs	<I2S_sample_rate>=2
			62.50		µs	<I2S_sample_rate>=3
			45.35		µs	<I2S_sample_rate>=4
			41.67		µs	<I2S_sample_rate>=5
	I ² S word alignment frequency				µs	<I2S_sample_rate>=6
					µs	<I2S_sample_rate>=7
					µs	<I2S_sample_rate>=8
			8.000		kHz	<I2S_sample_rate>=0
			11.03		kHz	<I2S_sample_rate>=1
			12.00		kHz	<I2S_sample_rate>=2
			16.00		kHz	<I2S_sample_rate>=3
			22.05		kHz	<I2S_sample_rate>=4
			24.00		kHz	<I2S_sample_rate>=5
T4	I ² S TXD setup time before I ² S CLK high end (before shifting edge of I ² S CLK)				kHz	<I2S_sample_rate>=6
					kHz	<I2S_sample_rate>=7
					kHz	<I2S_sample_rate>=8
T5	I ² S TXD invalid before I ² S CLK low end (before shifting edge of I ² S CLK)			24	ns	<I2S_mode> = 2,4,6,8,10,12
				24	ns	<I2S_mode> = 3,5,7,9,11,13
				32	ns	<I2S_mode> = 2,4,6,8,10,12
T6	I ² S TXD valid after I ² S CLK low begin (after shifting edge of I ² S CLK)			32	ns	<I2S_mode> = 3,5,7,9,11,13
				32	ns	<I2S_mode> = 2,4,6,8,10,12
				32	ns	<I2S_mode> = 3,5,7,9,11,13
T7	I ² S RXD setup time before I ² S CLK low end (before latching edge of I ² S CLK)	60			ns	<I2S_mode> = 2,4,6,8,10,12
		60			ns	<I2S_mode> = 3,5,7,9,11,13

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T7	I ² S RXD hold time after I ² S CLK high begin (after latching edge of I ² S CLK)	10			ns	<I2S_mode> = 2,4,6,8,10,12
	I ² S RXD hold time after I ² S CLK low begin (after latching edge of I ² S CLK)	10			ns	<I2S_mode> = 3,5,7,9,11,13

Table 21: AC characteristics of digital audio interface in Normal I²S mode and Master mode enabled

Normal I²S mode – Slave mode


Figure 5: AC characteristics of digital audio interface in Normal I²S mode (<I2S_mode> = 2,4,6,8,10,12) and Slave mode enabled

Figure 6: AC characteristics of digital audio interface in Normal I²S mode (<I2S_mode> = 3,5,7,9,11,13) and Slave mode enabled

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T1	I ² S clock period	3.906			μs	<I2S_sample_rate>=0
		2.834			μs	<I2S_sample_rate>=1
		2.604			μs	<I2S_sample_rate>=2
		1.953			μs	<I2S_sample_rate>=3
		1.417			μs	<I2S_sample_rate>=4
		1.302			μs	<I2S_sample_rate>=5
		0.977			μs	<I2S_sample_rate>=6
		0.709			μs	<I2S_sample_rate>=7
		0.651			μs	<I2S_sample_rate>=8

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
1/T1	I ² S clock frequency			256.0	kHz	<I2S_sample_rate>=0
				352.8	kHz	<I2S_sample_rate>=1
				384.0	kHz	<I2S_sample_rate>=2
				512.0	kHz	<I2S_sample_rate>=3
				705.6	kHz	<I2S_sample_rate>=4
				768.0	kHz	<I2S_sample_rate>=5
				1024	kHz	<I2S_sample_rate>=6
				1411	kHz	<I2S_sample_rate>=7
				1536	kHz	<I2S_sample_rate>=8
	I ² S word alignment period	125.0			μs	<I2S_sample_rate>=0
		90.70			μs	<I2S_sample_rate>=1
		83.33			μs	<I2S_sample_rate>=2
		62.50			μs	<I2S_sample_rate>=3
		45.35			μs	<I2S_sample_rate>=4
		41.67			μs	<I2S_sample_rate>=5
		31.25			μs	<I2S_sample_rate>=6
		22.68			μs	<I2S_sample_rate>=7
		20.83			μs	<I2S_sample_rate>=8
	I ² S word alignment frequency			8.000	kHz	<I2S_sample_rate>=0
				11.03	kHz	<I2S_sample_rate>=1
				12.00	kHz	<I2S_sample_rate>=2
				16.00	kHz	<I2S_sample_rate>=3
				22.05	kHz	<I2S_sample_rate>=4
				24.00	kHz	<I2S_sample_rate>=5
				32.00	kHz	<I2S_sample_rate>=6
				44.10	kHz	<I2S_sample_rate>=7
				48.00	kHz	<I2S_sample_rate>=8
T4	I ² S TXD invalid before I ² S CLK falling edge (before shifting edge of I ² S CLK)			24	ns	<I2S_mode> = 2,4,6,8,10,12
	I ² S TXD invalid before I ² S CLK rising edge (before shifting edge of I ² S CLK)			24	ns	<I2S_mode> = 3,5,7,9,11,13
T5	I ² S TXD valid after I ² S CLK falling edge (after shifting edge of I ² S CLK)			32	ns	<I2S_mode> = 2,4,6,8,10,12
	I ² S TXD valid after I ² S CLK rising edge (after shifting edge of I ² S CLK)			32	ns	<I2S_mode> = 3,5,7,9,11,13
T6	I ² S RXD setup time before I ² S CLK rising edge (before latching edge of I ² S CLK)	60			ns	<I2S_mode> = 2,4,6,8,10,12
	I ² S RXD setup time before I ² S CLK falling edge (before latching edge of I ² S CLK)	60			ns	<I2S_mode> = 3,5,7,9,11,13
T7	I ² S RXD hold time after I ² S CLK rising edge (after latching edge of I ² S CLK)	10			ns	<I2S_mode> = 2,4,6,8,10,12
	I ² S RXD hold time after I ² S CLK falling edge (after latching edge of I ² S CLK)	10			ns	<I2S_mode> = 3,5,7,9,11,13

Table 22: AC characteristics of digital audio interface in Normal I²S mode and Slave mode enabled

PCM mode – Master mode

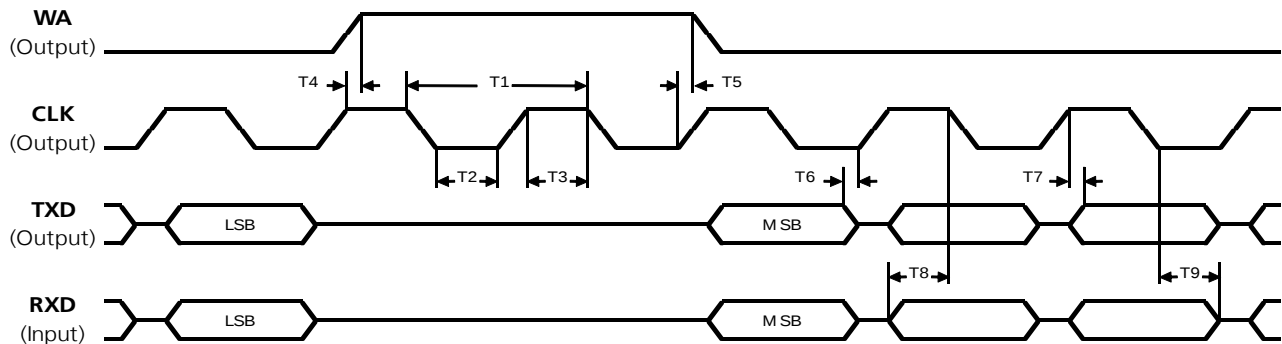


Figure 7: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 0) and Master mode enabled

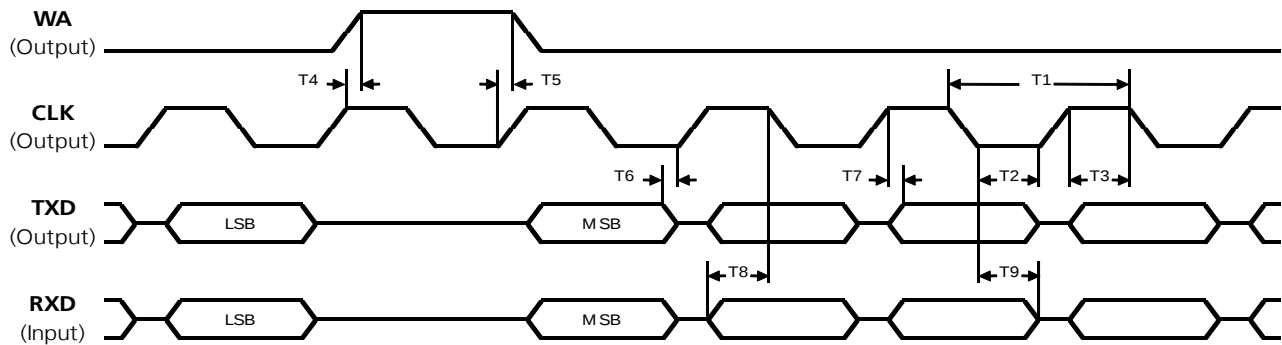


Figure 8: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 1) and Master mode enabled

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T1	I ² S clock period	6.940	6.944		μs	<I2S_mode>=0, <I2S_sample_rate>=0
		7.349	7.353		μs	<I2S_mode>=1, <I2S_sample_rate>=0
		5.035	5.039		μs	<I2S_mode>=0, <I2S_sample_rate>=1
		5.331	5.335		μs	<I2S_mode>=1, <I2S_sample_rate>=1
		4.626	4.630		μs	<I2S_mode>=0, <I2S_sample_rate>=2
		4.898	4.902		μs	<I2S_mode>=1, <I2S_sample_rate>=2
		3.468	3.472		μs	<I2S_mode>=0, <I2S_sample_rate>=3
		3.672	3.676		μs	<I2S_mode>=1, <I2S_sample_rate>=3
		2.516	2.520		μs	<I2S_mode>=0, <I2S_sample_rate>=4
		2.664	2.668		μs	<I2S_mode>=1, <I2S_sample_rate>=4
		2.311	2.315		μs	<I2S_mode>=0, <I2S_sample_rate>=5
		2.447	2.451		μs	<I2S_mode>=1, <I2S_sample_rate>=5
		1.732	1.736		μs	<I2S_mode>=0, <I2S_sample_rate>=6
		1.834	1.838		μs	<I2S_mode>=1, <I2S_sample_rate>=6
		1.256	1.260		μs	<I2S_mode>=0, <I2S_sample_rate>=7
		1.330	1.334		μs	<I2S_mode>=1, <I2S_sample_rate>=7
1/T1	I ² S clock frequency	1.153	1.157		μs	<I2S_mode>=0, <I2S_sample_rate>=8
		1.221	1.225		μs	<I2S_mode>=1, <I2S_sample_rate>=8
		144.0	144.1		kHz	<I2S_mode>=0, <I2S_sample_rate>=0
		136.0	136.1		kHz	<I2S_mode>=1, <I2S_sample_rate>=0

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
			198.5	198.6	kHz	<I2S_mode>=0, <I2S_sample_rate>=1
			187.4	187.6	kHz	<I2S_mode>=1, <I2S_sample_rate>=1
			216.0	216.2	kHz	<I2S_mode>=0, <I2S_sample_rate>=2
			204.0	204.2	kHz	<I2S_mode>=1, <I2S_sample_rate>=2
			288.0	288.3	kHz	<I2S_mode>=0, <I2S_sample_rate>=3
			272.0	272.3	kHz	<I2S_mode>=1, <I2S_sample_rate>=3
			396.9	397.5	kHz	<I2S_mode>=0, <I2S_sample_rate>=4
			374.9	375.4	kHz	<I2S_mode>=1, <I2S_sample_rate>=4
			432.0	432.7	kHz	<I2S_mode>=0, <I2S_sample_rate>=5
			408.0	408.7	kHz	<I2S_mode>=1, <I2S_sample_rate>=5
			576.0	577.3	kHz	<I2S_mode>=0, <I2S_sample_rate>=6
			544.0	545.2	kHz	<I2S_mode>=1, <I2S_sample_rate>=6
			793.8	796.3	kHz	<I2S_mode>=0, <I2S_sample_rate>=7
			749.7	752.0	kHz	<I2S_mode>=1, <I2S_sample_rate>=7
			864.0	867.0	kHz	<I2S_mode>=0, <I2S_sample_rate>=8
			816.0	818.7	kHz	<I2S_mode>=1, <I2S_sample_rate>=8
T2	I ² S clock low time	3.452	3.472		μs	<I2S_mode>=0, <I2S_sample_rate>=0
		3.656	3.676		μs	<I2S_mode>=1, <I2S_sample_rate>=0
		2.500	2.520		μs	<I2S_mode>=0, <I2S_sample_rate>=1
		2.648	2.668		μs	<I2S_mode>=1, <I2S_sample_rate>=1
		2.295	2.315		μs	<I2S_mode>=0, <I2S_sample_rate>=2
		2.431	2.451		μs	<I2S_mode>=1, <I2S_sample_rate>=2
		1.716	1.736		μs	<I2S_mode>=0, <I2S_sample_rate>=3
		1.818	1.838		μs	<I2S_mode>=1, <I2S_sample_rate>=3
		1.240	1.260		μs	<I2S_mode>=0, <I2S_sample_rate>=4
		1.314	1.334		μs	<I2S_mode>=1, <I2S_sample_rate>=4
		1.137	1.157		μs	<I2S_mode>=0, <I2S_sample_rate>=5
		1.205	1.225		μs	<I2S_mode>=1, <I2S_sample_rate>=5
		0.848	0.868		μs	<I2S_mode>=0, <I2S_sample_rate>=6
		0.899	0.919		μs	<I2S_mode>=1, <I2S_sample_rate>=6
		0.610	0.630		μs	<I2S_mode>=0, <I2S_sample_rate>=7
		0.647	0.667		μs	<I2S_mode>=1, <I2S_sample_rate>=7
T3	I ² S clock high time	0.559	0.579		μs	<I2S_mode>=0, <I2S_sample_rate>=8
		0.593	0.613		μs	<I2S_mode>=1, <I2S_sample_rate>=8
		3.452	3.472		μs	<I2S_mode>=0, <I2S_sample_rate>=0
		3.656	3.676		μs	<I2S_mode>=1, <I2S_sample_rate>=0
		2.500	2.520		μs	<I2S_mode>=0, <I2S_sample_rate>=1
		2.648	2.668		μs	<I2S_mode>=1, <I2S_sample_rate>=1
		2.295	2.315		μs	<I2S_mode>=0, <I2S_sample_rate>=2
		2.431	2.451		μs	<I2S_mode>=1, <I2S_sample_rate>=2
		1.716	1.736		μs	<I2S_mode>=0, <I2S_sample_rate>=3
		1.818	1.838		μs	<I2S_mode>=1, <I2S_sample_rate>=3
		1.240	1.260		μs	<I2S_mode>=0, <I2S_sample_rate>=4
		1.314	1.334		μs	<I2S_mode>=1, <I2S_sample_rate>=4
		1.137	1.157		μs	<I2S_mode>=0, <I2S_sample_rate>=5
		1.205	1.225		μs	<I2S_mode>=1, <I2S_sample_rate>=5
		0.848	0.868		μs	<I2S_mode>=0, <I2S_sample_rate>=6
		0.899	0.919		μs	<I2S_mode>=1, <I2S_sample_rate>=6
		0.610	0.630		μs	<I2S_mode>=0, <I2S_sample_rate>=7
		0.647	0.667		μs	<I2S_mode>=1, <I2S_sample_rate>=7
		0.559	0.579		μs	<I2S_mode>=0, <I2S_sample_rate>=8
		0.593	0.613		μs	<I2S_mode>=1, <I2S_sample_rate>=8

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
	I ² S word alignment period		125.0		μs	<I2S_sample_rate>=0
			90.70		μs	<I2S_sample_rate>=1
			83.33		μs	<I2S_sample_rate>=2
			62.50		μs	<I2S_sample_rate>=3
			45.35		μs	<I2S_sample_rate>=4
			41.67		μs	<I2S_sample_rate>=5
			31.25		μs	<I2S_sample_rate>=6
			22.68		μs	<I2S_sample_rate>=7
	I ² S word alignment frequency		20.83		μs	<I2S_sample_rate>=8
			8.000		kHz	<I2S_sample_rate>=0
			11.03		kHz	<I2S_sample_rate>=1
			12.00		kHz	<I2S_sample_rate>=2
			16.00		kHz	<I2S_sample_rate>=3
			22.05		kHz	<I2S_sample_rate>=4
			24.00		kHz	<I2S_sample_rate>=5
			32.00		kHz	<I2S_sample_rate>=6
			44.10		kHz	<I2S_sample_rate>=7
			48.00		kHz	<I2S_sample_rate>=8
T4	I ² S CLK high begin to I ² S WA high begin	-24		32	ns	<I2S_mode> = 0
T5	I ² S CLK low end to I ² S WA high end	-24		32	ns	<I2S_mode> = 0
T6	I ² S TXD invalid before I ² S CLK low end			24	ns	<I2S_mode> = 0
T7	I ² S TXD valid after I ² S CLK high begin			22	ns	<I2S_mode> = 0
T8	I ² S RXD setup time before I ² S CLK high end	60			ns	<I2S_mode> = 0
T9	I ² S RXD hold time after I ² S CLK low begin	12			ns	<I2S_mode> = 0

Table 23: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 0,1) and Master mode enabled

PCM mode – Slave mode

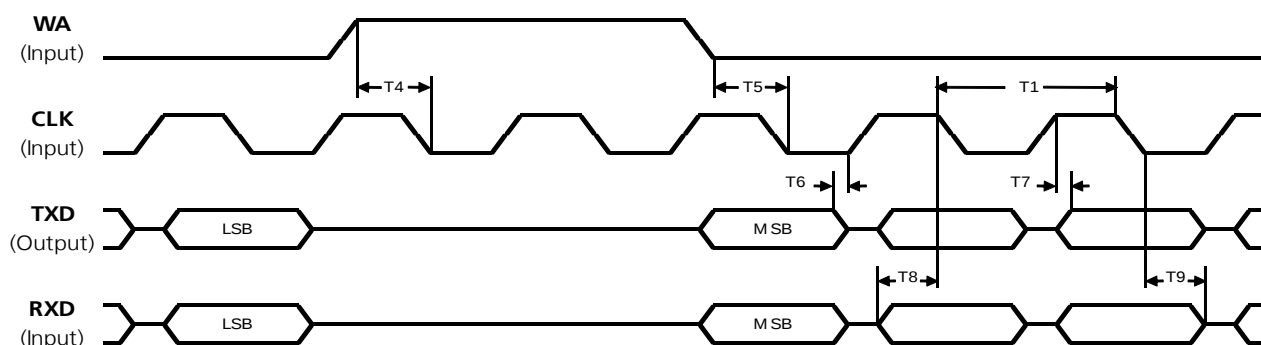


Figure 9: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 0) and Slave mode enabled

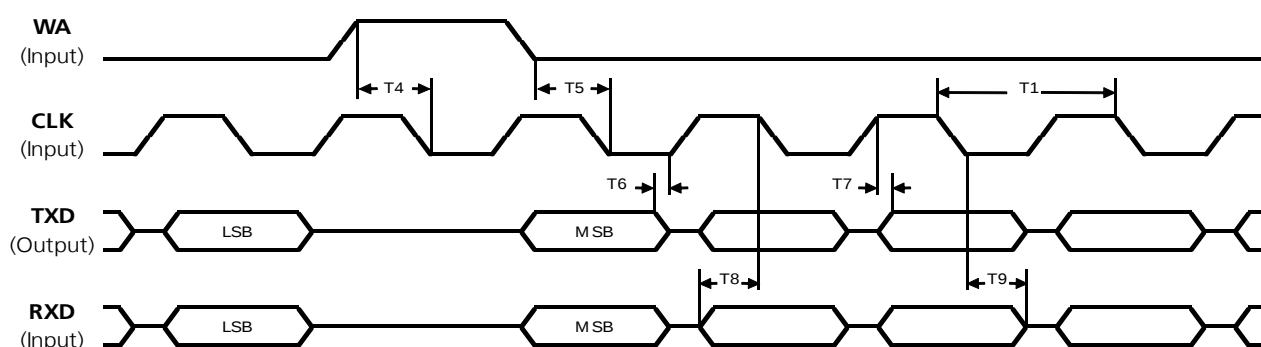


Figure 10: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 1) and Slave mode enabled

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T1	I ² S clock period	6.944			μs	<I2S_mode>=0, <I2S_sample_rate>=0
		7.353			μs	<I2S_mode>=1, <I2S_sample_rate>=0
		5.039			μs	<I2S_mode>=0, <I2S_sample_rate>=1
		5.335			μs	<I2S_mode>=1, <I2S_sample_rate>=1
		4.630			μs	<I2S_mode>=0, <I2S_sample_rate>=2
		4.902			μs	<I2S_mode>=1, <I2S_sample_rate>=2
		3.472			μs	<I2S_mode>=0, <I2S_sample_rate>=3
		3.676			μs	<I2S_mode>=1, <I2S_sample_rate>=3
		2.520			μs	<I2S_mode>=0, <I2S_sample_rate>=4
		2.668			μs	<I2S_mode>=1, <I2S_sample_rate>=4
		2.315			μs	<I2S_mode>=0, <I2S_sample_rate>=5
		2.451			μs	<I2S_mode>=1, <I2S_sample_rate>=5
		1.736			μs	<I2S_mode>=0, <I2S_sample_rate>=6
		1.838			μs	<I2S_mode>=1, <I2S_sample_rate>=6
		1.260			μs	<I2S_mode>=0, <I2S_sample_rate>=7
		1.334			μs	<I2S_mode>=1, <I2S_sample_rate>=7
		1.157			μs	<I2S_mode>=0, <I2S_sample_rate>=8
		1.225			μs	<I2S_mode>=1, <I2S_sample_rate>=8

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
1/T1	I ² S clock frequency	144.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=0
		136.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=0
		198.5			kHz	<I2S_mode>=0, <I2S_sample_rate>=1
		187.4			kHz	<I2S_mode>=1, <I2S_sample_rate>=1
		216.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=2
		204.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=2
		288.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=3
		272.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=3
		396.9			kHz	<I2S_mode>=0, <I2S_sample_rate>=4
		374.9			kHz	<I2S_mode>=1, <I2S_sample_rate>=4
		432.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=5
		408.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=5
		576.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=6
		544.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=6
		793.8			kHz	<I2S_mode>=0, <I2S_sample_rate>=7
		749.7			kHz	<I2S_mode>=1, <I2S_sample_rate>=7
		864.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=8
		816.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=8
	I ² S word alignment period		125.0		µs	<I2S_sample_rate>=0
			90.70		µs	<I2S_sample_rate>=1
			83.33		µs	<I2S_sample_rate>=2
			62.50		µs	<I2S_sample_rate>=3
			45.35		µs	<I2S_sample_rate>=4
			41.67		µs	<I2S_sample_rate>=5
			31.25		µs	<I2S_sample_rate>=6
			22.68		µs	<I2S_sample_rate>=7
			20.83		µs	<I2S_sample_rate>=8
	I ² S word alignment frequency		8.000		kHz	<I2S_sample_rate>=0
			11.03		kHz	<I2S_sample_rate>=1
			12.00		kHz	<I2S_sample_rate>=2
			16.00		kHz	<I2S_sample_rate>=3
			22.05		kHz	<I2S_sample_rate>=4
			24.00		kHz	<I2S_sample_rate>=5
			32.00		kHz	<I2S_sample_rate>=6
			44.10		kHz	<I2S_sample_rate>=7
			48.00		kHz	<I2S_sample_rate>=8
T4	I ² S WA high begin before I ² S CLK low begin (latching edge of I ² S CLK)	36			ns	<I2S_mode> = 0
T5	I ² S WA low begin before I ² S CLK low begin (latching edge of I ² S CLK)	36			ns	<I2S_mode> = 0
T6	I ² S TXD invalid before I ² S CLK rising edge (shifting edge of I ² S CLK)			12	ns	<I2S_mode> = 0
T7	I ² S TXD valid after I ² S CLK rising edge (shifting edge of I ² S CLK)			79	ns	<I2S_mode> = 0
T8	I ² S RXD setup time before I ² S CLK falling edge (latching edge of I ² S CLK)	22			ns	<I2S_mode> = 0
T9	I ² S RXD hold time after I ² S CLK falling edge (latching edge of I ² S CLK)	24			ns	<I2S_mode> = 0

Table 24: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 0,1) and Slave mode enabled

4.2.9.2 AC characteristics of Digital Clock Output pin

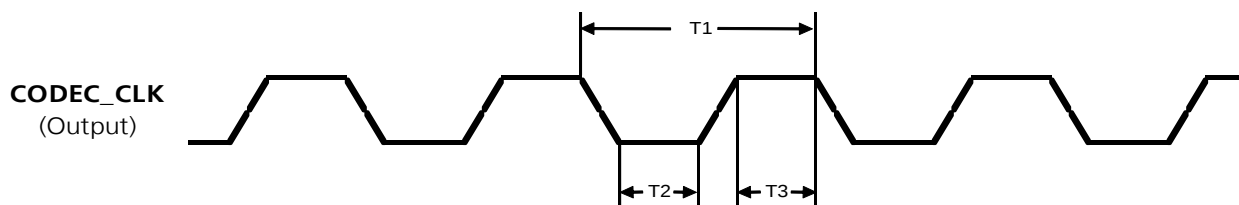


Figure 11: AC characteristics of CODEC_CLK digital clock output

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T1	CODEC_CLK clock period		38		ns	CODEC_CLK output set to 26 MHz
			77		ns	CODEC_CLK output set to 13 MHz
1/T1	CODEC_CLK clock frequency		26		MHz	CODEC_CLK output set to 26 MHz
			13		MHz	CODEC_CLK output set to 13 MHz
T2	CODEC_CLK clock low time	10			ns	CODEC_CLK output set to 26 MHz
		26			ns	CODEC_CLK output set to 13 MHz
T3	CODEC_CLK clock high time	10			ns	CODEC_CLK output set to 26 MHz
		26			ns	CODEC_CLK output set to 13 MHz

Table 25: AC characteristics of CODEC_CLK digital clock output

4.2.9.3 AC characteristics of SPI / IPC pins

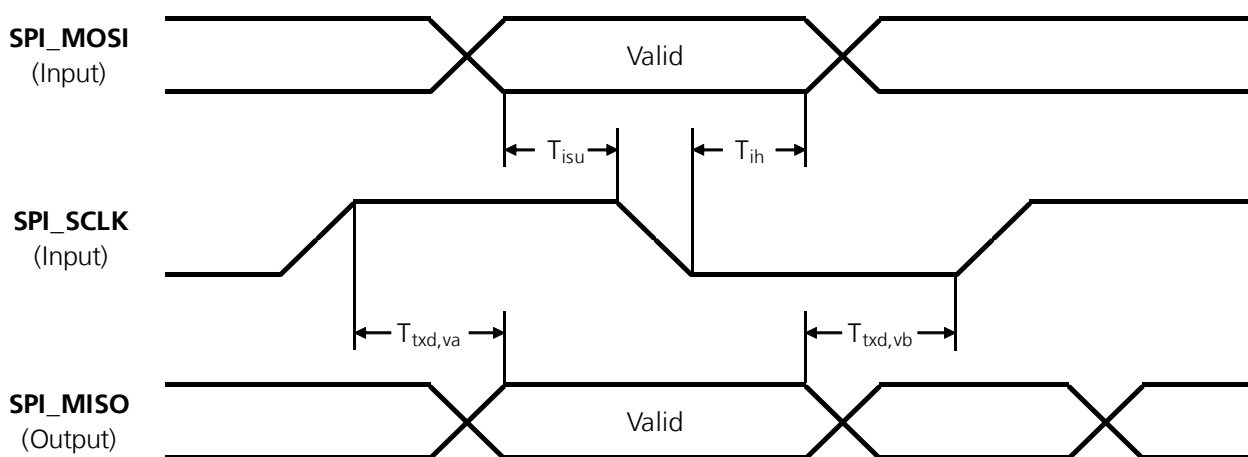


Figure 12: SPI_MOSI, SPI_MISO, SPI_SCLK timings

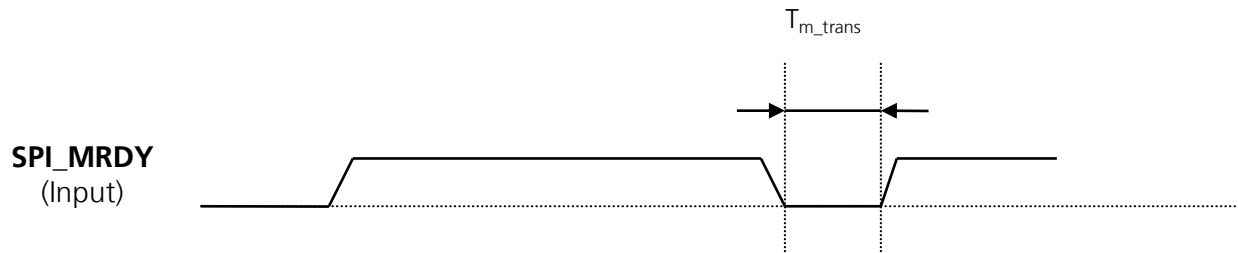


Figure 13: SPI_MRDY transition

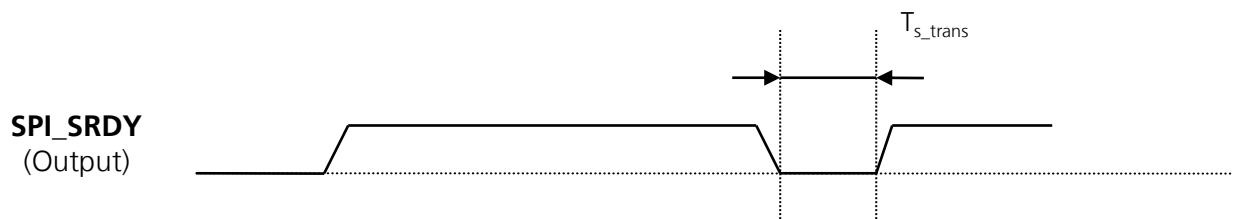


Figure 14: SPI_SRDY transition

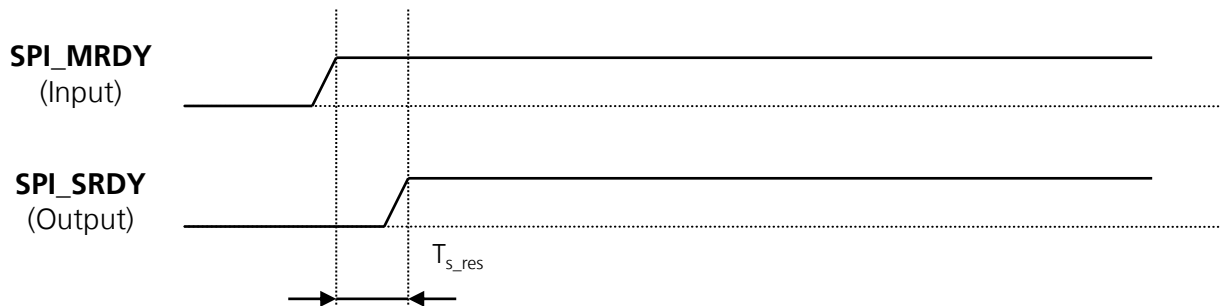


Figure 15: SPI_SRDY response

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
	SPI_SCLK frequency	0.26		26.0	MHz	
	SPI_SCLK period	38.5		3846.2	ns	
T_{isu}	Receive data setup time	5			ns	
T_{ih}	Receive data hold time	5			ns	
$T_{txd,va}$	Transmit data valid after clock rising edge			13	ns	
$T_{txd,vb}$	Transmit data valid before clock rising edge			0	ns	
$T_{m,trans}$	Time between two master data transfers	80			ns	Power saving disabled by AT+UPSV
		62			μs	Power saving enabled by AT+UPSV
$T_{s,trans}$	Time between two slave data transfers	80			ns	
$T_{s,res}$	SPI_SRDY active after SPI_MRDY active			200	μs	Power saving disabled by AT+UPSV
				10	ms	Power saving enabled by AT+UPSV

Table 26: AC characteristics of SPI interface

4.2.10 USB pins

USB data lines (**USB_D+** and **USB_D-**) are compliant to the USB 2.0 high-speed specification. Refer to the Universal Serial Bus Revision 2.0 specification [8] for detailed electrical characteristics.

Parameter	Min.	Typ.	Max.	Unit	Remarks
USB detection voltage on pin VUSB_DET	4.40	5.00	5.25	V	
Current sink at VUSB_DET		30		μA	
High-speed squelch detection threshold (input differential signal amplitude)	100		150	mV	
High speed disconnect detection threshold (input differential signal amplitude)	525		625	mV	
High-speed data signaling input common mode voltage range	-50		500	mV	
High-speed idle output level	-10		10	mV	
High-speed data signaling output high level	360		440	mV	
High-speed data signaling output low level	-10		10	mV	
Chirp J level (output differential voltage)	700		1100	mV	
Chirp K level (output differential voltage)	-900		-500	mV	

Table 27: USB pins characteristics

4.2.11 DDC (I²C) pins

DDC (I²C) lines (**SCL** and **SDA**) are compliant to the I²C-bus standard mode specification. Refer to the I²C-Bus Specification Version 2.1 [9] for detailed electrical characteristics.

Parameter	Min.	Typ.	Max.	Unit	Remarks
Internal supply for DDC domain	1.73	1.80	1.87	V	Digital I/O Interfaces supply (V_INT)
L-level input	-0.20		0.35	V	
H-level input	1.31		1.93	V	
L-level output		0.00	0.35	V	Max value at I _{OL} = +1.0 mA
Input/Output leakage current			0.7	μA	0.2 V < V _{IN} < 1.93 V
Clock frequency on SCL		100		kHz	

Table 28: DDC (I²C) pins characteristics (DDC domain)

5 Mechanical specifications

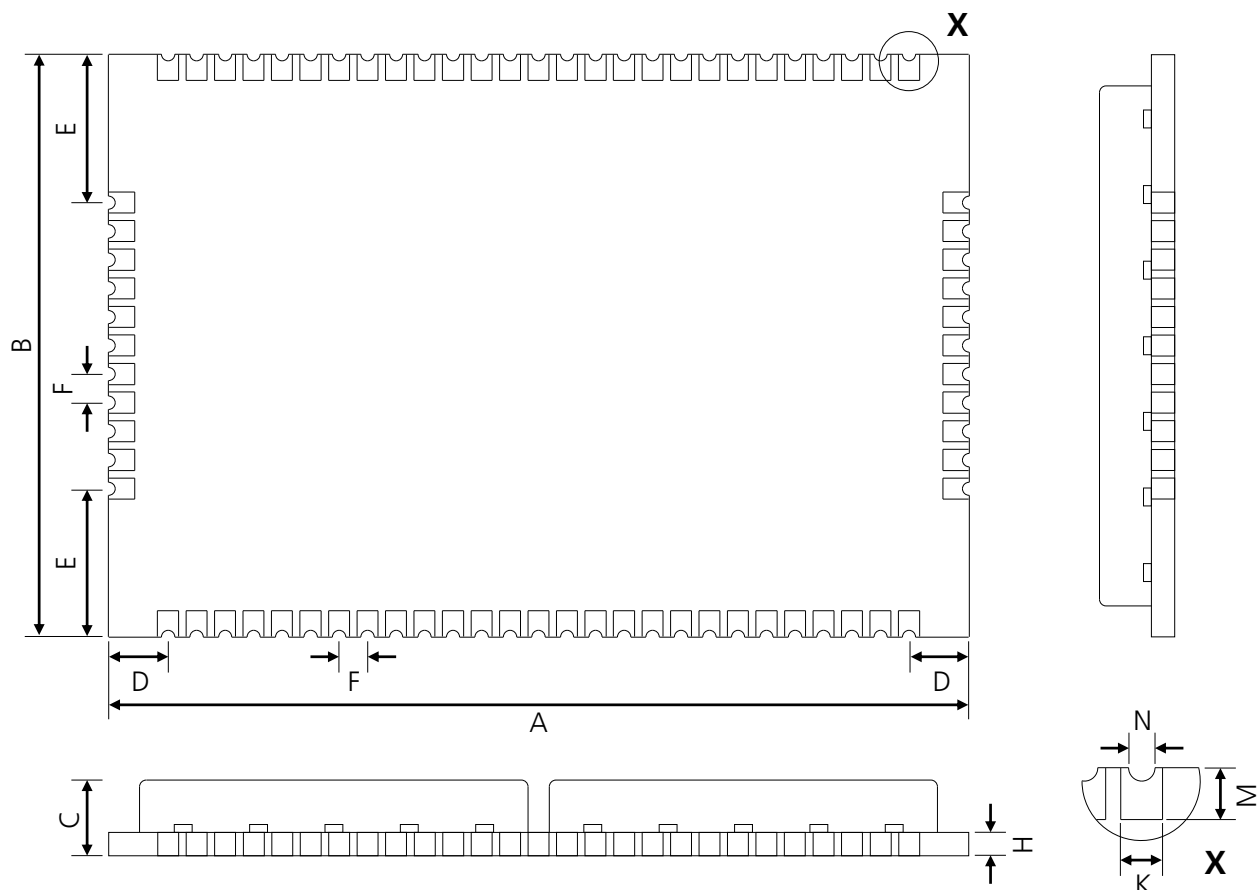


Figure 16: Dimensions (LISA-U2 series bottom and sides views)

Parameter	Description	Typical		Tolerance	
A	Module Height [mm]	33.2	(1307.1 mil)	+0.20/-0.20	(+7.9/-7.9 mil)
B	Module Width [mm]	22.4	(881.9 mil)	+0.20/-0.20	(+7.9/-7.9 mil)
C	Module Total Thickness [mm]	2.6	(102.4 mil)	+0.27/-0.17	(+10.6/-6.7 mil)
D	Horizontal Edge to Pin Pitch [mm]	2.3	(90.6 mil)	+0.20/-0.20	(+7.9/-7.9 mil)
E	Vertical Edge to Pin Pitch [mm]	5.7	(224.4 mil)	+0.20/-0.20	(+7.9/-7.9 mil)
F	Pin to Pin Pitch [mm]	1.1	(43.3 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
K	Pad width [mm]	0.8	(31.5 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
M	Pad height [mm]	1.0	(39.4 mil)	+0.10/-0.10	(+3.9/-3.9 mil)
N	Pad half-moon diameter [mm]	0.5	(19.7 mil)	+0.10/-0.10	(+3.9/-3.9 mil)
Weight	Module Weight [g]	< 5			

Note: the values in mil have been calculated from the relative values in mm.

Table 29: Dimensions



For information regarding Footprint and Paste Mask see the LISA-U series System Integration Manual [6].

6 Reliability tests and approvals

6.1 Reliability tests

Qualifications according to ISO 16750 "Road vehicles - Environmental conditions and testing for electrical and electronic equipment".

6.2 Approvals



Products marked with this lead-free symbol on the product label comply with the "Directive 2002/95/EC of the European Parliament and the Council on the Restriction of Use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

LISA-U2 modules are RoHS compliant.

No natural rubbers, hygroscopic materials, or materials containing asbestos are employed.

Table 30 lists the LISA-U2 series main approvals.

Directive / Standard / Regulatory	LISA-U200	LISA-U230	LISA-U260	LISA-U270
GCF (Global Certification Forum)	•	•	•	•
PTCRB (PCS Type Certification Review Board)	•	•	•	•
R&TTE (Radio and Telecommunications Terminal Equipment EU Directive)	•	•	•	•
CE (Conformité Européenne)	CE NB ID: 0682	CE NB ID: 0682	CE NB ID: 0682	CE NB ID: 0682
FCC (US Federal Communications Commission)	FCC ID: XPYLISAU200	FCC ID: XPYLISAU230	FCC ID: XPYLISAU200	FCC ID: XPYLISAU200
IC (Industry Canada)	IC ID: 8595A-LISAU200	IC ID: 8595A-LISAU230	IC ID: 8595A-LISAU200	IC ID: 8595A-LISAU200

Table 30: LISA-U2 series main certification approvals

For the complete list of countries and network operators approvals, refer to our website www.u-blox.com.

7 Product handling & soldering

7.1 Packaging

LISA-U2 modules are delivered as hermetically sealed, reeled tapes to enable efficient production, production lot set-up and tear-down. For more information about packaging, see the u-blox Package Information Guide [11].



Figure 17: Reeled LISA-U2 modules

7.1.1 Reels

LISA-U2 modules are deliverable in quantities of 150 pieces on a reel. LISA-U2 modules are delivered using reel Type B as described in the u-blox Package Information Guide [11].

Parameter	Specification
Reel Type	B
Delivery Quantity	150

Table 31: Reel information for LISA-U2 modules



Quantities of less than 150 pieces are also available. Contact u-blox for more information.

7.1.2 Tapes

Figure 18 shows the position and orientation of LISA-U2 modules as they are delivered on tape. The dimensions of the tapes are specified in Figure 19.

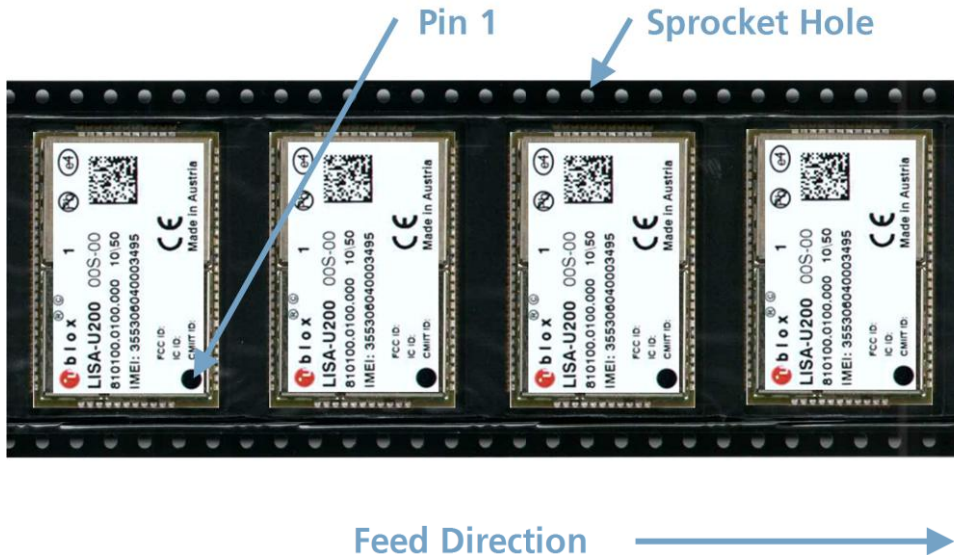


Figure 18: Orientation for LISA-U2 modules on tape

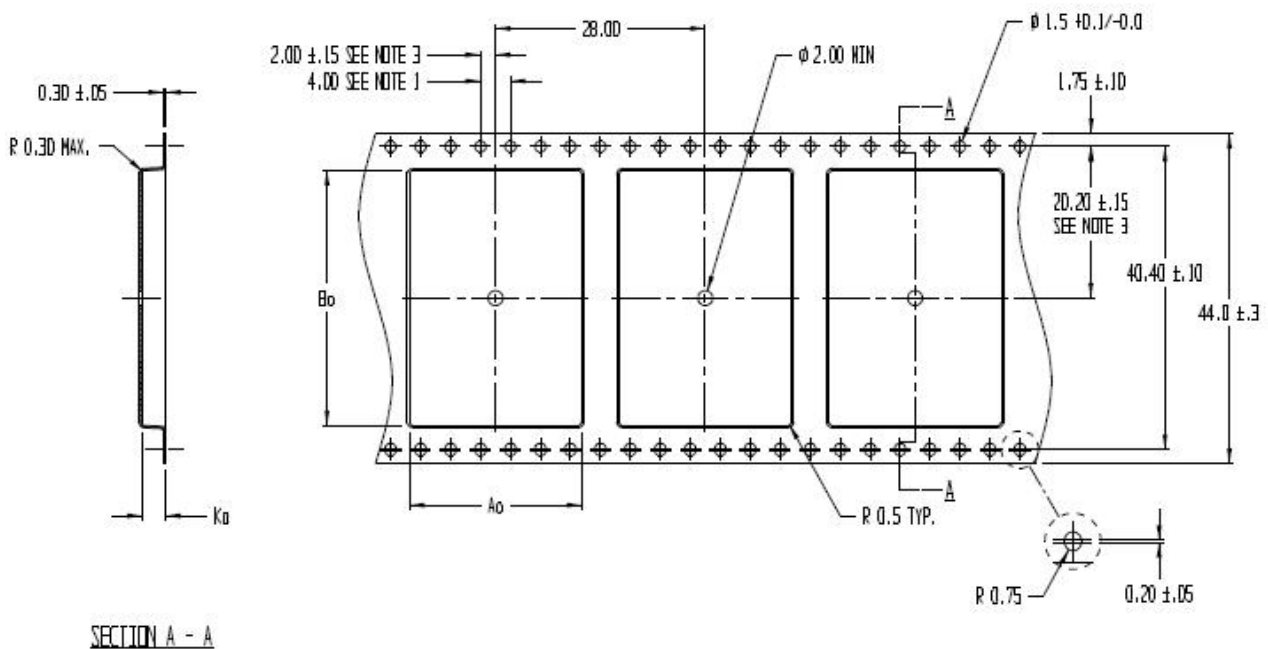


Figure 19: LISA-U2 series tape dimensions (mm)

Parameter	Value
A ₀	23.0
B ₀	34.0
K ₀	3.2

Table 32: LISA-U2 series tape dimensions (mm)



Note 1: 10 sprocket hole pitch cumulative tolerance ± 0.2 .



Note 2: the camber is compliant with EIA 481.



Note 3: the pocket position relative to sprocket hole is measured as true position of pocket, not pocket hole.



Note 4: A_0 and B_0 are calculated on a plane at a distance "R" above the bottom of the pocket.

7.2 Moisture Sensitivity Levels



LISA-U2 modules are Moisture Sensitive Devices (MSD) in accordance to the IPC/JEDEC specification.

The Moisture Sensitivity Level (MSL) relates to the packaging and handling precautions required. LISA-U2 modules are rated at MSL level 4. For more information regarding moisture sensitivity levels, labeling, storage and drying see the u-blox Package Information Guide [11].



For MSL standard see IPC/JEDEC J-STD-020 (can be downloaded from www.jedec.org).

7.3 Reflow soldering

Reflow profiles are to be selected according to u-blox recommendations (see LISA-U series System Integration Manual [6]).



Failure to observe these recommendations can result in severe damage to the device!

7.4 ESD precautions



LISA-U2 modules contain highly sensitive electronic circuitry and are Electrostatic Sensitive Devices (ESD). Handling LISA-U2 modules without proper ESD protection may destroy or damage them permanently.

LISA-U2 modules are Electrostatic Sensitive Devices (ESD) and require special ESD precautions typically applied to ESD sensitive components.

Table 8 reports the maximum ESD ratings of the LISA-U2 module.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates LISA-U2 module.

ESD precautions should be implemented on the application board where the module is mounted, as described in the LISA-U series System Integration Manual [6].



Failure to observe these precautions can result in severe damage to the device!

8 Default settings

Interface	AT Settings	Comments
UART interface	Enabled	Multiplexing mode can be enabled by AT+CMUX command providing following channels: - Channel 0: control channel - Channel 1 – 5: AT commands / data connection - Channel 6: GPS tunneling All LISA-U2 modules versions except LISA-U200-00S provide an additional channel: - Channel 7: SAP (SIM Access Profile)
	AT+IPR=0	Autobauding enabled  On LISA-U200-00S version AT+IPR=115200.
	AT+ICF=3,1	Frame format: 8 bits, no parity, 1 stop bit  Where AT+IPR=0 is the default value, the +ICF value in the profile is not applied (+IPR=0 overrules the +ICF setting) and the automatic frame detection is active.
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode
	AT&D1	Upon an ON-to-OFF transition of DTR, the DCE enters online command state and issues an OK result code
	AT&C1	Circuit 109 changes in accordance with the Carrier detect status; ON if the Carrier is detected, OFF otherwise
USB interface	Enabled	6 CDCs are available, configured as described in the following list: - USB1: AT commands / data connection - USB2: AT commands / data connection - USB3: AT commands / data connection - USB4: GPS tunneling - USB5: Primary TraceLog (debug purpose) - USB6: Secondary TraceLog (debug purpose) All LISA-U2 modules versions except LISA-U200-00S provide an additional CDC: - USB7: SAP (SIM Access Profile)
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode
	AT&D1	Upon an ON-to-OFF transition of DTR, the DCE enters online command state and issues an OK result code
	AT&C1	Circuit 109 changes in accordance with the Carrier detect status; ON if the Carrier is detected, OFF otherwise
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode
	AT&D1	Upon an ON-to-OFF transition of DTR, the DCE enters online command state and issues an OK result code
SPI interface	Enabled	Multiplexing mode can be enabled by AT+CMUX command providing following channels: - Channel 0: control channel - Channel 1 – 5: AT commands / data connection - Channel 6: GPS tunneling All LISA-U2 modules versions except LISA-U200-00S provide an additional channel: - Channel 7: SAP (SIM Access Profile)
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode
	AT&D1	Upon an ON-to-OFF transition of DTR, the DCE enters online command state and issues an OK result code
	AT&C1	Circuit 109 changes in accordance with the Carrier detect status; ON if the Carrier is detected, OFF otherwise
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode
	AT&D1	Upon an ON-to-OFF transition of DTR, the DCE enters online command state and issues an OK result code
Power Saving	AT+UPSV=0	Disabled
Network registration	AT+COPS=0	Self network registration

Table 33: Default settings

Refer to the u-blox AT Commands Manual [5] and to the LISA-U series System Integration Manual [6] for information about further settings.

9 Labeling and ordering information

9.1 Product labeling

The label on u-blox modules includes important product information. The location of the product type number is shown in Figure 20.



Figure 20: Location of product type number on LISA-U2 module label

9.2 Explanation of codes

3 different product code formats are used. The **Product Name** is used in documentation such as this data sheet and identifies all u-blox products, independent of packaging and quality grade. The **Ordering Code** includes options and quality, while the **Type Number** includes the hardware and firmware versions. Table 34 details these 3 different formats:

Format	Structure
Product Name	LISA-CDVG
Ordering Code	LISA-CDVG-TTQ
Type Number	LISA-CDVG-TTQ-XX

Table 34: Product Code Formats

The parts of the product code are explained in Table 35.

Code	Meaning	Example
C	Cellular standard (i.e. G: GSM; E: EDGE; W: WEDGE; H: HSDPA; U: HSUPA; L: LTE; C: CDMA 1xRTT; D: EV-DO)	U: HSUPA
D	Generation, e.g. chip or function set; range[0...9]	2
V	Variant based on the same cellular chip range: [0...9]	
G	GPS/GNSS generation (if GPS/GNSS functionality available)	6 = u-blox 6, 0: no GPS/GNSS functionality
TT	Version	0
Q	Quality grade/production site - S = standard - A = automotive - B = standard / made in Brazil	S
XX		Default value is 00

Table 35: Part identification code

9.3 Ordering information

Ordering No.	Product
LISA-U200-00S	HSPA 800/850/1900/2100 MHz, quad-band GPRS/EDGE, data only, 33.2 x 22.4 x 2.6 mm, 150 pcs/reel
LISA-U200-01S	HSPA 800/850/900/1700/1900/2100 MHz, quad-band GPRS/EDGE, voice and data, 33.2 x 22.4 x 2.6 mm, 150 pcs/reel
LISA-U230-01S	HSPA 800/850/900/1700/1900/2100 MHz, quad-band GPRS/EDGE, voice and data, 33.2 x 22.4 x 2.6 mm, 150 pcs/reel
LISA-U260-01S	HSPA 850/1900 MHz, quad-band GPRS/EDGE, voice and data, 33.2 x 22.4 x 2.6 mm, 150 pcs/reel
LISA-U270-01S	HSPA 900/2100 MHz, quad-band GPRS/EDGE, voice and data, 33.2 x 22.4 x 2.6 mm, 150 pcs/reel

Table 36: Product ordering codes

Appendix

A Glossary

Name	Definition
BER	Bit Error Rate
DCE	Data Communication Equipment
DDC	Display Data Channel (I ² C compatible) Interface
DL	Down-link (Reception)
Driver Class	Output Driver Class: see Table 20 for definition
DRX	Discontinuous Reception
DTE	Data Terminal Equipment
EDGE	Enhanced Data rates for GSM Evolution
ERS	External Reset Input Signal
GDI	Generic Digital Interfaces (power domain)
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communication
H	High
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I ² C	Inter-Integrated Circuit Interface
I ² S	Inter-IC Sound Interface
L	Low
LCC	Leadless Chip Carrier
N/A	Not Applicable (used in the I/O field of pinout)
OD	Open Drain
PCN / IN	Product Change Notification / Information Note
PD	Pull-Down
POS	Power-On Input (power domain)
PU	Pull-Up
PU/PD Class	Pull Class: see Table 20 for definition
RMC	Reference Measurement Channel
SIM	SIM Interface (power domain)
SPI	Serial Peripheral Interface
T	Tristate (Output of the pin set to tri-state, i.e. high impedance state)
T/PD	Tristate with internal active Pull-Down enabled
T/PU	Tristate with internal active Pull-Up enabled
UART	Universal Asynchronous Receiver-Transmitter serial interface
UL	Up-link (Transmission)
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus (power domain)

Table 37: Explanation of abbreviations and terms used

Related documents

- [1] 3GPP TS 27.007 V3.13.0 - AT command set for User Equipment (UE) (Release 1999)
- [2] 3GPP TS 27.005 V3.2.0 (2002-06) - Use of Data Terminal Equipment - Data Circuit terminating; Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS) (Release 1999)
- [3] 3GPP TS 27.010 V3.4.0 - Terminal Equipment to User Equipment (TE-UE) multiplexer protocol (Release 1999)
- [4] ITU-T Recommendation V24, 02-2000. List of definitions for interchange circuits between Data Terminal Equipment (DTE) and Data Connection Equipment (DCE)
- [5] u-blox AT Commands Manual, Docu No WLS-SW-11000
- [6] LISA-U series System Integration Manual, Docu No 3G.G2-HW-10002
- [7] GSM Mux Implementation Application Note for wireless modules, Docu No WLS-CS-11002
- [8] Universal Serial Bus Revision 2.0 specification, <http://www.usb.org/developers/docs/>
- [9] I2C-Bus Specification Version 2.1 Philips Semiconductors (January 2000), http://www.nxp.com/acrobat_download/literature/9398/39340011_21.pdf
- [10] u-blox SPI Interface Application Note, Docu No 3G.G2-CS-11000
- [11] u-blox Package Information Guide, Docu No GPS-X-11004
- [12] GPS Implementation Application Note, Docu No GSM.G1-CS-09007



For regular updates to u-blox documentation and to receive product change notifications, register on our homepage.

Revision history

Revision	Date	Name	Status / Comments
-	Jul. 25, 2011	lpah	Initial release (draft)
1	Oct. 12, 2011	sses	First release for LISA-U200-00S, LISA-U200-01x, LISA-U230-01x
2	Nov. 22, 2011	sses	Updated status to Advance Information Added Antenna Supervisor support by LISA-U200-00S Added module switch-on by RESET_N support Updated LISA-U2x0-01x features in GPIO section Updated ESD maximum rating table
3	Feb. 02, 2012	sses	Updated status to Preliminary Updated current consumption table Updated features support in module power off and GPIO sections
A	May. 15, 2012	sses / lpah	Updated status to Objective Specification Updated PWR_ON low time to switch-on the module Removed Audio over USB support Added UART autobauding feature support
A1	Jul. 20, 2012	sses / lpah	Updated status to Preliminary Updated LISA-U2x0-01x GPRS/EDGE multi-slot class support Updated list of available USB drivers Updated module dimensions tolerances
A2	Sep. 28, 2012	lpah	Updated status to Advance Information First release for LISA-U260-01S, LISA-U270-01S
A3	Nov. 26, 2012	lpah	Updated status to Preliminary status

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