WIRELESS

locate, communicate, accelerate

LISA-U1 series

3.75G UMTS/HSPA Wireless Modules

Data Sheet

Abstract

Technical data sheet describing the LISA-U1 series UMTS/HSPA wireless modules.

These modules are a complete and cost efficient 3.75G solution offering dual-band high-speed HSDPA/HSUPA and quad-band GSM/EGPRS voice and/or data transmission technology in a compact form factor.

33.2 x 22.4 x 2.6 mm

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Document Information	
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Document status information	
Objective Specification	This document contains target values. Revised and supplementary data will be published later.
Advance Information	This document contains data based on early testing. Revised and supplementary data will be published later.
Preliminary	This document contains data from product verification. Revised and supplementary data may be published later.
Released	This document contains the final product specification.

This document applies to the following products:

Name	Type number	Firmware version	PCN / IN
LISA-U100	LISA-U100-00S-00	10.72	UBX-TN-12031
	LISA-U100-01S-00	11.40	UBX-TN-12008
LISA-U110	LISA-U110-00S-00	10.72	UBX-TN-12031
	LISA-U110-01S-00	11.40	UBX-TN-12008
	LISA-U110-60S-00	11.43	UBX-TN-12050
LISA-U120	LISA-U120-00S-00	10.72	UBX-TN-12031
	LISA-U120-01S-00	11.40	UBX-TN-12008
LISA-U130	LISA-U130-00S-00	10.72	UBX-TN-12031
	LISA-U130-01S-00	11.40	UBX-TN-12008
	LISA-U130-60S-00	11.43	UBX-TN-12050

Contents

1 Functional description

1.1 Overview

LISA-U1 series modules are a 3.75G solution providing full dual-band HSPA and quad-band GSM/EDGE data transmission in a compact form factor. These modules feature low power consumption and HSUPA category 6, HSDPA category 8, GPRS/EDGE class 12 data transmission with voice capability. They also combine baseband, RF transceiver, power management unit, and power amplifier in a single, easy-to-integrate solution.

LISA-U1 series modules are complete, fully qualified and certified solutions, which reduces cost and enables short time to market. They are ideally suited to M2M and automotive applications such as: mobile Internet terminals and applications, car infotainment and telematics, Automatic Meter Reading (AMR), Remote Monitoring Automation and Control (RMAC), surveillance and security, eCall, road pricing, asset tracking, fleet management, anti theft systems, and Point of Sales (PoS) terminals.

LISA-U1 series modules support full access to u-blox positioning chips and modules via serial port. Thus WCDMA/GSM and GPS/GNSS can be controlled through a single serial port from any host processor. The compact LISA form factor and SMT pads allow fully automated assembly with standard pick & place and reflow soldering equipment for cost-efficient, high-volume production.

1.2 Product features

Module	Technology		Bands		Interface					Audio		Functions										
	HSUPA [Mb/s]	HSDPA [Mb/s]	UMTS/HSPA bands [MHz]	GSM/GPRS/EDGE quad-band	UART	SPI (5-wire)	USB	DDC for u-blox GPS/GNSS	GPIO	Analog Audio	Digital Audio	Network indication	Antenna Supervisor	Jamming detection	Embedded TCP/UDP stack	HTTP, SSL	GPS/GNSS via Modem	Embedded AssistNow	FW update over AT (FOAT)	In-band modem	Rx diversity	CellLocate	SIM Access Profile (SAP)
LISA-U100-00S	5.76	7.2	850/1900	•	1	1	1	1	5			•	•		•		•	•					
LISA-U100-01S	5.76	7.2	850/1900	•	1	1	1	1	5			•	•	•	•	•	•	•	•			•	
LISA-U110-00S	5.76	7.2	900/2100	•	1	1	1	1	5			•	•		•		•	•					
LISA-U110-01S	5.76	7.2	900/2100	•	1	1	1	1	5			•	•	•	•	•	•	•	•			•	
LISA-U110-60S	5.76	7.2	900/2100	•	1	1	1	1	5			•	•	•	•	•	•	•	•			•	
LISA-U120-00S	5.76	7.2	850/1900	•	1	1	1	1	5	1	1	•	•		•		•	•					
LISA-U120-01S	5.76	7.2	850/1900	•	1	1	1	1	5	1	1	•	•	•	•	•	•	•	•	•		•	
LISA-U130-00S	5.76	7.2	900/2100	•	1	1	1	1	5	1	1	•	•		•		•	•					
LISA-U130-01S	5.76	7.2	900/2100	•	1	1	1	1	5	1	1	•	•	•	•	•	•	•	•	•		•	
LISA-U130-60S	5.76	7.2	900/2100	•	1	1	1	1	5	1	1	•	•	•	•	•	•	•	•	•		•	

LISA-U110-60S and LISA-U130-60S modules FW versions are approved and locked for SoftBank Japanese network operator.

Table 1: LISA-U1 series features

1.3 Block diagram

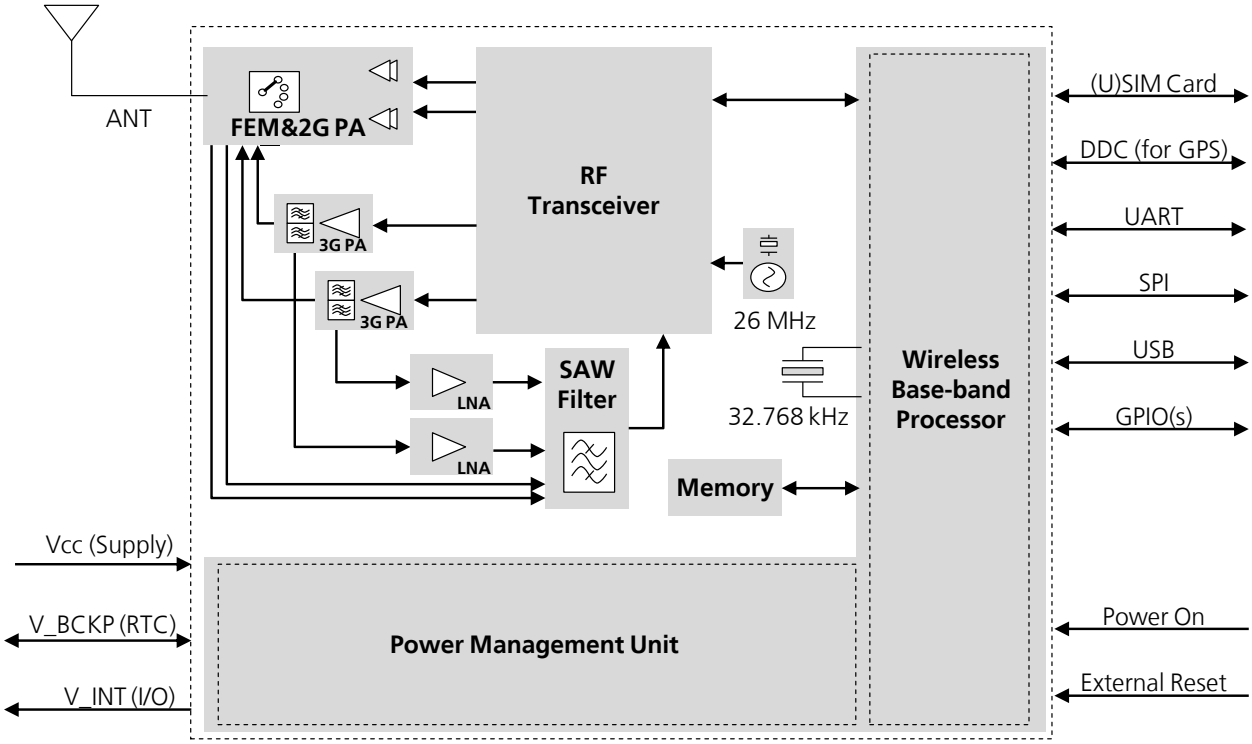

Figure 1: LISA-U100 / LISA-U110 block diagram

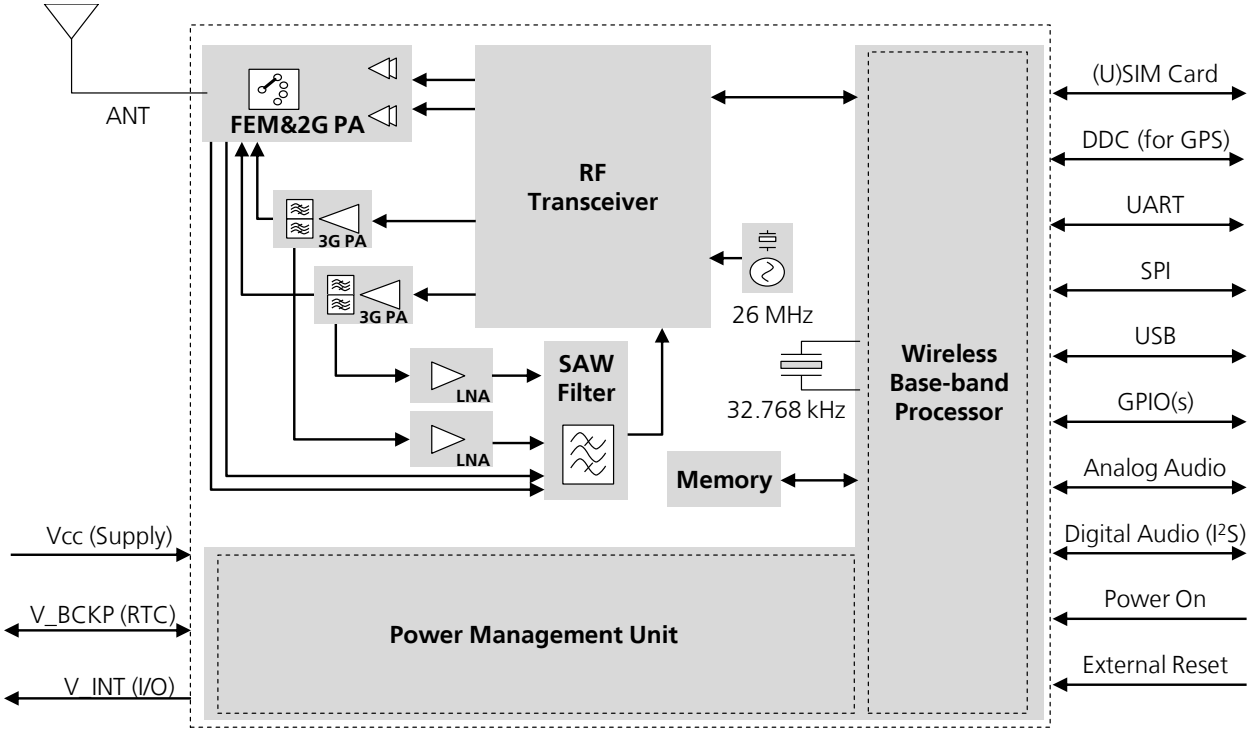

Figure 2: LISA-U120 / LISA-U130 block diagram

1.4 Product description

3G UMTS/HSDPA/HSUPA Characteristics	2G GSM/GPRS/EDGE Characteristics
Class A User Equipment[1]	Class B Mobile Station[2]
UMTS Terrestrial Radio Access (UTRA) Frequency Division Duplex (FDD) 3GPP Release 6 High Speed Packet Access (HSPA)	GSM EDGE Radio Access (GERA) 3GPP Release 6
Dual-band support: • Band II (1900 MHz) and Band V (850 MHz) for LISA-U100, LISA-U120 • Band I (2100 MHz) and Band VIII (900 MHz) for LISA-U110, LISA-U130	Quad-band support • GSM 850 MHz, E-GSM 900 MHz, DCS 1800 MHz, PCS 1900 MHz
WCDMA/HSDPA/HSUPA Power Class • Power Class 3 (24 dBm) for WCDMA/HSDPA/HSUPA mode	GSM/GPRS Power Class • Power Class 4 (33 dBm) for GSM/E-GSM bands • Power Class 1 (30 dBm) for DCS/PCS bands EDGE Power Class • Power Class E2 (27 dBm) for GSM/E-GSM bands • Power Class E2 (26 dBm) for DCS/PCS bands
PS (Packet Switched) Data Rate • HSUPA category 6, up to 5.76 Mb/s UL • HSDPA category 8, up to 7.2 Mb/s DL • WCDMA PS data up to 384 kb/s DL/UL	PS (Packet Switched) Data Rate • GPRS multislot class 12[3], coding scheme CS1-CS4, up to 85.6 kb/s DL/UL • EDGE multislot class 12[3], coding scheme MCS1-MCS9, up to 236.8 kb/s DL/UL
CS (Circuit Switched) Data Rate • WCDMA CS data up to 64 kb/s DL/UL	CS (Circuit Switched) Data Rate • GSM CS data up to 9.6 kb/s DL/UL supported in transparent/non transparent mode

Table 2: LISA-U1 series UMTS/HSDPA/HSUPA and GSM/GPRS/EDGE characteristics

Operation modes I to III are supported on GSM/GPRS network, with user-defined preferred service selectable from GSM to GPRS. Paging messages for GSM calls can be monitored during GPRS data transfer in not-coordinating NOM II-III.

Direct Link mode for TCP and UDP sockets is supported by all LISA-U1 series modules except LISA-U1x0-00S versions.

[1] Device can work simultaneously in Packet Switch and Circuit Switch mode: voice calls are possible while the data connection is active without any interruption in service.

[2] Device can be attached to both GPRS and GSM services (i.e. Packet Switch and Circuit Switch mode) using one service at a time. If for example during data transmission an incoming call occurs, the data connection is suspended to allow the voice communication. Once the voice call has terminated, the data service is resumed.

[3] GPRS/EDGE multislot class 12 implies a maximum of 4 slots in DL (reception) and 4 slots in UL (transmission) with 5 slots in total. GPRS class determines the number of timeslots available for upload and download and thus the speed at which data can be transmitted and received, with higher classes typically allowing faster data transfer rates.

Basic features[4]	Supplementary services	Short Message Service (SMS)
Display of Called Number	Call Hold/Resume (CH)	SMS Classes 0, 1, 2, 3
Indication of Call Progress Signals	Call Waiting (CW)	Mobile-Originating SMS (MO SMS)
Country/PLMN Indication	Multi-Party (MTPY)	Mobile-Terminating SMS (MT SMS)
International Access Function	Call Forwarding (CF)	SMS Cell Broadcast (SMS CB)
Service Indicator	Call Divert	Text and PDU mode supported
Dual Tone Multi Frequency (DTMF)	Explicit Call Transfer (ECT)	SMS during circuit-switched calls
Subscription Identity Management	Call Barring (CB)	SMS over PSD or CSD
Service Provider Indication	Call Completion to Busy Subscriber (CCBS)	SMS storage on SIM and memory module
Abbreviated Dialing	Advice of Charge Charging (AOCC)	
SIM Toolkit	Calling Line Identification Presentation (CLIP)	
	Calling Line Identification Restriction (CLIR)	
	Connected Line Identification Presentation (COLP)	
	Connected Line Identification Restriction (COLR)	
	Unstructured Supplementary Services Data (USSD)	
	Network Identify and Time Zone (NITZ)	

Table 3: Basic Features[4], Supplementary Services, and Short Message Service (SMS)

1.5 AT Command support

The module supports AT commands according to 3GPP standards: TS 27.007 [1], 27.005 [2], 27.010 [3], and the u-blox AT command extension.

☞ For the complete list of the supported AT commands and their syntax see the u-blox AT Commands Manual [5].

RIL (Radio Interface Layer) is provided with LISA-U1 series modules and is compatible with following deliveries:

- Android Gingerbread 2.3
- Android Ice Cream Sandwich 4.0
- Windows Embedded CE 6.0
- Windows Embedded Compact 7

1.6 AssistNow clients and GPS/GNSS integration

For customers using u-blox positioning chips and modules, LISA-U1 series modules feature embedded AssistNow Online and AssistNow Offline clients. AssistNow A-GPS provides better GPS performance and faster Time-To-First-Fix. The clients can be enabled / disabled with an AT command.

LISA-U1 series modules act as a stand-alone AssistNow client, making AssistNow available with no additional requirements for resources or software integration on an external host micro controller. Full access to u-blox positioning chips and modules is available via the wireless modules, through a dedicated DDC (I²C) interface. This means that GSM/WCDMA and GPS/GNSS can be controlled through a single serial port from any host processor.

For more details, see the GPS Implementation Application Note [7].

[4] These functionalities are supported via AT commands (for more details see the u-blox AT Commands Manual [5]).

1.7 In-Band modem (LISA-U120 / LISA-U130 only)

☞ In-Band modem is not supported by LISA-U120-00S and LISA-U130-00S.

LISA-U130 supports In-Band modem for eCall, according to the 3GPP TS 26.267 specification [9]. In-Band modem is a mandatory feature to meet eCall requirements and to develop in-vehicle devices that fully support eCall.

According to the eCall (Pan-European automatic in-vehicle emergency call system) specification, an eCall must be generated automatically or manually following a car accident, using GSM cellular service "112". When activated, the in-vehicle eCall system (IVS) creates an emergency call carrying both voice and data (e.g. vehicle GPS position) directly to the nearest 112 Public Safety Answering Point (PSAP).

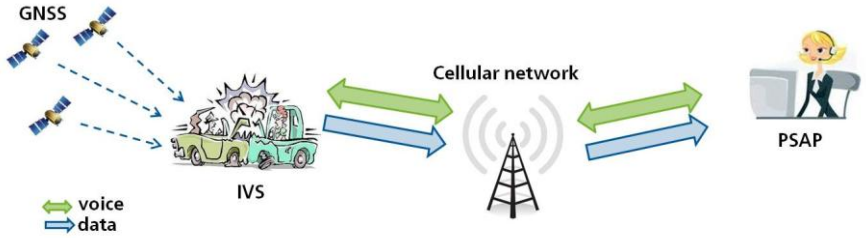

Figure 3: In-Band modem diagram flow

In-band modem allows fast and reliable transmission of vehicle Minimum Set of Data (MSD - 140 bytes) and the establishment of a voice emergency call using the same physical channel (voice channel) without any modifications of the existing cellular network architecture.

1.8 Smart temperature supervision

An internal temperature sensor constantly monitors the board temperature of LISA-U1 series modules. The measured temperature is compared with the internally predefined thresholds and the following actions may be taken:

- A warning notification is reported by the module when the temperature is close to the limit (upper or lower) but still inside the valid operation range (i.e. the module is still in a valid and good working condition)
- A shutdown is notified and automatically forced by the module when the temperature value is outside the specified range (i.e. the module is in a dangerous working condition). For security reasons the shutdown is suspended in case of emergency call in progress: in this case the device will switch off at call termination

Smart Temperature Supervisor feature can be enabled or disabled via an AT command (for more details please to u-blox AT commands manual [5], +USTS AT command). If the feature is disabled there is no embedded protection against not allowed temperature working conditions.

☞ The sensor measures board temperature inside the shields, which can differ from ambient temperature.

1.9 Firmware (upgrade) Over serial interface, with AT commands (FOAT)

☞ Not supported by LISA-U1x0-00S.

This feature allows upgrading module Firmware over UART, USB and SPI interfaces, using AT commands.

- AT+UFWUPD command triggers a reboot followed by the upgrade procedure at a specified baud rate (refer to u-blox AT Commands Manual [5] for more details)
- Both Xmodem-1k protocol (1024 bytes packets) and Xmodem protocol (128 bytes packets) can be used for downloading the new firmware image via a terminal application
- A special boot loader on the module performs firmware installation, security verifications and module reboot
- Firmware authenticity verification is performed via a security signature during the download. The firmware is then installed, overwriting the current version. In case of power loss during this phase, the boot loader detects a fault at the next wake-up, and restarts the firmware download from the Xmodem-1k handshake. After completing the upgrade, the module is reset again and wakes-up in normal boot

1.10 Embedded TCP/IP and UDP/IP

LISA-U1 series modules include embedded TCP/IP and UDP/IP stack. For more details about AT commands see the u-blox AT Commands Manual [5].

Direct Link mode for TCP and UDP sockets is supported by all LISA-U1 series modules except LISA-U1x0-00S versions. Sockets can be set in Direct Link mode to establish a transparent end to end communication with an already connected TCP or UDP socket via serial interface.

1.11 FTP and FTPS

☞ Not supported by LISA-U1x0-00S.

File Transfer Protocol as well as Secure File Transfer Protocol functionalities are supported via AT commands. Files are read and stored in the local file system of the module. For more details about AT commands see u-blox AT Commands Manual [5].

1.12 HTTP and HTTPS

☞ Not supported by LISA-U1x0-00S.

HTTP and HTTPS protocols are supported. HEAD, GET, POST, DELETE and PUT operations are available. The file size to be uploaded or downloaded depends on the free space available in the local file system (FFS) at the moment of the operation. Up to 4 client contexts can be simultaneously used.

For more details about AT commands see the u-blox AT Commands Manual [5].

1.13 Jamming Detection

☞ Not supported by LISA-U1x0-00S.

In real network situations modules can experience various kind of out-of-coverage conditions: limited service conditions when roaming to networks not supporting the specific SIM, limited service in cells which are not suitable or barred due to operators' choices, no cell condition when moving to poorly served or highly interfered areas. In the latter case, interference can be artificially injected in the environment by a noise generator covering a given spectrum, thus obscuring the operator's carriers entitled to give access to the GSM/UMTS service.

The Jamming Detection Feature detects such "artificial" interference and reports the start and stop of such conditions to the application processor, which can react appropriately by e.g. switching off the radio transceiver in order to reduce power consumption and monitoring the environment at constant periods.

The congestion (i.e. jamming) detection feature can be enabled and configured by the +UCD AT command (for more details refer to the u-blox AT Commands Manual [5]).

1.14 Hybrid positioning and CellLocate

☞ Not supported by LISA-U1x0-00S.

Although GPS/GNSS technology is widespread, its reliance on the visibility of extremely weak satellite signals means that positioning is not always possible. Especially difficult environments are indoors, in enclosed or underground parking garages, as well as in urban canyons where satellite signals are blocked or jammed by multipath interference. The situation can be improved by augmenting satellite positioning data with cellular network information to provide positioning information even when GPS/GNSS reception is degraded or absent. This additional information can benefit numerous applications.

1.14.1 Positioning through cellular information: CellLocate

u-blox CellLocate enables the estimation of device position based on the parameters of the mobile network cells visible to the specific device. To estimate its position the u-blox Wireless module sends the CellLocate server the parameters of network cells visible to it using a UDP connection. In return the server provides the estimated position based on the CellLocate database. The u-blox wireless module can either send the parameters of the visible home network cells only (normal scan) or the parameters of all surrounding cells of all mobile operators (deep scan).

CellLocate is implemented using a set of two AT commands that allow configuration of the CellLocate service (AT+ULOCCELL) and requesting position according to the user configuration (AT+ULOC). The answer is provided in the form of an unsolicited AT command including latitude, longitude and estimated accuracy.

☞ Normal scan is only possible in 2G mode.

1.14.2 Hybrid positioning

With u-blox Hybrid positioning technology, u-blox wireless devices can be triggered to provide their current position using either a u-blox positioning chip and module or the estimated position from CellLocate. The choice depends on which positioning method provides the best and fastest solution according to the user configuration, exploiting the benefit of having multiple and complementary positioning methods.

Hybrid positioning is implemented through a set of three AT commands that allow configuration of the u-blox positioning chip and module (AT+ULOCGNSS), configuration of the CellLocate service (AT+ULOCCELL), and

requesting the position according to the user configuration (AT+ULOC). The answer is provided in the form of an unsolicited AT command including latitude, longitude and estimated accuracy (if the position has been estimated by CellLocate), and additional parameters if the position has been computed by the u-blox positioning chip and module.

The use of hybrid positioning requires a connection via the DDC (I^2C) bus between the LISA-U1 series wireless module and the u-blox positioning chip and module.

Refer to GPS Implementation Application Note [7] for the complete description of the feature.

u-blox is extremely mindful of user privacy. When a position is sent to the CellLocate server u-blox is unable to track the SIM used or the specific device.

2 Interfaces

2.1 Power Management

2.1.1 Module supply (VCC)

Modules must be supplied through the **VCC** pin by a DC power supply. Voltages must be stable: during operation, the current drawn from **VCC** can vary by some order of magnitude, especially due to the surging consumption profile of the GSM system (described in the LISA-U series System Integration Manual [6]). It is important that the system power supply circuit is able to support peak power.

2.1.2 RTC supply (V_BCKP)

V_BCKP is the Real Time Clock (RTC) supply. When VCC voltage is within the valid operating range, the internal Power Management Unit (PMU) supplies the RTC and the same supply voltage is available on **V_BCKP** pin. If the VCC voltage is under the minimum operating limit (e.g. during not powered mode), the RTC can be externally supplied via **V_BCKP** pin.

2.1.3 Digital I/O interfaces supply (V_INT)

LISA-U1 series modules provide an internally generated supply rail output for digital interfaces (**V_INT**). This can be used in place of an external discrete regulator to supply pull-up resistors on the DDC interface. This optimizes the bill of material for various applications, e.g. with u-blox positioning chip or module operating at 1.8 V.

2.2 RF antenna interface

The **ANT** pad has an impedance of 50 Ω and provides the RF antenna interface.

2.3 System functions

2.3.1 Module power-on

LISA-U1 series modules can be switched on in one of the following ways:

- Rising edge on **VCC** pins to a valid voltage as module supply, i.e. applying module supply
- Low pulse on the **PWR_ON** pin, i.e. forcing the pin (normally high with external pull-up) to a low level for a valid time period: **PWR_ON** pin requires an external pull-up resistor to set its value to logic high and must not be left floating
- Rising edge on the **RESET_N** pin, i.e. releasing the pin from the low level, normally high with internal pull-up
- RTC alarm, i.e. pre-programmed scheduled time by AT+CALA command (for more details refer to u-blox AT commands manual [5])

2.3.2 Module power-off

LISA-U1 series modules can be switched off, with parameters saving and proper network detach, in this way:

- AT+CPWROFF command (more details in u-blox AT Commands Manual [5])

2.3.3 Module reset

LISA-U1 series modules can be reset in one of these ways:

- Forcing to the low level the **RESET_N** pin, normally high with internal pull-up. This causes an "external" or "hardware" reset of the entire module, including the integrated power management unit, except for the RTC internal block: the **V_INT** interfaces supply is switched off and all the digital pins are set in tri-state mode, but the **V_BCKP** supply and the RTC block are enabled. Forcing an "external" or "hardware" reset, the current parameter settings are not saved in the module's non-volatile memory and a proper network detach is not performed
- By the AT+CFUN command (refer to u-blox AT Commands Manual [5]). This causes an "internal" or "software" reset of the baseband processor, excluding the integrated power management unit and the RTC internal block: the **V_INT** interfaces supply is enabled and each digital pin is set in its internal reset state (reported in the Table 5), the **V_BCKP** supply and the RTC block are enabled. When an "internal" or "software" reset is forced, the current parameter settings are saved in the module's non-volatile memory and a proper network detach is performed

2.4 (U)SIM interface

A (U)SIM card interface is provided on the SMT pads of the LISA-U1 series modules: the high-speed SIM/ME interface is implemented as well as automatic detection of the required SIM supporting voltage.

Both 1.8 V and 3 V SIM types are supported (1.8 V and 3 V ME). Activation and deactivation with automatic voltage switch from 1.8 V to 3 V is implemented, according to ISO-IEC 7816-3 specifications. The SIM driver supports the PPS (Protocol and Parameter Selection) procedure for baud-rate selection, according to the values proposed by the SIM Card.

2.5 Serial communication

LISA-U1 series modules provide the following serial communication interfaces where AT command interface and Packet-Switched / Circuit-Switched Data communication are concurrently available:

- One asynchronous serial interface (UART)
- One Inter Processor Communication (IPC) interface that includes a synchronous SPI-compatible interface
- One high-speed USB 2.0 compliant interface

When used as AT command interface, all the serial communication interfaces listed above can be used for firmware upgrade using AT command (+UFWUPD, for more details refer to u-blox AT Commands Manual [5]), but only the following serial communication interfaces can be used for firmware upgrade using the u-blox Easy Flash tool:

- The UART interface, using the **RxD** and **TxD** lines only
- The USB interface, using all the provided lines (**VUSB_DET**, **USB_D+** and **USB_D-**)

2.5.1 Asynchronous serial interface (UART)

The UART interface is a 9-wire unbalanced asynchronous serial interface provided for all communications with LISA-U1 series modules.

UART features are:

- Complete serial port with RS-232 functionality conforming to the ITU-T V.24 Recommendation [4], with CMOS compatible signal levels (0 V for low data bit or ON state and 1.8 V for high data bit or OFF state)
- Data lines (**RxD** as output, **TxD** as input), hardware flow control lines (**CTS** as output, **RTS** as input), modem status and control lines (**DTR** as input, **DSR** as output, **DCD** as output, **RI** as output) are provided
- Hardware flow control (default value), software flow control, or none flow control are supported
- Power saving indication available[5] on the hardware flow control output (**CTS** line): the line is driven to the OFF state when the module is not prepared to accept data by the UART interface
- 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400 and 460800 b/s baud rates are supported for the AT interface
- Default baud rate is 115200 b/s
- Autobauding is not supported
- Frame format can be:
  - 8N2 (8 data bits, no parity, 2 stop bits)
  - 8N1 (8 data bits, no parity, 1 stop bit)
  - 8E1 (8 data bits, even parity, 1 stop bit)
  - 8O1 (8 data bits, odd parity, 1 stop bit)
  - 7E1 (7 data bits, even parity, 1 stop bit)
  - 7O1 (7 data bits, odd parity, 1 stop bit)
- Default frame configuration is 8N1

UART serial interface can be opportunely configured through AT commands. For more details please refer to u-blox AT Commands Manual [5] (+IPR, +ICF, +IFC, &K, \Q, +UPSV AT command) and LISA-U series System Integration Manual [6].

2.5.2 Universal Serial Bus (USB)

The LISA-U1 series modules include a high-speed USB 2.0 compliant interface with maximum throughput of 480 Mb/s. The module itself acts as a USB device and can be connected to any USB host.

The USB is the main interface for transferring high speed data between LISA-U1 series and a host processor.

Signals **USB_D+/USB_D-** carry the USB serial data and signaling. The USB interface is automatically enabled by a valid USB VBUS supply voltage (5.0 V typical) on **VUSB_DET** pin.

The module simultaneously provides 6 USB CDCs (Communications Device Class) with this configuration:

- USB1: AT commands / data connection
- USB2: AT commands / data connection
- USB3: AT commands / data connection
- USB4: GPS tunneling
- USB5: Primary TraceLog (debug purpose)
- USB6: Secondary TraceLog (debug purpose)

[5] If enabled

The user can concurrently use AT command interface on one CDC and Packet-Switched / Circuit-Switched Data communication on another CDC.

USB CDC/ACM drivers are available for the following operating system platforms:

- Windows 2000
- Windows XP
- Windows Vista
- Windows 7
- Windows CE 5.0
- Windows Embedded CE 6.0
- Windows Embedded Compact 7
- Windows Embedded Automotive 7
- Windows Mobile 5
- Windows Mobile 6
- Windows Mobile 6.1
- Windows Mobile 6.5

LISA-U1 series modules are compatible with standard Linux/Android USB kernel drivers

2.5.3 Serial Peripheral Interface (SPI)

The LISA-U1 series modules provide a 5-wire Inter Processor Communication (IPC) interface that includes two handshake signals (**SPI_MRDY** and **SPI_SRDY**), added to a standard 3-wire SPI-compatible serial interface (**SPI_MOSI**, **SPI_MISO**, **SPI_SCLK**). The LISA-U1 series modules run natively as an SPI slave.

The SPI / IPC interface can be used for high speed data transfer (UMTS/HSPA) between LISA-U1 series modules and the host processor. The high speed communication (up to 26 Mb/s) between the two processors is possible only if both sides follow the same Inter Processor Communication (IPC) specifications.

Refer to LISA-U series System Integration Manual [6] and SPI Interface Application Note [12] for a detailed description of the implementation of the SPI / IPC protocol.

2.5.4 Multiplexer protocol

LISA-U1 series module has a software layer with MUX functionality, 3GPP TS 27.010 Multiplexer Protocol [3], available either on the UART or on the SPI physical link.

☞ The multiplexer protocol is not supported by the USB interface.

This is a data link protocol (layer 2 of OSI model) which uses HDLC-like framing and operates between the module (DCE) and the application processor (DTE) and allows simultaneous sessions over the used physical link (UART or SPI): the user can concurrently use AT command interface on one MUX channel and Packet-Switched / Circuit-Switched Data communication on another MUX channel. The multiplexer protocol can be used on one serial interface (UART or SPI) at a time. Each session consists of a stream of bytes transferring various kinds of data such as SMS, CBS, PSD, GPS, AT commands in general.

The following channels are defined:

- Channel 0: control channel
- Channel 1 – 5: AT commands / data connection
- Channel 6: GPS tunneling

This permits, for example, an SMS to be transferred to the DTE when a data connection is in progress.
For more details please refer to the GSM MUX Implementation Application Note [8].

2.6 DDC (I^2C) bus interface

The LISA-U1 series modules include an I^2C compatible DDC interface exclusively for communication with u-blox positioning chips and modules.

2.7 Audio (LISA-U120 and LISA-U130 only)

The LISA-U120 and LISA-U130 modules provide one analog and one digital audio interface:

- Analog audio interface: a differential analog microphone[6] input (**MIC_P/MIC_N**) shared for all uplink analog path modes (handset, headset and hands-free) and a differential analog output (**SPK_P/SPK_N**) shared for all downlink analog path modes (earpiece, headset and loudspeaker). The uplink or downlink analog path profiles use the same physical input or output but have different sets of audio parameters (for more details please refer to u-blox AT Commands Manual [5], AT+USPM, AT+USGC, AT+UDBF, AT+USTN commands)
- Digital audio interface: a 4-wire I^2S digital audio interface, including **I2S_CLK**, **I2S_RXD**, **I2S_TXD**, **I2S_WA**. This audio path is selected when parameters <main_uplink> and <main_downlink> in AT+USPM command (for more details please refer to u-blox AT Commands Manual [5]) are respectively "I^2S input line" and "I^2S output line"

For further details about the hardware integration of the audio interface in an application design, refer to the LISA-U series System Integration Manual [6].

For further details about the possible settings of the audio interface, as well as the allowed input/output audio path combinations and as the default values related to the uplink/downlink path, refer to u-blox AT Commands Manual [5], +USPM AT command.

2.8 GPIO

LISA-U1 series modules provide 5 pins (**GPIO1**, **GPIO2**, **GPIO3**, **GPIO4** and **GPIO5**) which can be configured as a general purpose input or output, or can be configured to provide special functions via u-blox AT commands (for further details please refer to the LISA-U series System Integration Manual [6] and refer to u-blox AT Commands Manual [5], +UGPIOC, +UGPIOR, +UGPIOW, +UGPS, +UGPRF).

The following custom functions are available on the GPIO pins of LISA-U1 series modules:

Function	Description	Default GPIO	Configurable GPIOs
GSM Tx-burst indication	GSM transmit slot indication	--	GPIO1
GPS supply enable	Enable/disable the supply of u-blox GPS/GNSS receiver connected to wireless module	GPIO2	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5
GPS data ready	Sense when u-blox GPS/GNSS receiver connected to wireless module is ready for sending data by DDC (I^2C)	GPIO3	GPIO3
GPS RTC sharing	RTC (Real Time Clock) synchronization signal to u-blox GPS/GNSS receiver connected to wireless module	GPIO4	GPIO4
SIM card detection	SIM card presence	GPIO5	GPIO5

[6] On LISA-U1 series the microphone supply is not available

Function	Description	Default GPIO	Configurable GPIOs
Network status indication	Network status: registered home network, registered roaming, data transmission, no service	--	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5
General purpose input	Input to sense high or low digital level	--	All
General purpose output	Output to set the high or the low digital level	--	All
Pad disabled	Tri-state with an internal active pull-down enabled	GPIO1	All

Table 4: GPIO custom functions configuration

☞ GPS data ready and GPS RTC sharing functions are not supported by LISA-U1x0-00S versions.

☞ On LISA-U1x0-00S **GPIO3** and **GPIO4** pins are by default configured as "pad disabled".

3 Pin definition

3.1 Pin assignment

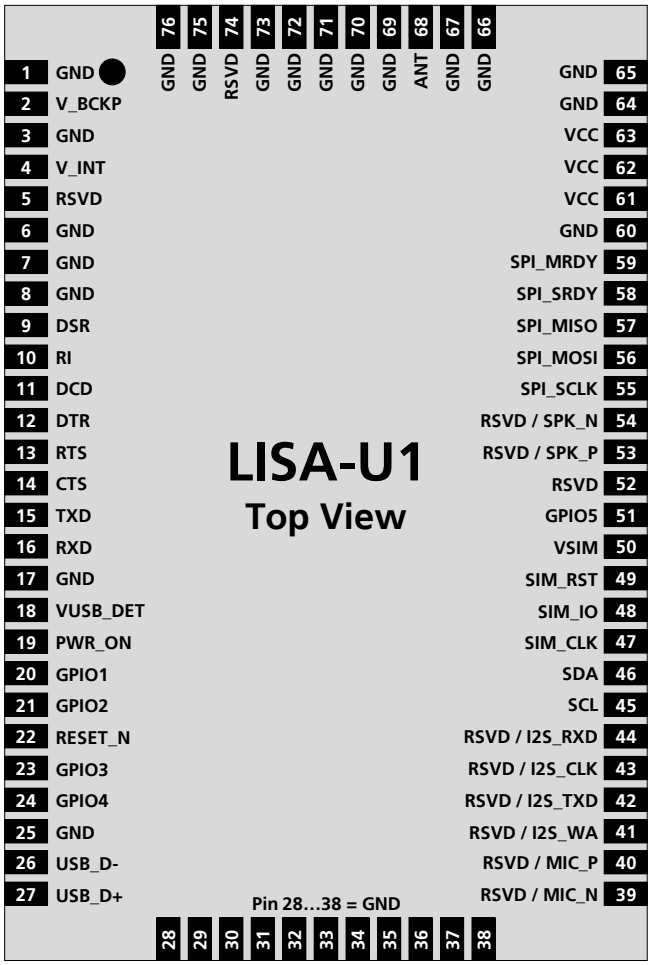

Figure 4: LISA-U1 series pin assignment

No	Module	Name	Power domain	I/O	Description	Remarks
1	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
2	All	V_BCKP	-	I/O	Real Time Clock supply input/output	V_BCKP = 2.3 V (typical) generated by the module to supply the Real Time Clock when VCC supply voltage is within valid operating range. A backup battery can be connected to this pin to supply the Real Time Clock when VCC supply voltage is not within valid operating range. See section 4.2.3 for detailed electrical specs.
3	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
4	All	V_INT	-	O	Digital I/O Interfaces supply output	V_INT = 1.8V (typical) generated by the module when it is switched-on and the RESET_N (external reset input pin) is not forced to the low level. See section 4.2.3 for detailed electrical specs.

No	Module	Name	Power domain	I/O	Description	Remarks
5	All	RSVD	-	N/A	RESERVED pin	This pin has special function: it must be connected to GND to allow module to work properly.
6	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
7	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
8	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
9	All	DSR	GDI	O	UART data set ready	Circuit 107 (DSR) in ITU-T V.24. Output driver class B. PU/PD class a. Value at internal reset: T/PU. See section 4.2.9 for detailed electrical specs.
10	All	RI	GDI	O	UART ring indicator	Circuit 125 (RI) in ITU-T V.24. Output driver class B. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
11	All	DCD	GDI	O	UART data carrier detect	Circuit 109 (DCD) in ITU-T V.24. Output driver class B. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
12	All	DTR	GDI	I	UART data terminal ready	Circuit 108/2 (DTR) in ITU-T V. 24. Internal active pull-up to V_INT enabled. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
13	All	RTS	GDI	I	UART ready to send	Circuit 105 (RTS) in ITU-T V.24. Internal active pull-up to V_INT enabled. PU/PD class c. Value at internal reset: T/PU. See section 4.2.9 for detailed electrical specs.
14	All	CTS	GDI	O	UART clear to send	Circuit 106 (CTS) in ITU-T V.24. Output driver class B. PU/PD class c. Value at internal reset: T/PU. See section 4.2.9 for detailed electrical specs.
15	All	TXD	GDI	I	UART transmitted data	Circuit 103 (TxD) in ITU-T V.24. Internal active pull-up to V_INT enabled. PU/PD class c. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
16	All	RXD	GDI	O	UART received data	Circuit 104 (RxD) in ITU-T V.24. Output driver class B. PU/PD class c. Value at internal reset: T/PU. See section 4.2.9 for detailed electrical specs.
17	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
18	All	VUSB_DET	USB	I	USB detect input	Input for VBUS (5 V typical) USB supply sense. See section 4.2.10 for detailed electrical specs.
19	All	PWR_ON	POS	I	Power-on input	The PWR_ON pin has high input impedance: do not leave it floating in noisy environment (an external pull-up resistor is required) See section 4.2.6 for detailed electrical specs.
20	All	GPIO1	GDI	I/O	GPIO	Output driver class D. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
21	All	GPIO2	GDI	I/O	GPIO	Output driver class C_0. PU/PD class b_0. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
22	All	RESET_N	ERS	I	External reset input	Internal 10 kΩ pull-up resistor to V_BCKP. See section 4.2.7 for detailed electrical specs.
23	All	GPIO3	GDI	I/O	GPIO	Output driver class B. PU/PD class c. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.

No	Module	Name	Power domain	I/O	Description	Remarks
24	All	GPIO4	GDI	I/O	GPIO	Output driver class B. PU/PD class c. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
25	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
26	All	USB_D-	USB	I/O	USB Data Line D-	90 Ω nominal differential impedance Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 high-speed specification [10] are part of the USB pad driver and need not be provided externally. Value at internal reset: T. See section 4.2.10 for detailed electrical specs.
27	All	USB_D+	USB	I/O	USB Data Line D+	90 Ω nominal differential impedance Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 high-speed specification [10] are part of the USB pad driver and need not be provided externally. Value at internal reset: T. See section 4.2.10 for detailed electrical specs.
28	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
29	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
30	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
31	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
32	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
33	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
34	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
35	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
36	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
37	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
38	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
39	LISA-U100 LISA-U110	RSVD	-	N/A	RESERVED pin	Leave unconnected.
	LISA-U120 LISA-U130	MIC_N	AUDIO	I	Differential analog audio input (negative)	Differential analog input shared for all path modes: handset, headset, hands-free mode. Internal DC blocking capacitor. See section 4.2.12 for detailed electrical specs.
40	LISA-U100 LISA-U110	RSVD	-	N/A	RESERVED pin	Leave unconnected.
	LISA-U120 LISA-U130	MIC_P	AUDIO	I	Differential analog audio input (positive)	Differential analog input shared for all path modes: handset, headset, hands-free mode. Internal DC blocking capacitor. See section 4.2.12 for detailed electrical specs.
41	LISA-U100 LISA-U110	RSVD	-	N/A	RESERVED pin	Leave unconnected.
	LISA-U120-00S LISA-U130-00S	I2S_WA	GDI	O	I^2S word alignment	Output driver class C. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
	LISA-U120-01S LISA-U130-01S LISA-U130-60S	I2S_WA	GDI	I/O	I^2S word alignment	Input with internal active pull-down to GND enabled in slave mode, Output in master mode. Output driver class C. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
42	LISA-U100 LISA-U110	RSVD	-	N/A	RESERVED pin	Leave unconnected.
	LISA-U120 LISA-U130	I2S_TXD	GDI	O	I^2S transmit data	Output driver class C. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.

No	Module	Name	Power domain	I/O	Description	Remarks
43	LISA-U100 LISA-U110	RSVD	-	N/A	RESERVED pin	Leave unconnected.
	LISA-U120-00S LISA-U130-00S	I2S_CLK	GDI	O	I²S clock	Output driver class C. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
	LISA-U120-01S LISA-U130-01S LISA-U130-60S	I2S_CLK	GDI	I/O	I²S clock	Input with internal active pull-down to GND enabled in slave mode, Output in master mode. Output driver class C. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
44	LISA-U100 LISA-U110	RSVD	-	N/A	RESERVED pin	Leave unconnected.
	LISA-U120 LISA-U130	I2S_RXD	GDI	I	I²S receive data	Internal active pull-down to GND enabled. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
45	All	SCL	DDC	O	I²C bus clock line	Fixed open drain. No internal pull-up. Value at internal reset: T. See section 4.2.11 for detailed electrical specs.
46	All	SDA	DDC	I/O	I²C bus data line	Fixed open drain. No internal pull-up. Value at internal reset: T. See section 4.2.11 for detailed electrical specs.
47	All	SIM_CLK	SIM	O	SIM clock	Value at internal reset: L. See section 4.2.8 for detailed electrical specs.
48	All	SIM_IO	SIM	I/O	SIM data	Internal 4.7 kΩ pull-up resistor to VSIM. Value at internal reset: L/PD. See section 4.2.8 for detailed electrical specs.
49	All	SIM_RST	SIM	O	SIM reset	Value at internal reset: L. See section 4.2.8 for detailed electrical specs.
50	All	VSIM	-	O	SIM supply output	VSIM = 1.80 V typical or 2.90 V typical generated by the module according to the SIM card type. See section 4.2.3 for detailed electrical specs.
51	All	GPIO5	GDI	I/O	GPIO	Output driver class C. PU/PD class c. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
52	All	RSVD	-	N/A	RESERVED pin	Leave unconnected.
53	LISA-U100 LISA-U110	RSVD	-	N/A	RESERVED pin	Leave unconnected.
	LISA-U120 LISA-U130	SPK_P	AUDIO	O	Differential analog audio output (positive)	Differential analog audio output shared for all path modes: earpiece, headset and loudspeaker mode. See section 4.2.12 for detailed electrical specs.
54	LISA-U100 LISA-U110	RSVD	-	N/A	RESERVED pin	Leave unconnected.
	LISA-U120 LISA-U130	SPK_N	AUDIO	O	Differential analog audio output (negative)	Differential analog audio output shared for all path modes: earpiece, headset and loudspeaker mode. See section 4.2.12 for detailed electrical specs.
55	All	SPI_SCLK	GDI	I	SPI Serial Clock Input	Idle low (CPOL=0). Internal active pull-down to GND enabled. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
56	All	SPI_MOSI	GDI	I	SPI Data Line Input	Shift data on rising clock edge (CPHA=1). Latch data on falling clock edge (CPHA=1). Idle high. Internal active pull-up to V_INT enabled. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.

No	Module	Name	Power domain	I/O	Description	Remarks
57	All	SPI_MISO	GDI	O	SPI Data Line Output	Shift data on rising clock edge (CPHA=1). Latch data on falling clock edge (CPHA=1). Idle high. Output driver class C. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
58	All	SPI_SRDY	GDI	O	SPI Slave Ready Output	Idle low. Output driver class B. PU/PD class c. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
59	All	SPI_MRDY	GDI	I	SPI Master Ready Input	Idle low. Internal active pull-down to GND enabled. PU/PD class c. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
60	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
61	All	VCC	-	I	Module supply input	All VCC pads must be connected to external supply
62	All	VCC	-	I	Module supply input	All VCC pads must be connected to external supply
63	All	VCC	-	I	Module supply input	All VCC pads must be connected to external supply
64	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
65	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
66	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
67	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
68	All	ANT	-	I/O	RF input/output for Tx/Rx antenna	50 Ω nominal impedance
69	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
70	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
71	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
72	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
73	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
74	All	RSVD	-	N/A	RESERVED pin	Leave unconnected.
75	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
76	All	GND	-	N/A	Ground	All GND pads must be connected to ground.

Table 5: Pinout

☞ For more information about pinout see LISA-U series System Integration Manual [6].

See Appendix A for explanation of abbreviations and terms used.

4 Electrical specifications

Stressing the device above one or more of the ratings listed in the Absolute Maximum Rating section may cause permanent damage. These are stress ratings only. Operating the module at these or at any conditions other than those specified in the Operating Conditions sections (chapter 4.2) of the specification should be avoided. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Operating conditions ranges define those limits within which the functionality of the device is guaranteed.

Where application information is given, it is advisory only and does not form part of the specification.

4.1 Absolute maximum rating

Limiting values given below are in accordance with the Absolute Maximum Rating System (IEC 134).

Symbol	Description	Condition	Min.	Max.	Unit
VCC	Module supply voltage	Input DC voltage at VCC pin	-0.30	4.70	V
ICC	Module supply current	Input DC current at VCC pin		2.50	A
VUSB_DET	USB detection pin	Input DC voltage at VUSB_DET	-0.30	5.35	V
USB	USB D+/D- pins	Input DC voltage at USB_D+ and USB_D-	-1.00	5.35	V
V_BCKP	RTC supply voltage	Input DC voltage at V_BCKP pin	-0.15	2.50	V
GDI	Generic digital interfaces	Input DC voltage at Generic digital interfaces pins	-0.30	3.60	V
DDC	DDC interface	Input DC voltage at DDC interface pins	-0.30	3.60	V
SIM	SIM interface	Input DC voltage at SIM interface pin	-0.30	3.60	V
ERS	External reset signal	Input DC voltage at External reset signal pin	-0.15	2.50	V
POS	Power-on input	Input DC voltage at Power-on signal pin	-0.30	4.70	V
AUDIO	Audio input pins	Input DC voltage at Audio pins	-0.15	3.00	V
V_ANT	Antenna voltage	Input DC voltage at ANT pin	-0.15	3.00	V
P_ANT	Antenna power	Input RF power at ANT pin		10	dBm
Rho_ANT	Antenna ruggedness	Output RF load mismatch ruggedness at ANT pin		10:1	VSWR
Tstg	Storage Temperature		-40	85	°C

Table 6: Absolute maximum ratings

The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification, given in table above, must be limited to values within the specified boundaries by using appropriate protection devices.

4.1.1 Maximum ESD

Parameter	Min.	Typ.	Max.	Unit	Remarks
ESD sensitivity for all pins except ANT pin			1000	V	Human Body Model according to JESD22-A114F
ESD sensitivity for ANT pin			1000	V	Human Body Model according to JESD22-A114F
ESD immunity for ANT pin			500	V	Contact Discharge according to IEC 61000-4-2
			500	V	Air Discharge according to IEC 61000-4-2

Table 7: Maximum ESD ratings

LISA-U1 series modules are Electrostatic Sensitive Devices (ESD) and require special precautions when handling.

4.2 Operating conditions

Unless otherwise indicated, all operating condition specifications are at an ambient temperature of 25°C.

Operation beyond the operating conditions is not recommended and extended exposure beyond them may affect device reliability.

4.2.1 Operating temperature range

Symbol	Parameter	Min.	Typ.	Max.	Units	Remarks
Topr	Operating temperature range	-40		+85	°C	
		-20		+65	°C	Normal operating temperature range See chapter 4.2.1.1
		-40		-20	°C	Extended operating temperature range 1 See chapter 4.2.1.2
		+65		+85	°C	Extended operating temperature range 2 See chapter 4.2.1.3

Table 8: Environmental conditions

4.2.1.1 Normal operating temperature range

The wireless module is fully functional and meets the ETSI specification across the specified temperature range.

4.2.1.2 Extended operating temperature range 1

The wireless module is fully functional across the specified temperature range. Occasional deviations from the ETSI specification may occur.

4.2.1.3 Extended operating temperature range 2

The wireless module is functional across the specified temperature range. Occasional deviations from the ETSI specification may occur. Thermal protection including automatic shutdown is implemented for protection against overheating. Thermal protection is disabled for emergency calls. For more details, please refer to u-blox AT Commands Manual [5], +USTS AT command).

4.2.2 Module thermal resistance

Symbol	Parameter	Min.	Typ.	Max.	Units	Remarks
$R_{th,M-A}$	Module-to-Ambient thermal resistance	9		12	°C/W	Thermal resistance from the module internal temperature sensor to the ambient, with the module mounted on a 90 mm x 70 mm x 1.46 mm 4-layers PCB with a high coverage of copper in still air conditions
$R_{th,M-C}$	Module-to-Case thermal resistance	1.5		3.5	°C/W	Thermal resistance from the module internal temperature sensor to the module case, evaluated as the thermal resistance from the module internal temperature sensor to the ambient, with the module mounted on a 90 mm x 70 mm x 1.46 mm 4-layers PCB with a high coverage of copper, with a robust aluminum heat-sink on the back of the application board, with forced air ventilation

Table 9: LISA-U1 series module thermal resistance

4.2.3 Supply/Power pins

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Module supply normal operating input voltage[7]	3.40	3.80	4.20	V
	Module supply extended operating input voltage[8]	3.10		4.20	V
ICC_PEAK	Module supply peak current consumption: peak of current consumption through the VCC pad during a GSM transmit burst, at VCC = 3.8 V, with a matched antenna (typ. value) or with a mismatched antenna (max. value)[9]		2.00	2.50	A
V_BCKP	RTC supply input voltage	1.00	2.30	2.50	V
I_BCKP	RTC supply average current consumption, at V_BCKP = 2.3 V		2.50		µA

Table 10: Input characteristics of Supply/Power pins

Symbol	Parameter	Min.	Typ.	Max.	Unit
VSIM	SIM supply output voltage	1.76	1.80	1.83	V
		2.84	2.90	2.94	V
V_BCKP	RTC supply output voltage	2.19	2.30	2.42	V
I_BCKP	RTC supply output current capability			3	mA
V_INT	Digital I/O Interfaces supply output voltage	1.76	1.80	1.85	V
I_INT	Digital I/O Interfaces supply output current capability			50	mA

Table 11: Output characteristics of Supply/Power pins

[7] Input voltage at **VCC** must be above the normal operating range minimum limit to switch-on the module.
[8] Occasional deviations from the ETSI specifications may occur. Ensure that input voltage at **VCC** never drops below the extended operating range minimum limit during module operation: the wireless module may switch-off when the **VCC** voltage value drops below the extended operating range minimum limit.
[9] Use this figure to dimension maximum current capability of power supply.

4.2.4 Power consumption

Table 12 reports power consumption of LISA-U1 series module[10].

Mode	Condition	Power Consumption[11]
Power Off Mode	Module is switched off by AT+CPWROFF	< 90 µA
GSM/GPRS/EDGE Cyclic Idle/Active-Mode (Power Saving enabled by AT+UPSV)	GSM 850 / E-GSM 900 / DCS 1800 / PCS 1900 bands DRX = 5[12] USB interface not attached to a USB host	< 2 mA
	GSM 850 / E-GSM 900 / DCS 1800 / PCS 1900 bands DRX = 5[12] USB interface in the suspend state	< 2.5 mA
GSM Talk (Connected) Mode	GSM 850 / E-GSM 900 bands Maximum Tx power (32.5 dBm typ.)	< 250 mA
	DCS 1800 / PCS 1900 bands Maximum Tx power (29.5 dBm typ.)	< 200 mA
GPRS TBF (Connected) Mode	GSM 850 / E-GSM 900 bands 4 Tx +1 Rx slots (up to 85.6 kb/s UL, 21.4 kb/s DL) Maximum Tx power (31.0 dBm typ.)	< 660 mA
	DCS 1800 / PCS 1900 bands 4 Tx +1 Rx slots (up to 85.6 kb/s UL, 21.4 kb/s DL) Maximum Tx power (28.0 dBm typ.)	< 440 mA
EDGE TBF (Connected) Mode	GSM 850 / E-GSM 900 bands 4 Tx +1 Rx slots (up to 236.8 kb/s UL, 59.2 kb/s DL) Maximum Tx power (25.0 dBm typ.)	< 460 mA
	DCS 1800 / PCS 1900 bands 4 Tx +1 Rx slots (up to 236.8 kb/s UL, 59.2 kb/s DL) Maximum Tx power (24.0 dBm typ.)	< 340 mA
UMTS/HSxPA Cyclic Idle/Active-Mode (Power Saving enabled by AT+UPSV)	Band II (1900 MHz) / V (850 MHz) for LISA-U100/U120 Band I (2100 MHz) / VIII (900 MHz) for LISA-U110/U130 DRX = 7[13] USB interface not attached to a USB host	< 2 mA
	Band II (1900 MHz) / V (850 MHz) for LISA-U100/U120 Band I (2100 MHz) / VIII (900 MHz) for LISA-U110/U130 DRX = 7[13] USB interface in the suspend state	< 2.5 mA
UMTS Talk (Connected) Mode	Band II (1900 MHz) / V (850 MHz) for LISA-U100/U120 Band I (2100 MHz) / VIII (900 MHz) for LISA-U110/U130 12.2 kb/s UL, 12.2 kb/s DL Maximum Tx power (23.0 dBm typ.)	< 620 mA
HSDPA (Connected) Mode	Band II (1900 MHz) / V (850 MHz) for LISA-U100/U120 Band I (2100 MHz) / VIII (900 MHz) for LISA-U110/U130 Maximum Tx power (23.0 dBm typ.)	< 670 mA
HSUPA (Connected) Mode	Band II (1900 MHz) / V (850 MHz) for LISA-U100/U120 Band I (2100 MHz) / VIII (900 MHz) for LISA-U110/U130 5.76 Mb/s UL, 384 kb/s DL Maximum Tx power (21.5 dBm typ.)	< 500 mA
HSPA (Connected) Mode	Band II (1900 MHz) / V (850 MHz) for LISA-U100/U120 Band I (2100 MHz) / VIII (900 MHz) for LISA-U110/U130 5.76 Mb/s UL, 7.2 Mb/s DL Maximum Tx power (21.5 dBm typ.)	< 500 mA

Table 12: Power consumption

[10] It is assumed that no significant load is connected to any digital and analog pin except for antenna
[11] Maximum values for module average current consumption by the VCC pins in the listed modes/conditions, at 25°C, with VCC = 3.8 V, with a matched antenna.
[12] Module is registered with the network, with a paging period of 1177 ms (2G network DRX setting = 5), with 16 neighbour cells.
[13] Module is registered with the network, with a paging period of 1280 ms (3G network DRX setting = 7).

4.2.5 RF Performance

Parameter		Min.	Max.	Unit	Remarks
Frequency range GSM 850	Uplink	824	849	MHz	Module transmit
	Downlink	869	894	MHz	Module receive
Frequency range E-GSM 900	Uplink	880	915	MHz	Module transmit
	Downlink	925	960	MHz	Module receive
Frequency range DCS 1800	Uplink	1710	1785	MHz	Module transmit
	Downlink	1805	1880	MHz	Module receive
Frequency range PCS 1900	Uplink	1850	1910	MHz	Module transmit
	Downlink	1930	1990	MHz	Module receive
Frequency range UMTS 850 (band V)	Uplink	824	849	MHz	Module transmit
	Downlink	869	894	MHz	Module receive
Frequency range UMTS 900 (band VIII)	Uplink	880	915	MHz	Module transmit
	Downlink	925	960	MHz	Module receive
Frequency range UMTS 1900 (band II)	Uplink	1850	1910	MHz	Module transmit
	Downlink	1930	1990	MHz	Module receive
Frequency range UMTS 2100 (band I)	Uplink	1920	1980	MHz	Module transmit
	Downlink	2110	2170	MHz	Module receive

Table 13: Operating RF frequency bands

Parameter	Min.	Typ.	Max.	Unit	Remarks
Receiver input sensitivity GSM 850	-102.0	-110.0		dBm	Downlink RF level @ BER Class II < 2.4 %
Receiver input sensitivity E-GSM 900	-102.0	-110.0		dBm	Downlink RF level @ BER Class II < 2.4 %
Receiver input sensitivity DCS 1800	-102.0	-110.0		dBm	Downlink RF level @ BER Class II < 2.4 %
Receiver input sensitivity PCS 1900	-102.0	-110.0		dBm	Downlink RF level @ BER Class II < 2.4 %
Receiver input sensitivity UMTS 850 (band V)	-104.7	-112.0		dBm	Downlink RF level for RMC @ BER < 0.1 %
Receiver input sensitivity UMTS 900 (band VIII)	-103.7	-111.0		dBm	Downlink RF level for RMC @ BER < 0.1 %
Receiver input sensitivity UMTS 1900 (band II)	-104.7	-111.0		dBm	Downlink RF level for RMC @ BER < 0.1 %
Receiver input sensitivity UMTS 2100 (band I)	-106.7	-111.0		dBm	Downlink RF level for RMC @ BER < 0.1 %

Condition: 50 Ω source

Table 14: Receiver sensitivity performance

Parameter	Min.	Typ.	Max.	Unit	Remarks
Maximum output power GSM 850		32.5		dBm	Uplink burst RF power for GSM or GPRS 1-slot TCH at PCL 5 or Gamma 3
		32.5		dBm	Uplink burst RF power for GPRS 2-slot TCH at Gamma 3
		31.7		dBm	Uplink burst RF power for GPRS 3-slot TCH at Gamma 3
		30.5		dBm	Uplink burst RF power for GPRS 4-slot TCH at Gamma 3
		27.0		dBm	Uplink burst RF power for EDGE 8PSK 1-slot TCH at PCL 8 or Gamma 6
		27.0		dBm	Uplink burst RF power for EDGE 8PSK 2-slot TCH at Gamma 6
		26.2		dBm	Uplink burst RF power for EDGE 8PSK 3-slot TCH at Gamma 6
		25.0		dBm	Uplink burst RF power for EDGE 8PSK 4-slot TCH at Gamma 6
Maximum output power E-GSM 900		32.5		dBm	Uplink burst RF power for GSM or GPRS 1-slot TCH at PCL 5 or Gamma 3
		32.5		dBm	Uplink burst RF power for GPRS 2-slot TCH at Gamma 3
		31.7		dBm	Uplink burst RF power for GPRS 3-slot TCH at Gamma 3
		30.5		dBm	Uplink burst RF power for GPRS 4-slot TCH at Gamma 3
		27.0		dBm	Uplink burst RF power for EDGE 8PSK 1-slot TCH at PCL 8 or Gamma 6
		27.0		dBm	Uplink burst RF power for EDGE 8PSK 2-slot TCH at Gamma 6
		26.2		dBm	Uplink burst RF power for EDGE 8PSK 3-slot TCH at Gamma 6
		25.0		dBm	Uplink burst RF power for EDGE 8PSK 4-slot TCH at Gamma 6
Maximum output power DCS 1800		29.5		dBm	Uplink burst RF power for GSM or GPRS 1-slot TCH at PCL 0 or Gamma 3
		29.5		dBm	Uplink burst RF power for GPRS 2-slot TCH at Gamma 3
		28.7		dBm	Uplink burst RF power for GPRS 3-slot TCH at Gamma 3
		27.5		dBm	Uplink burst RF power for GPRS 4-slot TCH at Gamma 3
		26.0		dBm	Uplink burst RF power for EDGE 8PSK 1-slot TCH at PCL 2 or Gamma 5
		26.0		dBm	Uplink burst RF power for EDGE 8PSK 2-slot TCH at Gamma 5
		25.2		dBm	Uplink burst RF power for EDGE 8PSK 3-slot TCH at Gamma 5
		24.0		dBm	Uplink burst RF power for EDGE 8PSK 4-slot TCH at Gamma 5
Maximum output power PCS 1900		29.5		dBm	Uplink burst RF power for GSM or GPRS 1-slot TCH at PCL 0 or Gamma 3
		29.5		dBm	Uplink burst RF power for GPRS 2-slot TCH at Gamma 3
		28.7		dBm	Uplink burst RF power for GPRS 3-slot TCH at Gamma 3
		27.5		dBm	Uplink burst RF power for GPRS 4-slot TCH at Gamma 3
		26.0		dBm	Uplink burst RF power for EDGE 8PSK 1-slot TCH at PCL 2 or Gamma 5
		26.0		dBm	Uplink burst RF power for EDGE 8PSK 2-slot TCH at Gamma 5
		25.2		dBm	Uplink burst RF power for EDGE 8PSK 3-slot TCH at Gamma 5
		24.0		dBm	Uplink burst RF power for EDGE 8PSK 4-slot TCH at Gamma 5
Maximum output power UMTS 850 (Band V)		23.0		dBm	Uplink continuous RF power for RMC at maximum power
Maximum output power UMTS 900 (Band VIII)		23.0		dBm	Uplink continuous RF power for RMC at maximum power
Maximum output power UMTS 1900 (Band II)		23.0		dBm	Uplink continuous RF power for RMC at maximum power
Maximum output power UMTS 2100 (Band I)		23.0		dBm	Uplink continuous RF power for RMC at maximum power

Condition: 50 Ω output load

Table 15: Transmitter maximum output power

4.2.6 PWR_ON pin

Pin Name	Parameter	Min.	Typ.	Max.	Unit	Remarks
PWR_ON	Internal supply for Power-On Input Signal	2.18	2.30	2.41	V	RTC supply (V_BCKP)
	L-level input	-0.30		0.65	V	High input impedance (no internal pull-up)
	H-level input	2.00		4.50	V	High input impedance (no internal pull-up)
	L-level input current		-8		µA	
	PWR_ON low time to switch-on the module	5			ms	

Table 16: PWR_ON pin characteristics (POS domain)

4.2.7 RESET_N pin

Pin Name	Parameter	Min.	Typ.	Max.	Unit	Remarks
RESET_N	Internal supply for External Reset Input Signal	2.18	2.30	2.41	V	RTC supply (V_BCKP)
	L-level input	-0.30		0.65	V	
	H-level input	1.69		2.48	V	
	L-level input current		-230		µA	
	Pull-up resistance		10		kΩ	Internal pull-up to RTC supply (V_BCKP)
	RESET_N low time to perform a proper reset	50			ms	

Table 17: RESET_N pin characteristics (ERS domain)

4.2.8 (U)SIM pins

The SIM pins are a dedicated interface to the (U)SIM chip card/IC. The electrical characteristics fulfill regulatory specification requirements. The values in Table 18 are for information only.

Parameter	Min.	Typ.	Max.	Unit	Remarks
Low-level input	0.00		0.36	V	VSIM = 1.80 V
	0.00		0.58	V	VSIM = 2.90 V
High-level input	1.26		3.30	V	VSIM = 1.80 V
	2.03		3.30	V	VSIM = 2.90 V
Low-level output		0.00	0.20	V	VSIM = 1.80 V, Max value at I_{OL} = +1.0 mA
		0.00	0.20	V	VSIM = 2.90 V, Max value at I_{OL} = +1.0 mA
High-level output	1.60	1.80		V	VSIM = 1.80 V, Min value at I_{OH} = -1.0 mA
	2.70	2.90		V	VSIM = 2.90 V, Min value at I_{OH} = -1.0 mA
Input/Output leakage current			0.7	µA	0.2V < V_{IN} < 3.3V
Internal pull-up resistor on SIM_IO to VSIM		4.7		kΩ	
Clock frequency on SIM_CLK		3.25		MHz	

Table 18: (U)SIM pins characteristics (SIM domain)

4.2.9 Generic Digital Interfaces pins

Parameter	Min.	Typ.	Max.	Unit	Remarks
Internal supply for GDI domain	1.77	1.80	1.83	V	Digital I/O Interfaces supply (V_INT)
Input characteristic: L-level input	-0.20		0.35	V	
Input characteristic: H-level input	1.28		1.97	V	
Output characteristics: L-level output		0.00	0.20	V	Max value at I_{OL} = +0.1mA for driver class A
		0.00	0.35	V	Max value at I_{OL} = +8.0mA for driver class A
		0.00	0.20	V	Max value at I_{OL} = +0.1mA for driver class B
		0.00	0.35	V	Max value at I_{OL} = +4.0mA for driver class B
		0.00	0.20	V	Max value at I_{OL} = +0.1mA for driver class C
		0.00	0.35	V	Max value at I_{OL} = +2.5mA for driver class C
		0.00	0.54	V	Max value at I_{OL} = +1.0mA for driver class C_0
		0.00	0.20	V	Max value at I_{OL} = +0.1mA for driver class D
		0.00	0.35	V	Max value at I_{OL} = +1.0mA for driver class D
Output characteristics: H-level output	1.45	1.80		V	Min value at I_{OH} = -8.0mA for driver class A
	1.60	1.80		V	Min value at I_{OH} = -0.1mA for driver class A
	1.45	1.80		V	Min value at I_{OH} = -4.0mA for driver class B
	1.60	1.80		V	Min value at I_{OH} = -0.1mA for driver class B
	1.45	1.80		V	Min value at I_{OH} = -2.0mA for driver class C
	1.60	1.80		V	Min value at I_{OH} = -0.1mA for driver class C
	1.26	1.80		V	Min value at I_{OH} = -1.0mA for driver class C_0
	1.45	1.80		V	Min value at I_{OH} = -1.0mA for driver class D
	1.60	1.80		V	Min value at I_{OH} = -0.1mA for driver class D
Input/Output leakage current			0.7	µA	0.2 V < V_{IN} < 1.97 V
Pull-up input current			-220	µA	PU/PD Class a
			-110	µA	PU/PD Class b
			-100	µA	PU/PD Class b_0
			-60	µA	PU/PD Class c
Pull-down input current			+200	µA	PU/PD Class a
			+100	µA	PU/PD Class b
			+85	µA	PU/PD Class b_0
			+55	µA	PU/PD Class c

Table 19: Generic Digital Interfaces pins characteristics (GDI domain)

4.2.9.1 AC characteristics of digital audio interfaces pins (LISA-U120 and LISA-U130 only)

The 4-wire I²S digital audio interface can be configured in 4 modes:

- Normal I²S mode – Master mode
- Normal I²S mode – Slave mode
- PCM mode – Master mode
- PCM mode – Slave mode

LISA-U120-00S and LISA-U130-00S versions don't support I²S slave mode: module acts as master only.

The sample rate (i.e. word alignment frequency) of transmitted and received words of LISA-U120-00S and LISA-U130-00S versions cannot be configured by the <I2S_sample_rate> parameter of the AT+UI2S command: the sample rate is fixed at 8 kHz (i.e. the <I2S_sample_rate> parameter is fixed to 0).

Normal I²S mode – Master mode

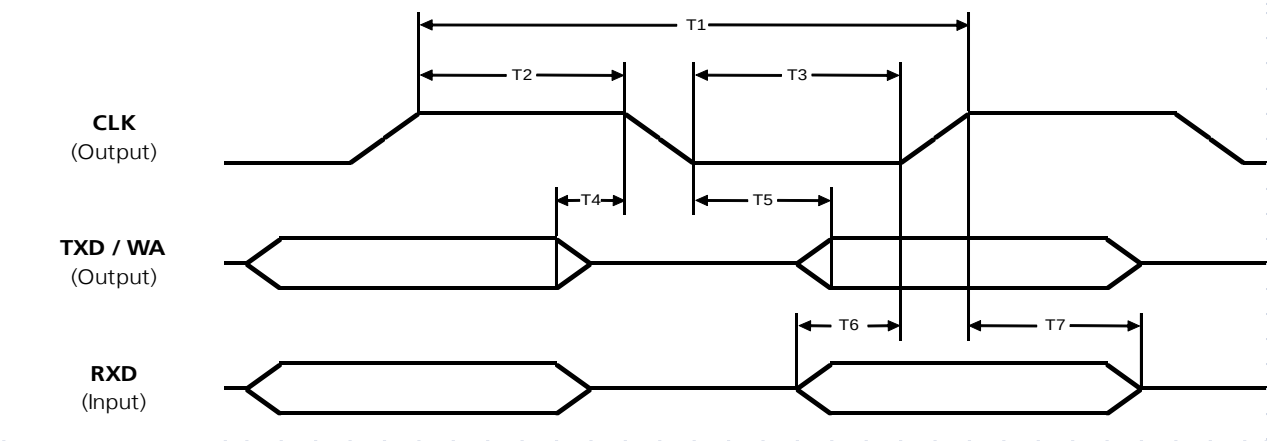

Figure 5: AC characteristics of digital audio interface in Normal I²S mode (<I2S_mode> = 2,4,6,8,10,12) and Master mode enabled

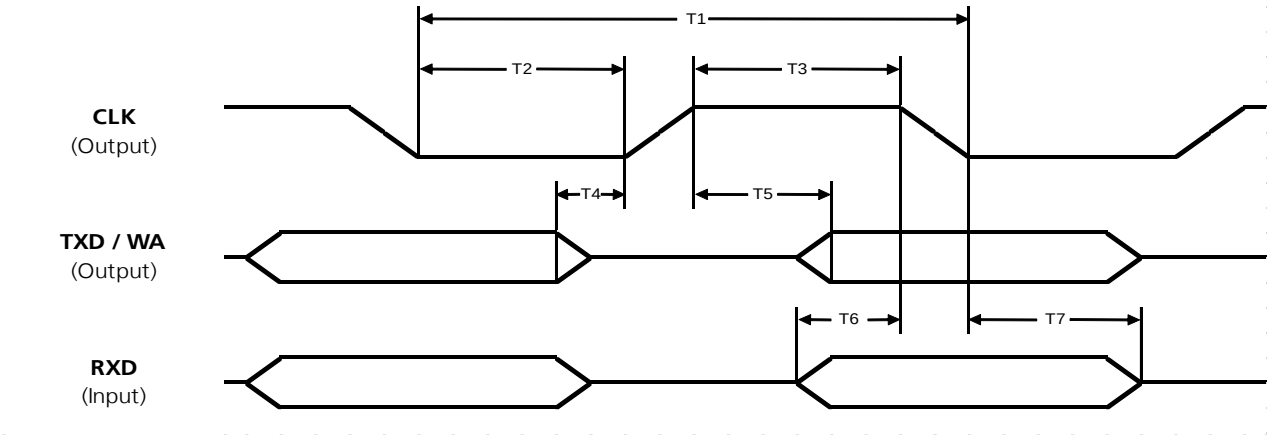

Figure 6: AC characteristics of digital audio interface in Normal I²S mode (<I2S_mode> = 3,5,7,9,11,13) and Master mode enabled

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T1	I²S clock period	3.902	3.906		µs	<I2S_sample_rate>=0
		2.830	2.834		µs	<I2S_sample_rate>=1
		2.600	2.604		µs	<I2S_sample_rate>=2
		1.949	1.953		µs	<I2S_sample_rate>=3
		1.413	1.417		µs	<I2S_sample_rate>=4
		1.298	1.302		µs	<I2S_sample_rate>=5
		0.973	0.977		µs	<I2S_sample_rate>=6
		0.705	0.709		µs	<I2S_sample_rate>=7
		0.647	0.651		µs	<I2S_sample_rate>=8
1/T1	I²S clock frequency		256.0	256.3	kHz	<I2S_sample_rate>=0
			352.8	353.3	kHz	<I2S_sample_rate>=1
			384.0	384.6	kHz	<I2S_sample_rate>=2
			512.0	513.1	kHz	<I2S_sample_rate>=3
			705.6	707.6	kHz	<I2S_sample_rate>=4
			768.0	770.4	kHz	<I2S_sample_rate>=5

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
			1024	1028	kHz	<I2S_sample_rate>=6
			1411	1419	kHz	<I2S_sample_rate>=7
			1536	1545	kHz	<I2S_sample_rate>=8
T2	I²S clock high time	1.933	1.953		µs	<I2S_sample_rate>=0
		1.397	1.417		µs	<I2S_sample_rate>=1
		1.282	1.302		µs	<I2S_sample_rate>=2
		0.957	0.977		µs	<I2S_sample_rate>=3
		0.689	0.709		µs	<I2S_sample_rate>=4
		0.631	0.651		µs	<I2S_sample_rate>=5
		0.468	0.488		µs	<I2S_sample_rate>=6
		0.334	0.354		µs	<I2S_sample_rate>=7
		0.306	0.326		µs	<I2S_sample_rate>=8
T3	I²S clock low time	1.933	1.953		µs	<I2S_sample_rate>=0
		1.397	1.417		µs	<I2S_sample_rate>=1
		1.282	1.302		µs	<I2S_sample_rate>=2
		0.957	0.977		µs	<I2S_sample_rate>=3
		0.689	0.709		µs	<I2S_sample_rate>=4
		0.631	0.651		µs	<I2S_sample_rate>=5
		0.468	0.488		µs	<I2S_sample_rate>=6
		0.334	0.354		µs	<I2S_sample_rate>=7
		0.306	0.326		µs	<I2S_sample_rate>=8
	I²S word alignment period		125.0		µs	<I2S_sample_rate>=0
			90.70		µs	<I2S_sample_rate>=1
			83.33		µs	<I2S_sample_rate>=2
			62.50		µs	<I2S_sample_rate>=3
			45.35		µs	<I2S_sample_rate>=4
			41.67		µs	<I2S_sample_rate>=5
			31.25		µs	<I2S_sample_rate>=6
			22.68		µs	<I2S_sample_rate>=7
			20.83		µs	<I2S_sample_rate>=8
	I²S word alignment frequency		8.000		kHz	<I2S_sample_rate>=0
			11.03		kHz	<I2S_sample_rate>=1
			12.00		kHz	<I2S_sample_rate>=2
			16.00		kHz	<I2S_sample_rate>=3
			22.05		kHz	<I2S_sample_rate>=4
			24.00		kHz	<I2S_sample_rate>=5
			32.00		kHz	<I2S_sample_rate>=6
			44.10		kHz	<I2S_sample_rate>=7
			48.00		kHz	<I2S_sample_rate>=8
T4	I2S TXD invalid before I2S CLK high end (before shifting edge of I2S CLK)			24	ns	<I2S_mode> = 2,4,6,8,10,12
	I2S TXD invalid before I2S CLK low end (before shifting edge of I2S CLK)			24	ns	<I2S_mode> = 3,5,7,9,11,13
T5	I2S TXD valid after I2S CLK low begin (after shifting edge of I2S CLK)			32	ns	<I2S_mode> = 2,4,6,8,10,12
	I2S TXD valid after I2S CLK high begin (after shifting edge of I2S CLK)			32	ns	<I2S_mode> = 3,5,7,9,11,13
T6	I2S RXD setup time before I2S CLK low end (before latching edge of I2S CLK)	60			ns	<I2S_mode> = 2,4,6,8,10,12
	I2S RXD setup time before I2S CLK high end (before latching edge of I2S CLK)	60			ns	<I2S_mode> = 3,5,7,9,11,13

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T7	I2S RXD hold time after I2S CLK high begin (after latching edge of I2S CLK)	10			ns	<I2S_mode> = 2,4,6,8,10,12
	I2S RXD hold time after I2S CLK low begin (after latching edge of I2S CLK)	10			ns	<I2S_mode> = 3,5,7,9,11,13

Table 20: AC characteristics of digital audio interface in Normal I²S mode and Master mode enabled

Normal I²S mode – Slave mode (LISA-U120 and LISA-U130 only)

☞ LISA-U120-00S and LISA-U130-00S versions don't support normal I²S slave mode.

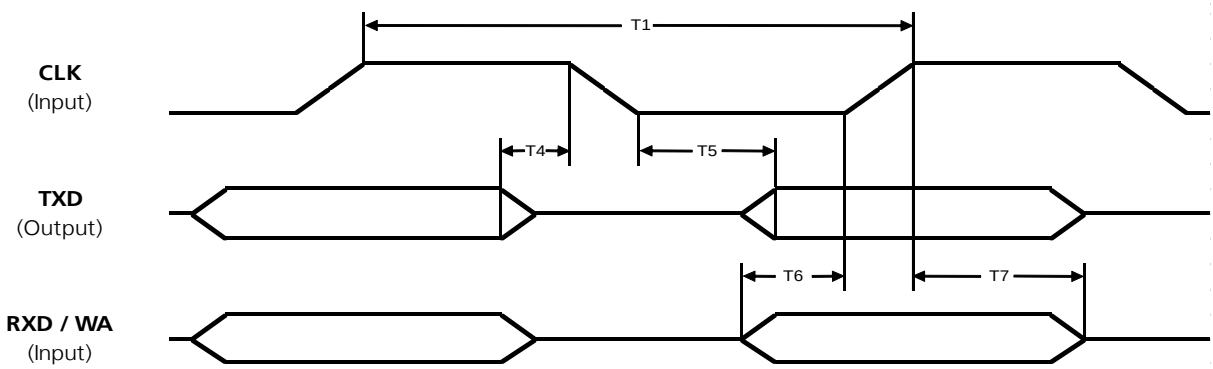

Figure 7: AC characteristics of digital audio interface in Normal I²S mode (<I2S_mode> = 2,4,6,8,10,12) and Slave mode enabled

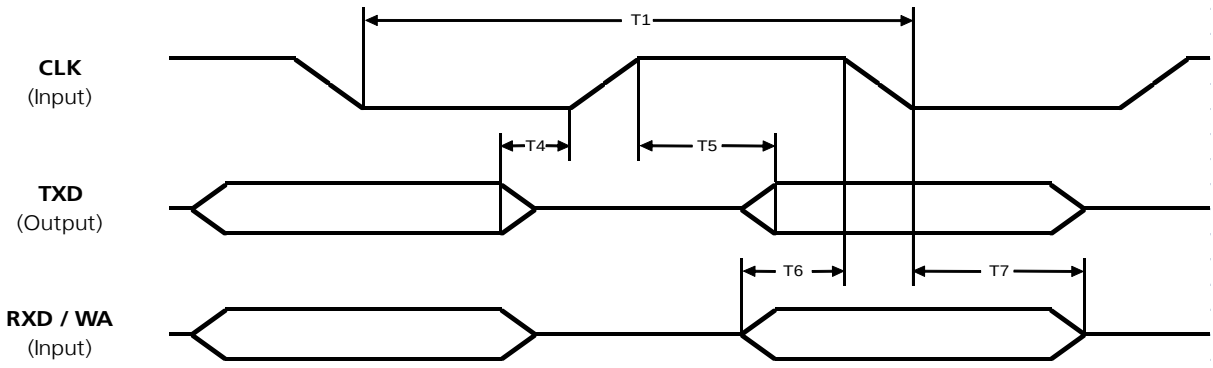

Figure 8: AC characteristics of digital audio interface in Normal I²S mode (<I2S_mode> = 3,5,7,9,11,13) and Slave mode enabled

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T1	I²S clock period	3.906			µs	<I2S_sample_rate>=0
		2.834			µs	<I2S_sample_rate>=1
		2.604			µs	<I2S_sample_rate>=2
		1.953			µs	<I2S_sample_rate>=3
		1.417			µs	<I2S_sample_rate>=4
		1.302			µs	<I2S_sample_rate>=5
		0.977			µs	<I2S_sample_rate>=6

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
		0.709			µs	<I2S_sample_rate>=7
		0.651			µs	<I2S_sample_rate>=8
1/T1	I²S clock frequency			256.0	kHz	<I2S_sample_rate>=0
				352.8	kHz	<I2S_sample_rate>=1
				384.0	kHz	<I2S_sample_rate>=2
				512.0	kHz	<I2S_sample_rate>=3
				705.6	kHz	<I2S_sample_rate>=4
				768.0	kHz	<I2S_sample_rate>=5
				1024	kHz	<I2S_sample_rate>=6
				1411	kHz	<I2S_sample_rate>=7
				1536	kHz	<I2S_sample_rate>=8
	I²S word alignment period	125.0			µs	<I2S_sample_rate>=0
		90.70			µs	<I2S_sample_rate>=1
		83.33			µs	<I2S_sample_rate>=2
		62.50			µs	<I2S_sample_rate>=3
		45.35			µs	<I2S_sample_rate>=4
		41.67			µs	<I2S_sample_rate>=5
		31.25			µs	<I2S_sample_rate>=6
		22.68			µs	<I2S_sample_rate>=7
		20.83			µs	<I2S_sample_rate>=8
	I²S word alignment frequency			8.000	kHz	<I2S_sample_rate>=0
				11.03	kHz	<I2S_sample_rate>=1
				12.00	kHz	<I2S_sample_rate>=2
				16.00	kHz	<I2S_sample_rate>=3
				22.05	kHz	<I2S_sample_rate>=4
				24.00	kHz	<I2S_sample_rate>=5
				32.00	kHz	<I2S_sample_rate>=6
				44.10	kHz	<I2S_sample_rate>=7
				48.00	kHz	<I2S_sample_rate>=8
T4	I2S TXD invalid before I2S CLK falling edge (before shifting edge of I2S CLK)			24	ns	<I2S_mode> = 2,4,6,8,10,12
	I2S TXD invalid before I2S CLK rising edge (before shifting edge of I2S CLK)			24	ns	<I2S_mode> = 3,5,7,9,11,13
T5	I2S TXD valid after I2S CLK falling edge (after shifting edge of I2S CLK)			32	ns	<I2S_mode> = 2,4,6,8,10,12
	I2S TXD valid after I2S CLK rising edge (after shifting edge of I2S CLK)			32	ns	<I2S_mode> = 3,5,7,9,11,13
T6	I2S RXD setup time before I2S CLK rising edge (before latching edge of I2S CLK)	60			ns	<I2S_mode> = 2,4,6,8,10,12
	I2S RXD setup time before I2S CLK falling edge (before latching edge of I2S CLK)	60			ns	<I2S_mode> = 3,5,7,9,11,13
T7	I2S RXD hold time after I2S CLK rising edge (after latching edge of I2S CLK)	10			ns	<I2S_mode> = 2,4,6,8,10,12
	I2S RXD hold time after I2S CLK falling edge (after latching edge of I2S CLK)	10			ns	<I2S_mode> = 3,5,7,9,11,13

Table 21: AC characteristics of digital audio interface in Normal I²S mode and Slave mode enabled

PCM mode – Master mode

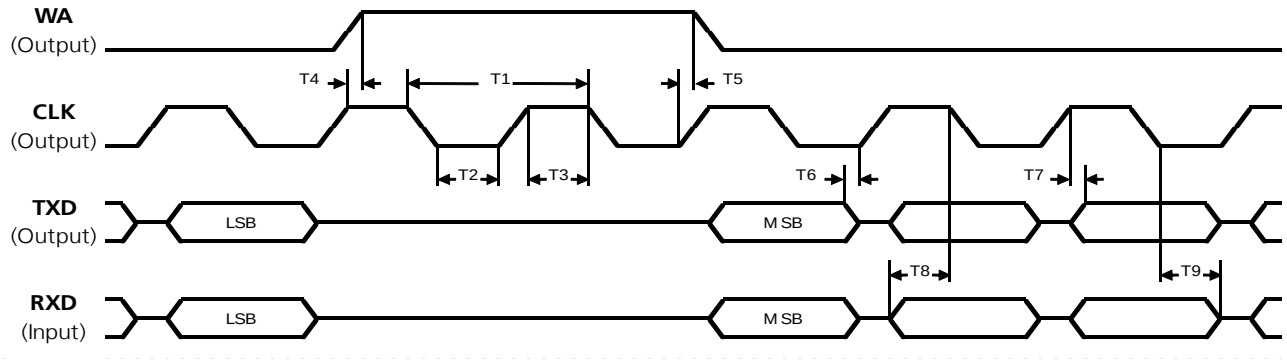

Figure 9: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 0) and Master mode enabled

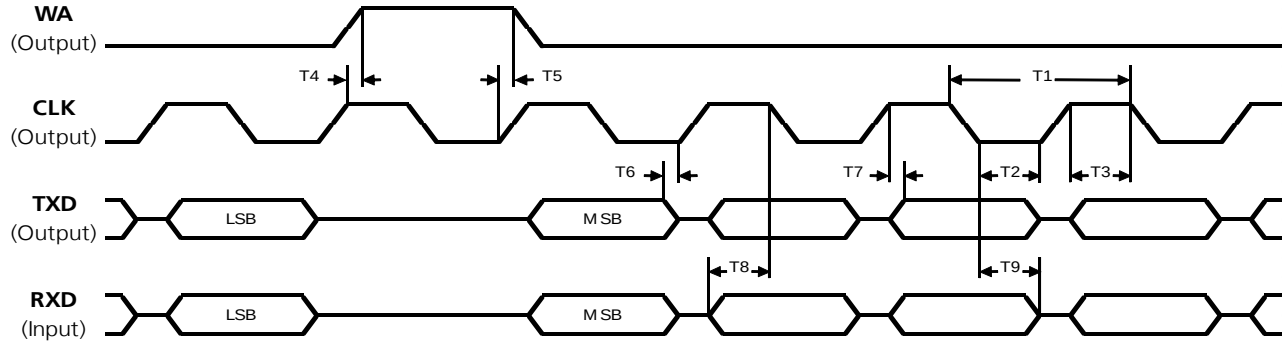

Figure 10: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 1) and Master mode enabled

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T1	I^2S clock period	6.940	6.944		µs	<I2S_mode>=0, <I2S_sample_rate>=0
		7.349	7.353		µs	<I2S_mode>=1, <I2S_sample_rate>=0
		5.035	5.039		µs	<I2S_mode>=0, <I2S_sample_rate>=1
		5.331	5.335		µs	<I2S_mode>=1, <I2S_sample_rate>=1
		4.626	4.630		µs	<I2S_mode>=0, <I2S_sample_rate>=2
		4.898	4.902		µs	<I2S_mode>=1, <I2S_sample_rate>=2
		3.468	3.472		µs	<I2S_mode>=0, <I2S_sample_rate>=3
		3.672	3.676		µs	<I2S_mode>=1, <I2S_sample_rate>=3
		2.516	2.520		µs	<I2S_mode>=0, <I2S_sample_rate>=4
		2.664	2.668		µs	<I2S_mode>=1, <I2S_sample_rate>=4
		2.311	2.315		µs	<I2S_mode>=0, <I2S_sample_rate>=5
		2.447	2.451		µs	<I2S_mode>=1, <I2S_sample_rate>=5
		1.732	1.736		µs	<I2S_mode>=0, <I2S_sample_rate>=6
		1.834	1.838		µs	<I2S_mode>=1, <I2S_sample_rate>=6
		1.256	1.260		µs	<I2S_mode>=0, <I2S_sample_rate>=7
		1.330	1.334		µs	<I2S_mode>=1, <I2S_sample_rate>=7
		1.153	1.157		µs	<I2S_mode>=0, <I2S_sample_rate>=8
		1.221	1.225		µs	<I2S_mode>=1, <I2S_sample_rate>=8
1/T1	I^2S clock frequency		144.0	144.1	kHz	<I2S_mode>=0, <I2S_sample_rate>=0
			136.0	136.1	kHz	<I2S_mode>=1, <I2S_sample_rate>=0

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
			198.5	198.6	kHz	<I2S_mode>=0, <I2S_sample_rate>=1
			187.4	187.6	kHz	<I2S_mode>=1, <I2S_sample_rate>=1
			216.0	216.2	kHz	<I2S_mode>=0, <I2S_sample_rate>=2
			204.0	204.2	kHz	<I2S_mode>=1, <I2S_sample_rate>=2
			288.0	288.3	kHz	<I2S_mode>=0, <I2S_sample_rate>=3
			272.0	272.3	kHz	<I2S_mode>=1, <I2S_sample_rate>=3
			396.9	397.5	kHz	<I2S_mode>=0, <I2S_sample_rate>=4
			374.9	375.4	kHz	<I2S_mode>=1, <I2S_sample_rate>=4
			432.0	432.7	kHz	<I2S_mode>=0, <I2S_sample_rate>=5
			408.0	408.7	kHz	<I2S_mode>=1, <I2S_sample_rate>=5
			576.0	577.3	kHz	<I2S_mode>=0, <I2S_sample_rate>=6
			544.0	545.2	kHz	<I2S_mode>=1, <I2S_sample_rate>=6
			793.8	796.3	kHz	<I2S_mode>=0, <I2S_sample_rate>=7
			749.7	752.0	kHz	<I2S_mode>=1, <I2S_sample_rate>=7
			864.0	867.0	kHz	<I2S_mode>=0, <I2S_sample_rate>=8
			816.0	818.7	kHz	<I2S_mode>=1, <I2S_sample_rate>=8
T2	I²S clock low time	3.452	3.472		µs	<I2S_mode>=0, <I2S_sample_rate>=0
		3.656	3.676		µs	<I2S_mode>=1, <I2S_sample_rate>=0
		2.500	2.520		µs	<I2S_mode>=0, <I2S_sample_rate>=1
		2.648	2.668		µs	<I2S_mode>=1, <I2S_sample_rate>=1
		2.295	2.315		µs	<I2S_mode>=0, <I2S_sample_rate>=2
		2.431	2.451		µs	<I2S_mode>=1, <I2S_sample_rate>=2
		1.716	1.736		µs	<I2S_mode>=0, <I2S_sample_rate>=3
		1.818	1.838		µs	<I2S_mode>=1, <I2S_sample_rate>=3
		1.240	1.260		µs	<I2S_mode>=0, <I2S_sample_rate>=4
		1.314	1.334		µs	<I2S_mode>=1, <I2S_sample_rate>=4
		1.137	1.157		µs	<I2S_mode>=0, <I2S_sample_rate>=5
		1.205	1.225		µs	<I2S_mode>=1, <I2S_sample_rate>=5
		0.848	0.868		µs	<I2S_mode>=0, <I2S_sample_rate>=6
		0.899	0.919		µs	<I2S_mode>=1, <I2S_sample_rate>=6
		0.610	0.630		µs	<I2S_mode>=0, <I2S_sample_rate>=7
		0.647	0.667		µs	<I2S_mode>=1, <I2S_sample_rate>=7
		0.559	0.579		µs	<I2S_mode>=0, <I2S_sample_rate>=8
		0.593	0.613		µs	<I2S_mode>=1, <I2S_sample_rate>=8
T3	I²S clock high time	3.452	3.472		µs	<I2S_mode>=0, <I2S_sample_rate>=0
		3.656	3.676		µs	<I2S_mode>=1, <I2S_sample_rate>=0
		2.500	2.520		µs	<I2S_mode>=0, <I2S_sample_rate>=1
		2.648	2.668		µs	<I2S_mode>=1, <I2S_sample_rate>=1
		2.295	2.315		µs	<I2S_mode>=0, <I2S_sample_rate>=2
		2.431	2.451		µs	<I2S_mode>=1, <I2S_sample_rate>=2
		1.716	1.736		µs	<I2S_mode>=0, <I2S_sample_rate>=3
		1.818	1.838		µs	<I2S_mode>=1, <I2S_sample_rate>=3
		1.240	1.260		µs	<I2S_mode>=0, <I2S_sample_rate>=4
		1.314	1.334		µs	<I2S_mode>=1, <I2S_sample_rate>=4
		1.137	1.157		µs	<I2S_mode>=0, <I2S_sample_rate>=5
		1.205	1.225		µs	<I2S_mode>=1, <I2S_sample_rate>=5
		0.848	0.868		µs	<I2S_mode>=0, <I2S_sample_rate>=6
		0.899	0.919		µs	<I2S_mode>=1, <I2S_sample_rate>=6
		0.610	0.630		µs	<I2S_mode>=0, <I2S_sample_rate>=7
		0.647	0.667		µs	<I2S_mode>=1, <I2S_sample_rate>=7
		0.559	0.579		µs	<I2S_mode>=0, <I2S_sample_rate>=8
		0.593	0.613		µs	<I2S_mode>=1, <I2S_sample_rate>=8

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
	I2S word alignment period		125.0		µs	<I2S_sample_rate>=0
			90.70		µs	<I2S_sample_rate>=1
			83.33		µs	<I2S_sample_rate>=2
			62.50		µs	<I2S_sample_rate>=3
			45.35		µs	<I2S_sample_rate>=4
			41.67		µs	<I2S_sample_rate>=5
			31.25		µs	<I2S_sample_rate>=6
			22.68		µs	<I2S_sample_rate>=7
			20.83		µs	<I2S_sample_rate>=8
	I2S word alignment frequency		8.000		kHz	<I2S_sample_rate>=0
			11.03		kHz	<I2S_sample_rate>=1
			12.00		kHz	<I2S_sample_rate>=2
			16.00		kHz	<I2S_sample_rate>=3
			22.05		kHz	<I2S_sample_rate>=4
			24.00		kHz	<I2S_sample_rate>=5
			32.00		kHz	<I2S_sample_rate>=6
			44.10		kHz	<I2S_sample_rate>=7
			48.00		kHz	<I2S_sample_rate>=8
T4	I2S CLK high begin to I2S WA high begin	-24		32	ns	<I2S_mode> = 0
T5	I2S CLK low end to I2S WA high end	-24		32	ns	<I2S_mode> = 0
T6	I2S TXD invalid before I2S CLK low end			24	ns	<I2S_mode> = 0
T7	I2S TXD valid after I2S CLK high begin			22	ns	<I2S_mode> = 0
T8	I2S RXD setup time before I2S CLK high end	60			ns	<I2S_mode> = 0
T9	I2S RXD hold time after I2S CLK low begin	12			ns	<I2S_mode> = 0

Table 22: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 0,1) and Master mode enabled

PCM mode – Slave mode (LISA-U120 and LISA-U130 only)

LISA-U120-00S and LISA-U130-00S versions don't support PCM slave mode.

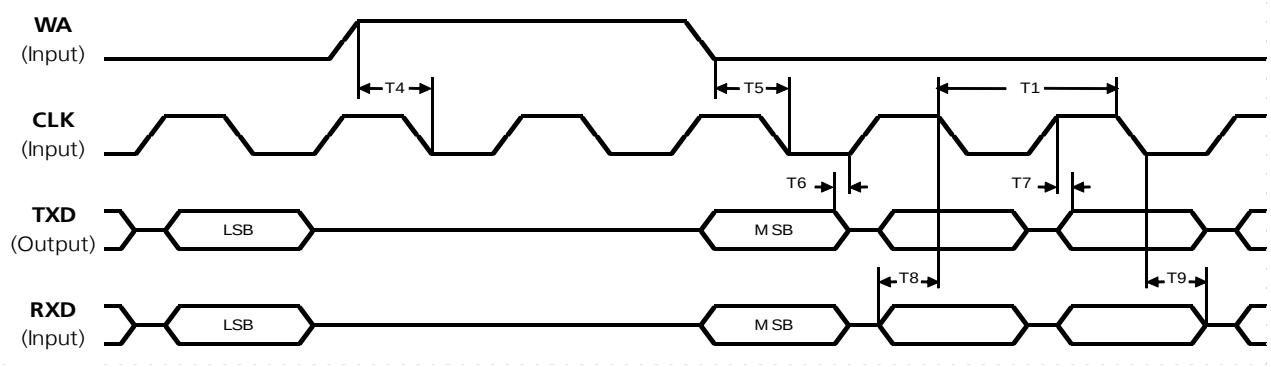

Figure 11: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 0) and Slave mode enabled

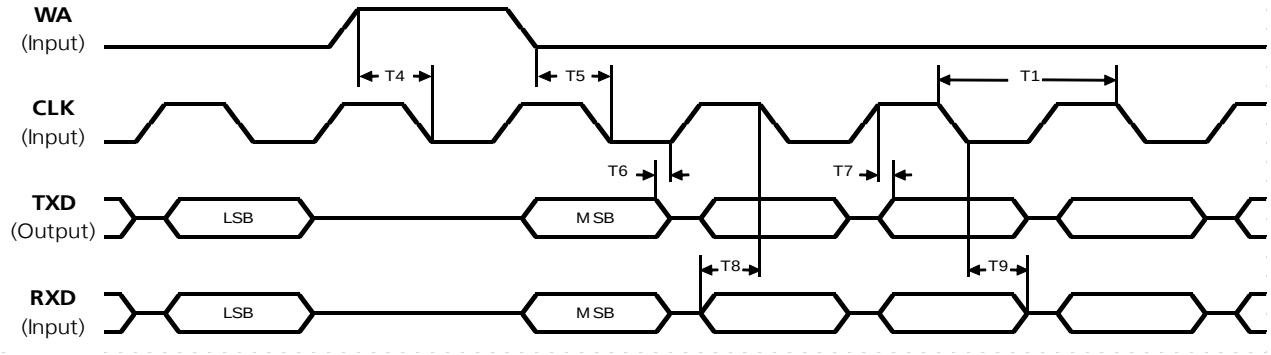

Figure 12: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 1) and Slave mode enabled

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T1	I^2S clock period	6.944			µs	<I2S_mode>=0, <I2S_sample_rate>=0
		7.353			µs	<I2S_mode>=1, <I2S_sample_rate>=0
		5.039			µs	<I2S_mode>=0, <I2S_sample_rate>=1
		5.335			µs	<I2S_mode>=1, <I2S_sample_rate>=1
		4.630			µs	<I2S_mode>=0, <I2S_sample_rate>=2
		4.902			µs	<I2S_mode>=1, <I2S_sample_rate>=2
		3.472			µs	<I2S_mode>=0, <I2S_sample_rate>=3
		3.676			µs	<I2S_mode>=1, <I2S_sample_rate>=3
		2.520			µs	<I2S_mode>=0, <I2S_sample_rate>=4
		2.668			µs	<I2S_mode>=1, <I2S_sample_rate>=4
		2.315			µs	<I2S_mode>=0, <I2S_sample_rate>=5
		2.451			µs	<I2S_mode>=1, <I2S_sample_rate>=5
		1.736			µs	<I2S_mode>=0, <I2S_sample_rate>=6
		1.838			µs	<I2S_mode>=1, <I2S_sample_rate>=6
		1.260			µs	<I2S_mode>=0, <I2S_sample_rate>=7
		1.334			µs	<I2S_mode>=1, <I2S_sample_rate>=7
		1.157			µs	<I2S_mode>=0, <I2S_sample_rate>=8

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
		1.225			µs	<I2S_mode>=1, <I2S_sample_rate>=8
1/T1	I²S clock frequency	144.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=0
		136.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=0
		198.5			kHz	<I2S_mode>=0, <I2S_sample_rate>=1
		187.4			kHz	<I2S_mode>=1, <I2S_sample_rate>=1
		216.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=2
		204.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=2
		288.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=3
		272.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=3
		396.9			kHz	<I2S_mode>=0, <I2S_sample_rate>=4
		374.9			kHz	<I2S_mode>=1, <I2S_sample_rate>=4
		432.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=5
		408.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=5
		576.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=6
		544.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=6
		793.8			kHz	<I2S_mode>=0, <I2S_sample_rate>=7
		749.7			kHz	<I2S_mode>=1, <I2S_sample_rate>=7
		864.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=8
		816.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=8
	I²S word alignment period		125.0		µs	<I2S_sample_rate>=0
			90.70		µs	<I2S_sample_rate>=1
			83.33		µs	<I2S_sample_rate>=2
			62.50		µs	<I2S_sample_rate>=3
			45.35		µs	<I2S_sample_rate>=4
			41.67		µs	<I2S_sample_rate>=5
			31.25		µs	<I2S_sample_rate>=6
			22.68		µs	<I2S_sample_rate>=7
			20.83		µs	<I2S_sample_rate>=8
	I²S word alignment frequency		8.000		kHz	<I2S_sample_rate>=0
			11.03		kHz	<I2S_sample_rate>=1
			12.00		kHz	<I2S_sample_rate>=2
			16.00		kHz	<I2S_sample_rate>=3
			22.05		kHz	<I2S_sample_rate>=4
			24.00		kHz	<I2S_sample_rate>=5
			32.00		kHz	<I2S_sample_rate>=6
			44.10		kHz	<I2S_sample_rate>=7
			48.00		kHz	<I2S_sample_rate>=8
T4	I2S WA high begin before I2S CLK low begin (latching edge of I2S CLK)	36			ns	<I2S_mode> = 0
T5	I2S WA low begin before I2S CLK low begin (latching edge of I2S CLK)	36			ns	<I2S_mode> = 0
T6	I2S TXD invalid before I2S CLK rising edge (shifting edge of I2S CLK)			12	ns	<I2S_mode> = 0
T7	I²S TXD valid after I²S CLK rising edge (shifting edge of I²S CLK)			79	ns	<I2S_mode> = 0
T8	I²S RXD setup time before I²S CLK falling edge (latching edge of I²S CLK)	22			ns	<I2S_mode> = 0
T9	I²S RXD hold time after I²S CLK falling edge (latching edge of I²S CLK)	24			ns	<I2S_mode> = 0

Table 23: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 0,1) and Slave mode enabled

4.2.9.2 AC characteristics of SPI / IPC pins

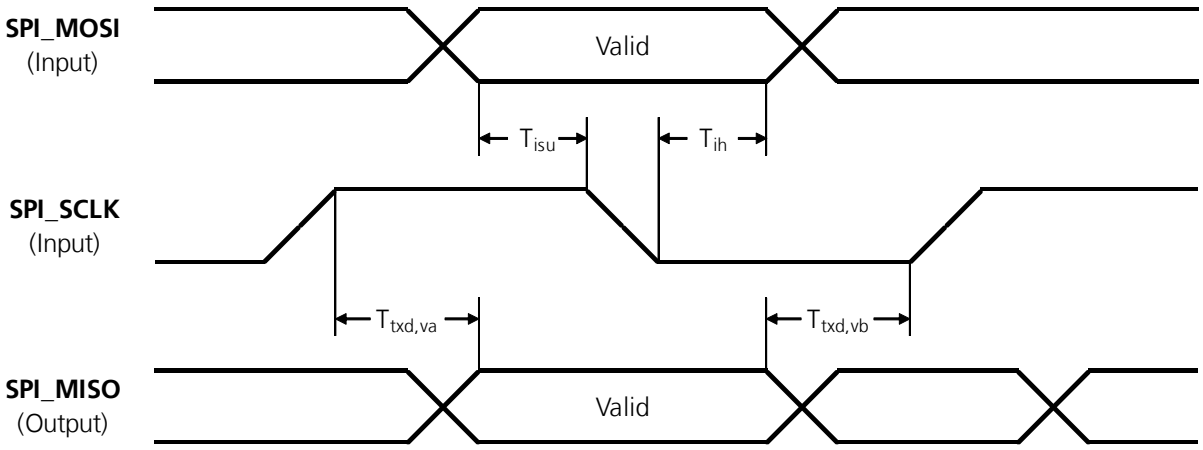

Figure 13: SPI_MOSI, SPI_MISO, SPI_SCLK timings

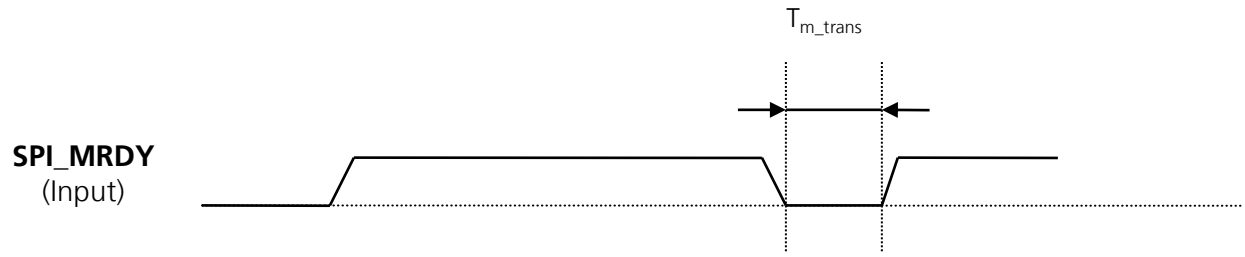

Figure 14: SPI_MRDY transition

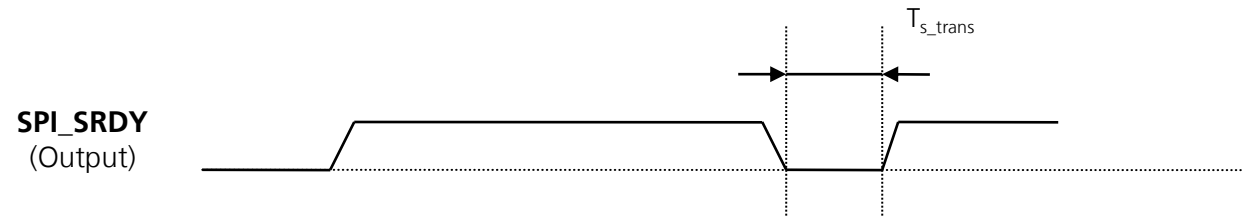

Figure 15: SPI_SRDY transition

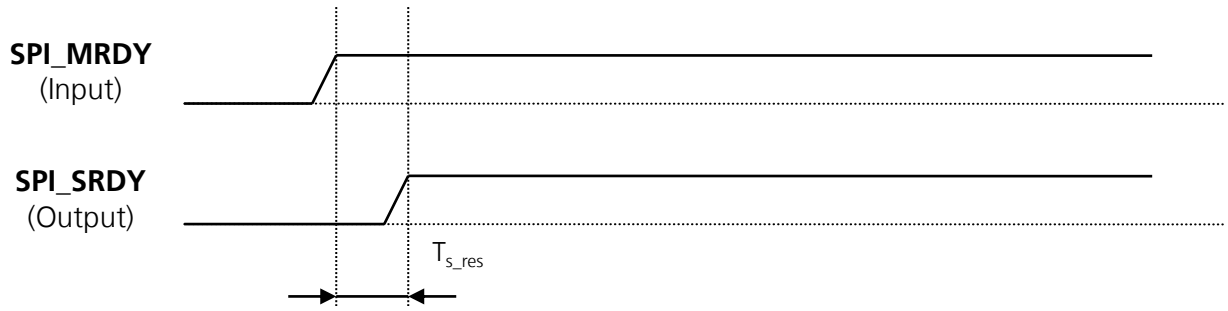

Figure 16: SPI_SRDY response

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
	SPI_SCLK frequency	0.26		26.0	MHz	
	SPI_SCLK period	38.5		3846.2	ns	
T_{isu}	Receive data setup time	5			ns	
T_{ih}	Receive data hold time	5			ns	
$T_{txd,va}$	Transmit data valid after clock rising edge			13	ns	
$T_{txd,vb}$	Transmit data valid before clock rising edge			0	ns	
T_{m_trans}	Time between two master data transfers	80			ns	Power saving disabled by AT+UPSV
		62			µs	Power saving enabled by AT+UPSV
T_{s_trans}	Time between two slave data transfers	80			ns	
T_{s_res}	SPI_SRDY active after SPI_MRDY active			200	µs	Power saving disabled by AT+UPSV
				10	ms	Power saving enabled by AT+UPSV

Table 24: AC characteristics of SPI interface

4.2.10 USB pins

USB data lines (**USB_D+** and **USB_D-**) are compliant to the USB 2.0 high-speed specification. Refer to the Universal Serial Bus Revision 2.0 specification [10] for detailed electrical characteristics.

Parameter	Min.	Typ.	Max.	Unit	Remarks
USB detection voltage on pin VUSB_DET	4.40	5.00	5.25	V	
Current sink at VUSB_DET		150		µA	
High-speed squelch detection threshold (input differential signal amplitude)	100		150	mV	
High speed disconnect detection threshold (input differential signal amplitude)	525		625	mV	
High-speed data signaling input common mode voltage range	-50		500	mV	
High-speed idle output level	-10		10	mV	
High-speed data signaling output high level	360		440	mV	
High-speed data signaling output low level	-10		10	mV	
Chirp J level (output differential voltage)	700		1100	mV	
Chirp K level (output differential voltage)	-900		-500	mV	

Table 25: USB pins characteristics

4.2.11 DDC (I²C) pins

DDC (I²C) lines (**SCL** and **SDA**) are compliant to the I²C-bus standard mode specification. Refer to the I²C-Bus Specification Version 2.1 [11] for detailed electrical characteristics.

Parameter	Min.	Typ.	Max.	Unit	Remarks
Internal supply for DDC domain	1.77	1.80	1.83	V	Digital I/O Interfaces supply (V_INT)
L-level input	-0.30		0.54	V	
H-level input	1.26		1.97	V	
L-level output		0.00	0.40	V	Max value at I_{OL} = +1.0 mA
Input/Output leakage current			0.7	µA	0.2 V < V_{IN} < 1.97 V
Clock frequency on SCL		100		kHz	

Table 26: DDC (I²C) pins characteristics (DDC domain)

4.2.12 Audio pins (LISA-U120 and LISA-U130 only)

Pin Name	Parameter	Min.	Typ.	Max.	Unit	Remarks
MIC_P/MIC_N	Differential input voltage			0.8	Vpp	Full scale differential voltage
	Differential input resistance		50		kΩ	
	Input capacitance		100		nF	Internal DC blocking capacitor at MIC_P and MIC_N pins
	Signal to noise	75			dB	Gain stage = +12 dB, Bandwidth 300-3900 Hz
	Signal to distortion (THD)	65			dB	
	Power supply rejection	45	66		dB	

If not specified otherwise, all parameters are measured with a bandwidth of 20 Hz,..., 20 kHz.

Table 27: Differential audio transmit path (MIC_P, MIC_N) input characteristics

Pin Name	Parameter	Min.	Typ.	Max.	Unit	Remarks
SPK_P/SPK_N	Maximum differential output voltage	3.3	3.7	4.1	Vpp	Full scale differential open circuit voltage
	Common mode output voltage		1.25		V	
	Output load resistance	14			Ω	
	Single-ended output load capacitance			250	pF	
	Signal to noise	76	80		dB	Load = 16 Ω, Gain stage = +0 dB, Input signal = 0 dBFS, Code 0, A-weighted
	Signal to distortion (THD)	60	70		dB	Load = 16 Ω, Input signal = 0 dBFS

If not specified otherwise, all parameters are measured with a bandwidth of 20 Hz,..., 20 kHz.

Table 28: Differential audio receive path (SPK_P, SPK_N) output characteristics

5 Mechanical specifications

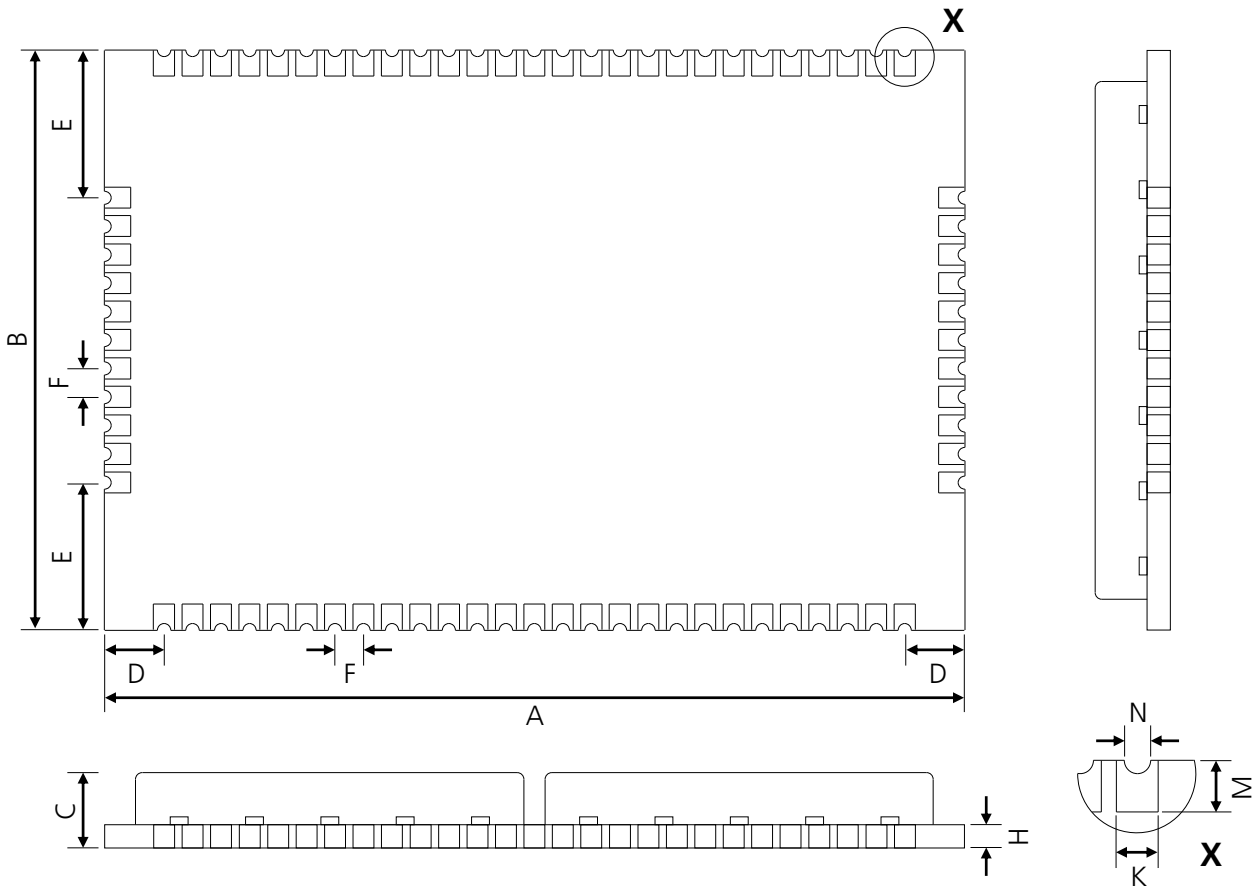

Figure 17: Dimensions (LISA-U1 series bottom and sides views)

Parameter	Description	Typical		Tolerance	
A	Module Height [mm]	33.2	(1307.1 mil)	+0.20/-0.20	(+7.9/-7.9 mil)
B	Module Width [mm]	22.4	(881.9 mil)	+0.20/-0.20	(+7.9/-7.9 mil)
C	Module Total Thickness [mm]	2.6	(102.4 mil)	+0.27/-0.17	(+10.6/-6.7 mil)
D	Horizontal Edge to Pin Pitch [mm]	2.3	(90.6 mil)	+0.20/-0.20	(+7.9/-7.9 mil)
E	Vertical Edge to Pin Pitch [mm]	5.7	(224.4 mil)	+0.20/-0.20	(+7.9/-7.9 mil)
F	Pin to Pin Pitch [mm]	1.1	(43.3 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
K	Pad width [mm]	0.8	(31.5 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
M	Pad height [mm]	1.0	(39.4 mil)	+0.10/-0.10	(+3.9/-3.9 mil)
N	Pad half-moon diameter [mm]	0.5	(19.7 mil)	+0.10/-0.10	(+3.9/-3.9 mil)
Weight	Module Weight [g]	< 7			

Note: the values in mil have been calculated from the relative values in mm.

Table 29: Dimensions

For information regarding Footprint and Paste Mask see the LISA-U series System Integration Manual [6].

6 Reliability tests and approvals

6.1 Reliability tests

A qualification according to ISO 16750 "Road vehicles - Environmental conditions and testing for electrical and electronic equipment" is performed on LISA-U1 series modules.

6.2 Approvals

Products marked with this lead-free symbol on the product label comply with the "Directive 2002/95/EC of the European Parliament and the Council on the Restriction of Use of certain Hazardous Substances in Electrical and Electronic Equipment" RoHS).

LISA-U1 series modules are RoHS compliant.

No natural rubbers, hygroscopic materials, or materials containing asbestos are employed.

LISA-U1 series modules main approvals are listed in Table 30.

Certification scheme	LISA-U100	LISA-U110	LISA-U120	LISA-U130
GCF (Global Certification Forum)	•	•	•	•
PTCRB (PCS Type Certification Review Board)	•		•	
R&TTE (Radio and Telecommunications Terminal Equipment EU Directive)	•	•	•	•
CE (Conformité Européenne)	CE NB ID: 0890	CE NB ID: 0890	CE NB ID: 0890	CE NB ID: 0890
FCC (US Federal Communications Commission)	FCC ID: XPYLISAU120		FCC ID: XPYLISAU120	
IC (Industry Canada)	IC ID: 8595A-LISAU120		IC ID: 8595A-LISAU120	

Table 30: LISA-U1 series main certification approvals

For the complete list of countries and network operators approvals please refer to our website www.u-blox.com.

7 Product handling & soldering

7.1 Packaging

LISA-U1 series modules are delivered as hermetically sealed, reeled tapes to enable efficient production, production lot set-up and tear-down. For more information about packaging, see the u-blox Package Information Guide [13].

Figure 18: Reeled LISA-U1 series modules

7.1.1 Reels

LISA-U1 series modules are deliverable in quantities of 150 pieces on a reel. LISA-U1 series modules are delivered using reel Type B as described in the u-blox Package Information Guide [13].

Parameter	Specification
Reel Type	B
Delivery Quantity	150

Table 31: Reel information for LISA-U1 series modules

☞ Quantities of less than 150 pieces are also available. Contact u-blox for more information.

7.1.2 Tapes

Figure 19 shows the position and orientation of LISA-U1 series modules as they are delivered on tape. The dimensions of the tapes are specified in Figure 20.

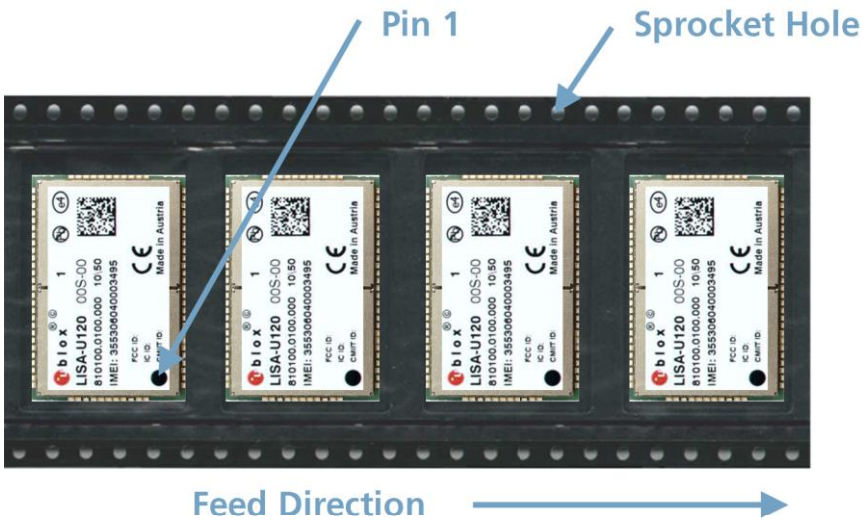

Figure 19: Dimensions for LISA-U1 series on tape

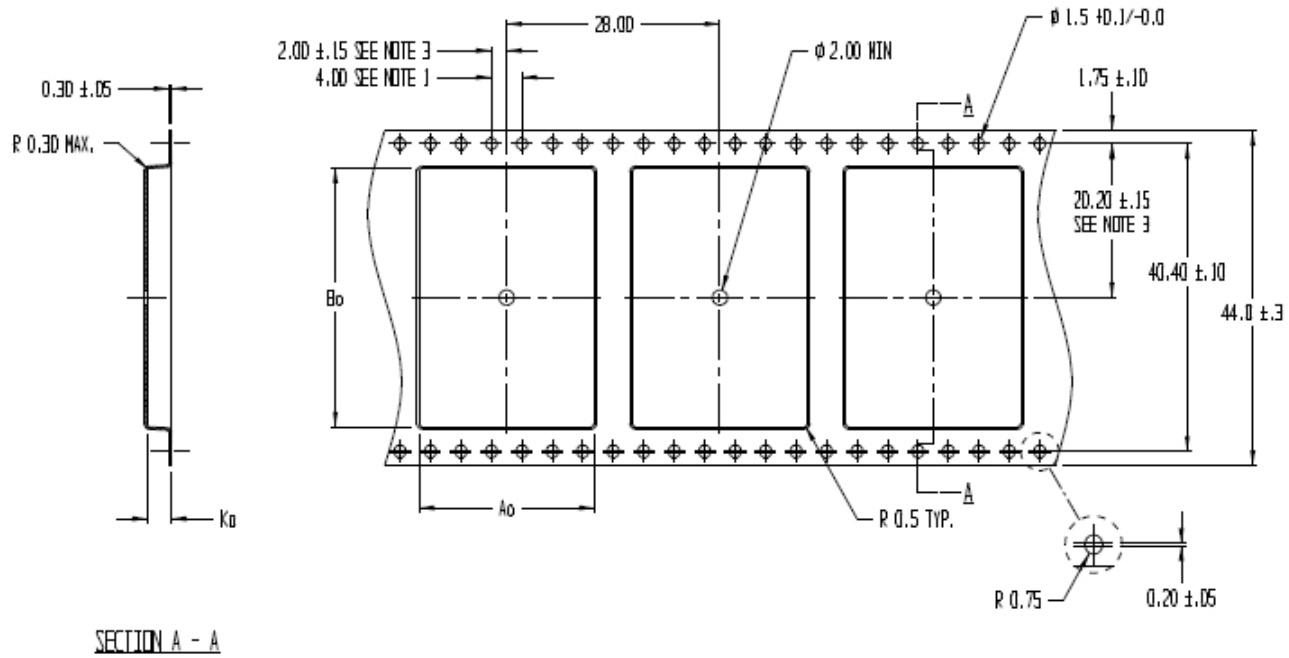

Figure 20: LISA-U1 series tape dimensions (mm)

Parameter	Value
A_0	23.0
B_0	34.0
K_0	3.2

Table 32: LISA-U1 series tape dimensions (mm) and notes

Note 1: 10 sprocket hole pitch cumulative tolerance ± 0.2.

Note 2: the camber is compliant with EIA 481.

Note 3: the pocket position relative to sprocket hole is measured as true position of pocket, not pocket hole.

Note 4: A_0 and B_0 are calculated on a plane at a distance "R" above the bottom of the pocket.

7.2 Moisture Sensitivity Levels

LISA-U1 series modules are Moisture Sensitive Devices (MSD) in accordance to the IPC/JEDEC specification.

The Moisture Sensitivity Level (MSL) relates to the packaging and handling precautions required. LISA-U1 series modules are rated at MSL level 4. For more information regarding moisture sensitivity levels, labeling, storage and drying see the u-blox Package Information Guide [13].

For MSL standard see IPC/JEDEC J-STD-020 (can be downloaded from www.jedec.org).

7.3 Reflow soldering

Reflow profiles are to be selected according to u-blox recommendations (see LISA-U series System Integration Manual [6]).

Failure to observe these recommendations can result in severe damage to the device!

7.4 ESD precautions

LISA-U1 series modules contain highly sensitive electronic circuitry and are Electrostatic Sensitive Devices (ESD). Handling LISA-U1 series modules without proper ESD protection may destroy or damage them permanently.

LISA-U1 series modules are Electrostatic Sensitive Devices (ESD) and require special ESD precautions typically applied to ESD sensitive components.

Maximum ESD ratings of the LISA-U1 series module are reported in Table 7.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates LISA-U1 series module.

ESD precautions should be implemented on the application board where the module is mounted, as described in the LISA-U series System Integration Manual [6].

Failure to observe these precautions can result in severe damage to the device!

8 Default settings

Interface	AT Settings	Comments
UART interface	Enabled	Multiplexing mode can be enabled by AT+CMUX command providing following channels: • Channel 0: control channel • Channel 1 – 5: AT commands /data connection • Channel 6: GPS tunneling
	AT+IPR=115200	Baud rate: 115200 b/s
	AT+ICF=3,1	Frame format: 8 bits, no parity, 1 stop bit
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode
	AT&D1	Upon an ON-to-OFF transition of DTR, the DCE enters online command state and issues an OK result code
	AT&C1	Circuit 109 changes in accordance with the Carrier detect status; ON if the Carrier is detected, OFF otherwise
USB interface	Enabled	6 CDCs are available, configured as described in the following list: • USB1: AT commands / data connection • USB2: AT commands / data connection • USB3: AT commands / data connection • USB4: GPS tunneling dedicated port • USB5: 2G trace dedicated port • USB6: 3G trace dedicated port
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode
	AT&D1	Upon an ON-to-OFF transition of DTR, the DCE enters online command state and issues an OK result code
	AT&C1	Circuit 109 changes in accordance with the Carrier detect status; ON if the Carrier is detected, OFF otherwise
SPI interface	Enabled	Multiplexing mode can be enabled by AT+CMUX command providing following channels: • Channel 0: control channel • Channel 1 – 5: AT commands /data connection • Channel 6: GPS tunneling
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode
	AT&D1	Upon an ON-to-OFF transition of DTR, the DCE enters online command state and issues an OK result code
	AT&C1	Circuit 109 changes in accordance with the Carrier detect status; ON if the Carrier is detected, OFF otherwise
Power Saving	AT+UPSV=0	Disabled
Network registration	AT+COPS=0	Self network registration

Table 33: Default settings

Refer to the u-blox AT Commands Manual [5] and to the LISA-U series System Integration Manual [6] for information about further settings.

9 Labeling and ordering information

9.1 Product labeling

The label on u-blox modules includes important product information. The location of the product type number is shown in Figure 21.

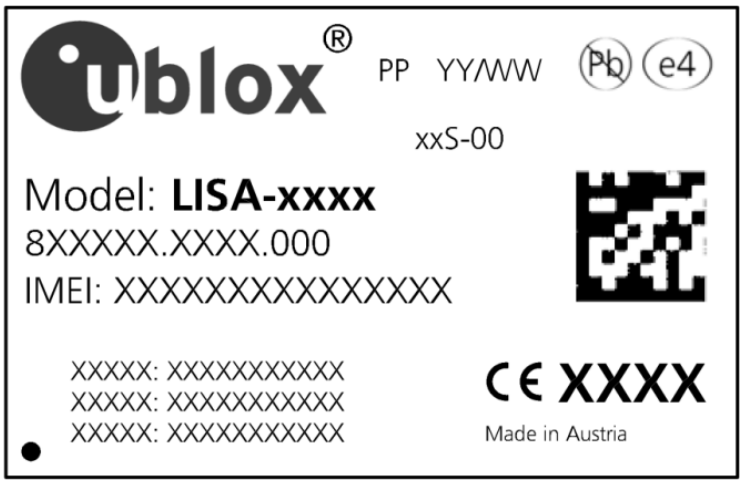

Figure 21: Location of product type number on LISA-U1 series module label

9.2 Explanation of codes

3 different product code formats are used. The **Product Name** is used in documentation such as this data sheet and identifies all u-blox products, independent of packaging and quality grade. The **Ordering Code** includes options and quality, while the **Type Number** includes the hardware and firmware versions. Table 34 details these 3 different formats:

Format	Structure
Product Name	LISA-CDVG
Ordering Code	LISA-CDVG-TTQ
Type Number	LISA-CDVG-TTQ-XX

Table 34: Product Code Formats

The parts of the product code are explained in Table 35.

Code	Meaning	Example
C	Cellular standard (i.e. G: GSM; E: EDGE; W: WEDGE; H: HSDPA; U: HSUPA, L: LTE; C: CDMA 1xRTT; D: EV-DO)	U: HSUPA
D	Generation, e.g. chip or function set; range: [0…9]	1
V	Variant based on the same cellular chip; range: [0...9]	
G	GPS/GNSS generation (if GPS/GNSS functionality available)	6 = u-blox 6, 0: no GPS/GNSS functionality
TT	Version	0
Q	Quality grade/production site • S = standard • A = automotive • B = standard / made in Brazil	S
XX		Default value is 00

Table 35: Part identification code

9.3 Ordering information

Ordering No.	Product
LISA-U100-00S LISA-U100-01S	HSPA 850/1900 MHz, quad-band GPRS/EDGE, data only (no voice), 33.2 x 22.4 x 2.6 mm 150 pcs/reel
LISA-U110-00S LISA-U110-01S	HSPA 900/2100 MHz, quad-band GPRS/EDGE, data only (no voice), 33.2 x 22.4 x 2.6 mm 150 pcs/reel
LISA-U110-60S	HSPA 900/2100 MHz, quad-band GPRS/EDGE, data only (no voice), 33.2 x 22.4 x 2.6 mm, FW version approved and locked for SoftBank Japanese network operator 150 pcs/reel
LISA-U120-00S LISA-U120-01S	HSPA 850/1900 MHz, quad-band GPRS/EDGE, voice and data, 33.2 x 22.4 x 2.6 mm 150 pcs/reel
LISA-U130-00S LISA-U130-01S	HSPA 900/2100 MHz, quad-band GPRS/EDGE, voice and data, 33.2 x 22.4 x 2.6 mm 150 pcs/reel
LISA-U130-60S	HSPA 900/2100 MHz, quad-band GPRS/EDGE, voice and data, 33.2 x 22.4 x 2.6 mm, FW version approved and locked for SoftBank Japanese network operator 150 pcs/reel

Table 36: Product ordering codes

Appendix

A Glossary

Name	Definition
BER	Bit Error Rate
DCE	Data Communication Equipment
DDC	Display Data Channel (I^2C compatible) Interface
DL	Down-link (Reception)
Driver Class	Output Driver Class: see Table 19 for definition
DRX	Discontinuous Reception
DTE	Data Terminal Equipment
EDGE	Enhanced Data rates for GSM Evolution
ERS	External Reset Input Signal
GDI	Generic Digital Interfaces (power domain)
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communication
H	High logic digital level
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I^2C	Inter-Integrated Circuit Interface
I^2S	Inter-IC Sound Interface
L	Low logic digital level
LCC	Leadless Chip Carrier
N/A	Not Applicable
OD	Open Drain
PCN / IN	Product Change Notification / Information Note
PD	Pull-Down
POS	Power-On Input Signal
PU	Pull-Up
PU/PD Class	Pull-Up / Pull-Down Class: see Table 19 for definition
RMC	Reference Measurement Channel
SIM	Subscriber Identity Module
SPI	Serial Peripheral Interface
T	Tristate (Output of the pin set to tri-state, i.e. high impedance state)
T/PD	Tristate with internal active Pull-Down enabled
T/PU	Tristate with internal active Pull-Up enabled
UART	Universal Asynchronous Receiver-Transmitter serial interface
UL	Up-link (Transmission)
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus interface

Table 37: Explanation of abbreviations and terms used

Related documents

[1] 3GPP TS 27.007 V3.13.0 - AT command set for User Equipment (UE) (Release 1999)

[2] 3GPP TS 27.005 V3.2.0 (2002-06) - Use of Data Terminal Equipment - Data Circuit terminating; Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS) (Release 1999)

[3] 3GPP TS 27.010 V3.4.0 - Terminal Equipment to User Equipment (TE-UE) multiplexer protocol (Release 1999)

[4] ITU-T Recommendation V24, 02-2000. List of definitions for interchange circuits between Data Terminal Equipment (DTE) and Data Connection Equipment (DCE)

[5] u-blox AT Commands Manual, Docu No WLS-SW-11000

[6] LISA-U series System Integration Manual, Docu No 3G.G2.HW.10002

[7] GPS Implementation Application Note, Docu No GSM.G1-CS-09007

[8] GSM MUX Implementation Application Note for wireless modules, Docu No WLS-CS-11002

[9] 3GPP TS 26.267 - Technical Specification Group Services and System Aspects; eCall Data Transfer; In-band modem solution; General description (Release 9)

[10] Universal Serial Bus Revision 2.0 specification, http://www.usb.org/developers/docs/

[11] I2C-Bus Specification Version 2.1 Philips Semiconductors (January 2000), http://www.nxp.com/acrobat_download/literature/9398/39340011_21.pdf

[12] u-blox SPI Interface Application Note, Docu No 3G.G2-CS-11000

[13] u-blox Package Information Guide, Docu No GPS-X-11004

☞ For regular updates to u-blox documentation and to receive product change notifications please register on our homepage.

Revision history

Revision	Date	Name	Status / Comments
-	Sep. 24, 2010	mbud / gcap / lpah	Initial release
1	Oct. 11, 2010	lpah	Improvements in the pinout table and dimensions figure
2	Dec. 03, 2010	sses	Some improvements inserted
3	Apr. 22, 2011	lpah	Updated status to Advance Information
4	Jul. 05, 2011	lpah	Updated status to Preliminary
5	Aug. 03, 2011	lpah	Minor improvements
A	Nov. 23, 2011	sses	Changed status to Advance Information From LISA-U1x0-00S data sheet, added description of LISA-U1x0-01S Added VCC extended operating range Improved ESD maximum rating description Updated Pinout Table (minor corrections) Updated I2S AC characteristics (added slave mode characteristics, settable sample rate characteristics and minor corrections) Updated Dimensions Table (minor corrections)
A1	Jan. 31, 2012	sses	Changed status to Preliminary
A2	Sep. 11, 2012	sses	Added LISA-U110-60S and LISA-U130-60S Updated list of available USB drivers Updated available custom functions over GPIOs Updated SPI description, features and AC characteristics

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