HUAWEI MU739 HSPA+ LGA Module

Development Board Guide

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About This Document

History

Version	Date	Section Number	Description
01	2011-12-28		Creation

Contents

1 Overview

1.1 About This Chapter

This chapter provides a brief description of the MU739 module development kit (DVK), including:

- Introduction to the DVK
- Components of the DVK

NOTE

- In the following chapters and sections, "module" refers to the MU739 module; "DVK" refers to the MU739 module development kit.
- DVK is only used to present the applicable functions of MU739 module. For details about the referenced circuit diagram, please see *HUAWEI MU739 HSPA+ LGA Module Hardware Guide*.

1.2 Introduction to the DVK

The DVK provides a complete solution based on the data functions of the module.

For designers who adopt the module in their design, the DVK facilitates their module-based programming and troubleshooting at the project development stage.

Consisting of a dedicated interface board and accessories, the DVK provides the following interfaces:

- 5 V power supply input interface
- One mini USB port
- One standard RS-232 interface: COM1
- Standard Subscriber Identity Module (SIM) card interface
- Two antenna connectors

The MU739 module is soldered onto the interface board in a manner that is similar to the surface mounting of chips. The signals output from the module are transferred to the development board for secondary development.

1.3 Components of the DVK

Table 1-1 lists the components of the DVK.

Check the components and their quantities after you obtain the DVK. If any component is missing or damaged, contact your DVK supplier.

Table 1-1 Components of the DVK

Number	Item	Quantity (pcs)
1	Development board	1
2	USB cable	1
3	2-pin jumper	3

2 Overview of the DVK

2.1 About This Chapter

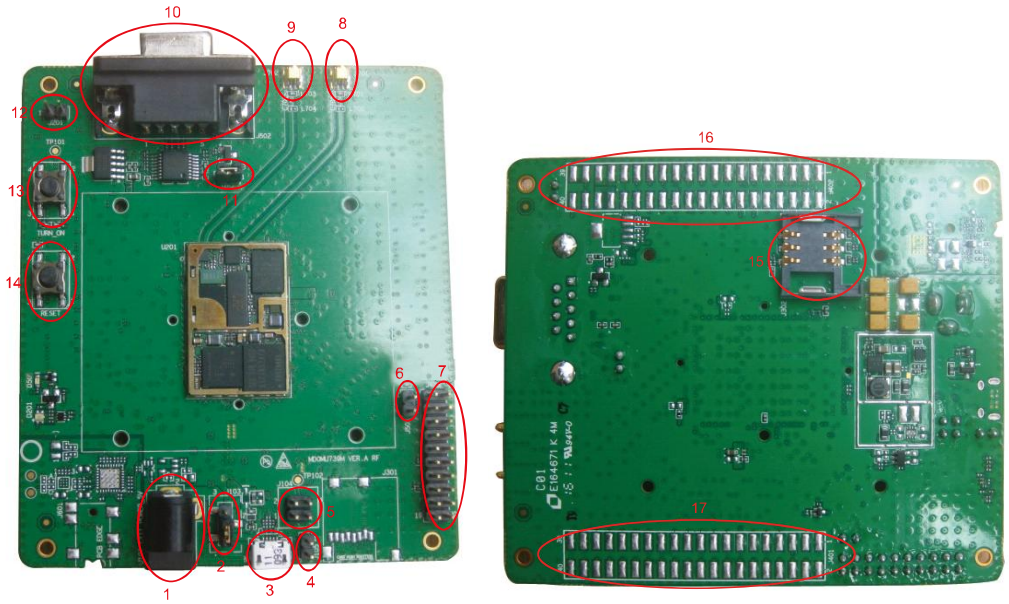
This chapter describes the structure, interface functions, and interface usage of the DVK development board.

- DVK Development Board Structure
- Interface Functions

2.2 DVK Development Board Structure

Figure 2-1 shows the layout of the DVK.

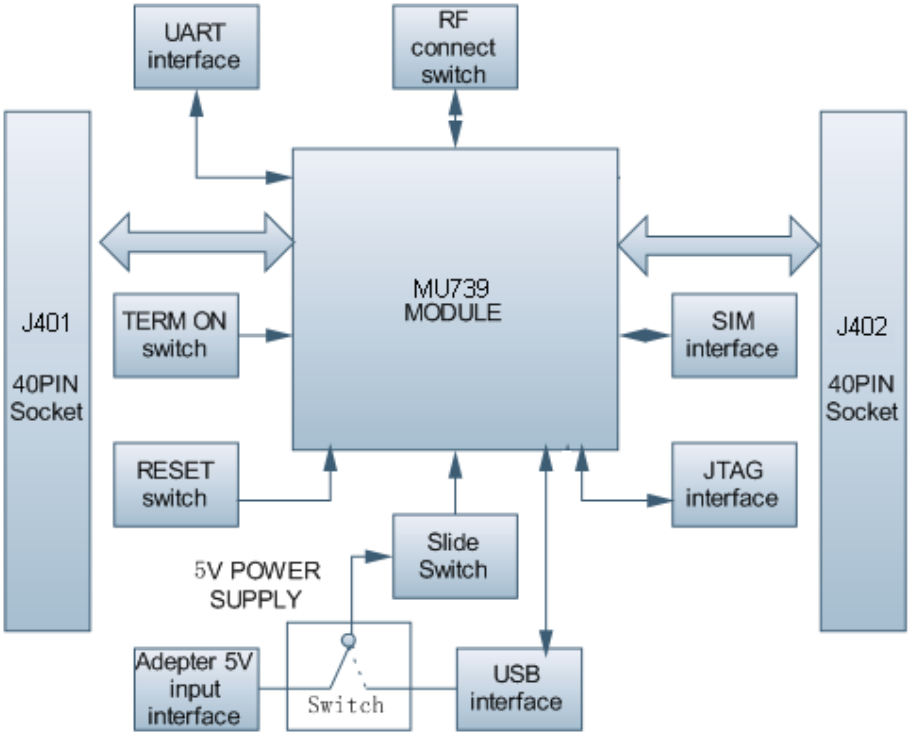
Figure 2-1 Layout of the DVK



1. 5 V power supply input interface
2. Power supply selecting jump
3. Mini USB port
4. GND pins
5. Output pins of DC-DC in base board
6. W-DISABLE control jump
7. Joint Test Action Group (JTAG) interface
8. Primary antenna interface
9. Diversity antenna interface
10. Universal asynchronous receiver/transmitter (UART) serial port
11. Low-level start jump
12. Reserved
13. Reserved high-level start button (not in use)
14. Reset button
15. SIM card interface
16. Socket for testing
17. Socket for testing

Figure 2-2 shows the structure of the DVK development board.

Figure 2-2 DVK structure



2.3 Interface Functions

2.3.1 Power Interface and Power Supply Mode

The power interface (as red circle 1 in Figure 2-1) on the DVK development board supplies power to the development board and the module.

Power can be supplied to the DVK development board in two modes: by an AC-DC 5 V output power adapter or by the USB 5 V power supply. You can use the jump J103 (as red circle 2 in Figure 2-1) to select a power supply mode. When pin 1 and pin 2 are connected, the USB VBUS power supply is used; when pin 2 and pin 3 are connected, the 5 V AC-DC power adapter is used. Only one mode can be selected at a time.

2.3.2 USB Communications Interface

The DVK development board provides a mini USB B-type connector (as red circle 3 in Figure 2-1). The connector implements communications between the module and a personal computer (PC) or other data terminal equipment (DTE).

2.3.3 JATG Interface

The JTAG interface (as red circle 7 in Figure 2-1) is used by the debugging tool to load software into the module. The JTAG interface is not provided for the user.

2.3.4 Serial Communications Interface

The DVK development board provides a DB9 female connector (as red circle 10 in Figure 2-1), it is a standard RS-232 serial communication interface, which supports 4-wire serial communication and can be connected to a PC or other DTE through a RS-232 serial cable. The serial communications interface is used for Huawei internal debug and cannot be used by customer.

2.3.5 Buttons

The DVK development board has two buttons: the reset button S401 (as red circle 14 in Figure 2-1) and the reserved high-level start button S402 (as red circle 13 in Figure 2-1).

The reset button S401 (marked as "Reset" on the development board) is used to reset the module. The reset signal of the module is at low level when the button is pressed.

The module reserves the high-level start button S402 (marked as "Turn_on" on the development board). MU739 supports high-level start, so reserve this button to control the module start. The button cannot be used by customer.

For details about power on or off the module, see the *HUAWEI MU739 HSPA+ LGA Module Hardware Guide.*

2.3.6 SIM Card Interface

The DVK development board provides a standard SIM card interface marked as "J302" (as red circle 15 in Figure 2-1) on the development board.

2.3.7 Antenna Connector

The DVK development board provides two antenna connectors. One is the primary antenna interface J701 (as red circle 8 in Figure 2-1), the other is the diversity antenna interface J702 (as red circle 9 in Figure 2-1). The antenna connectors can be connected to an RF tester (CMU200 or Agilent 8960), or directly connected to external antennas for the testing services of the existing network.

Because there is some line loss on the trace between the module and the antenna connector, when connect to CMU200 or other equipments for testing the RF parameter, this line loss should be considered. Table 2-1 lists the line loss which should be added on different frequency bands.

Table 2-1 Line loss of the baseboard

Frequency Bands (MHz)	Line Loss (dB)
850	0.4
900	0.4
1700	0.5
1900	0.6
2100	0.6

2.3.8 Jump Configuration

The DVK has 6 jumps, as shown in Figure 2-1 . Four jumps need to be configured necessarily during use. Table 2-2 lists the usage and configuration method of the jumps.

Table 2-2 jump configuration

Position Number	Mark on the Development Board	Usage and Configuration	Figure
J103	J307 (as red circle 2 in Figure 2-1)	This jump is used to select the power supply mode. Configuration is needed. For configuration method, see section 2.3.1.	
J104	J104 (as red circle 5 in Figure 2-1)	All the four pins are the output of DC-DC in base board. No configuration is needed. They can be used for testing.	
J105	J105 (as red circle 4 in Figure 2-1)	Both pins are GND pins. No configuration is needed. They can be used for testing.	
J501	J501 (as red circle 6 in Figure 2-1)	This jump is used to select the fly mode (low active). Configuration is needed. When the two pins are connected, the module enters the fly mode.	

Position Number	Mark on the Development Board	Usage and Configuration	Figure
J404	J404 (as red circle 11 in Figure 2-1)	This jump is used to start the module. Configuration is needed. The module can be started only when the two pins are connected.	
J201	J201 (as red circle 12 in Figure 2-1)	Reserved. No configuration is needed.	

2.3.9 Socket for Testing

The DVK provides two 40-pin sockets for testing. One is J401 (as red circle 17 in Figure 2-1), the other is J402 (as red circle 16 in Figure 2-1). Table 2-3 and Table 2-4 show the signal assignment of J401 and J402.

Table 2-3 Signals assignment of J401

Pin NO.	Pin definition
1	GND
2	GND
3	MIPI_HSI_TX_RDY
4	MIPI_HSI_RX_FLG
5	MIPI_HSI_TX_WAKE
6	MIPI_HSI_RX_DATA
7	MIPI_HSI_RX_WAKE
8	MIPI_HSI_RX_RDY
9	MIPI_HSI_TX_DATA
10	MIPI_HSI_TX_FLG
11	/
12	/
13	VCC_IN
14	GPIO3
15	GPIO4
16	GPIO2
17	WAKEUP_OUT
18	WAKEUP_IN

Pin NO.	Pin definition
19	LED_STATUS
20	GPIO5
21	LED_MODE
22	GND
23	EIN2
24	EIN1
25	GND
26	I2S_CLK1
27	I2S_RX
28	I2S_CLK0
29	NC
30	I2S_TX
31	NC
32	GPIO1
33	NC
34	NC
35	I2S_WA1
36	I2S_WA0
37	GND
38	GND
39	GND
40	GND

Table 2-4 Signals assignment of J402

Pin NO.	Pin definition
1	GND
2	GND
3	GND
4	GND
5	SIM_CLK
6	USB_DP

Pin NO.	Pin definition
7	SIM_RST
8	USB_DM
9	GND
10	PWRDWN_N
11	HSIC_USB_DATA
12	USB_VBUS
13	HSIC_USB_STRB
14	SIM_VCC
15	GND
16	RESIN_N
17	SIM_DATA
18	ON2_N
19	W_DISABLE_N
20	JTAG_TDO
21	/
22	VCC_EXT1
23	JTAG_TDI
24	JTAG_TCK
25	RESOUT_N
26	JTAG_TMS
27	ON1
28	JTAG_TRST_N
29	/
30	GND
31	GND
32	GND
33	GND
34	VBAT_PA
35	VBAT_PMU
36	VBAT_PA
37	/

Pin NO.	Pin definition
38	PWRDWN_N
39	/
40	/