HUAWEI LGA Module

PCM Audio Design Guide

Issue 01

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Huawei Technologies Co., Ltd.

Huawei Industrial Base, Bantian, Longgang, Shenzhen 518129, People's Republic of China
Tel: +86-755-28780808 Global Hotline: +86-755-28560808 Website: www.huawei.com
E-mail: mobile@huawei.com

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About This Document

History

Version	Date	Chapter	Descriptions
01	2011-05-04		Creation

Contents

1 Introduction

The purpose of this document is to describe some hardware specification which is useful to develop a product with HUAWEI LGA module supporting PCM (Pulse-Coded Modulation). This document is intended for HUAWEI customers who are integrators and about to implement their applications by using our module.

The HUAWEI LGA module supports the PCM, which can be used for the module to transmit and receive digital audio data. Linear and μ-law codecs are supported. The HUAWEI LGA module uses the PCM interface as part of the audio front end; it easily allows for an external codec to be used instead of the internal codec. As an example, through the PCM you could connect a HUAWEI LGA module to a Bluetooth device.

The HUAWEI LGA module has one PCM port. Please refer to the Hardware Guide of the module that you are in use to know the PIN number of the PCM ports.

2 Interface

2.1 PCM Interface

The PCM interface can be used in primary PCM mode that runs at 2.048 MHz.

We will mainly discuss this PCM mode in later section

Table 2-1 Definitions of pins on the LGA PCM interface

Pin No. (LGA)	Pin Name		I/O	Description
	Normal	MUX		
5	PCM_SYNC	GPIO	I/O	PCM interface sync
6	PCM_DIN	GPIO	I	PCM I/F data in
7	PCM_DOUT	GPIO	O	PCM I/F data out
8	PCM_CLK	GPIO	I/O	PCM interface clock

NOTE

- When the LGA module works on master mode, PCM_CLK and PCM_SYNC pins are in the output status; when the LGA module works on slave mode, PCM_CLK and PCM_SYNC pins are in the input status.
- Each product has two editions: Data only or Telematics. Data only does not support the PCM function

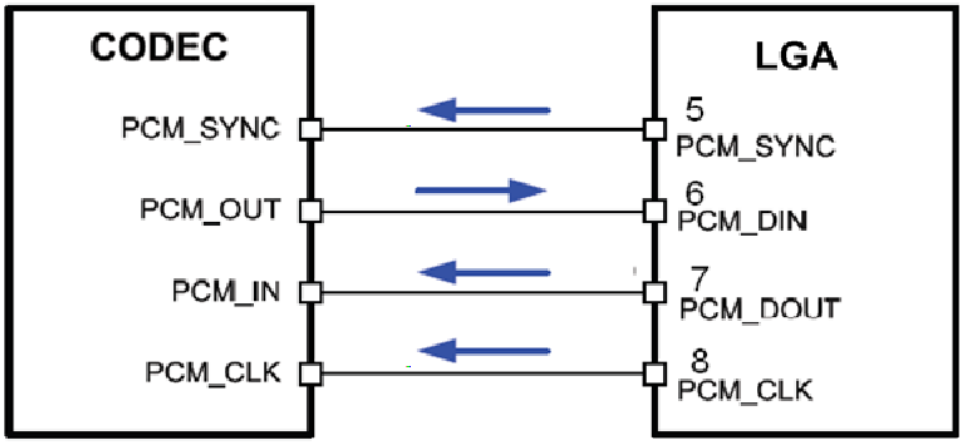
2.2 Configuration Mode

2.2.1 Primary PCM

The Primary PCM interface enables communication with an external codec to support hands-free applications. Linear and u-law codecs are supported by the Primary PCM interface. The auxiliary codec port operates with standard long-sync timing and a 2.048 MHz clock.

2.3 Clock Mode

Figure 2-1 The clock mode



The clock mode is defined:

Master, HUAWEI LGA module is the clock signal source; the PCM_CLK pin and PCM_SYNC pin become output and direction is from HUAWEI LGA module to external codec. Slave mode is only allowed in the Primary PCM Configuration Mode.

3 Timing

3.1 Summarize

- The HUAWEI LGA module allows the use of an external codec .It works under the “Primary i PCM Mode” at 2.048 MHz.
- The Primary PCM Mode sets the clock frequency/sync type to 2.048 MHz/short sync.
- In short sync mode, LGA module supports PRIM-MASTER mode.

3.2 PCM Timing

HUAWEI LGA module PCM interface supports an 8 kHz short sync mode at 2.048 MHz. In short-sync (Primary PCM) mode, the module device sets to be a master without slave support. Timing for mode is detailed below.

3.2.1 Primary PCM Mode(2.048 MHz PCM clock)

Figure 3-1 Primary PCM mode (2.048 MHz PCM clock)

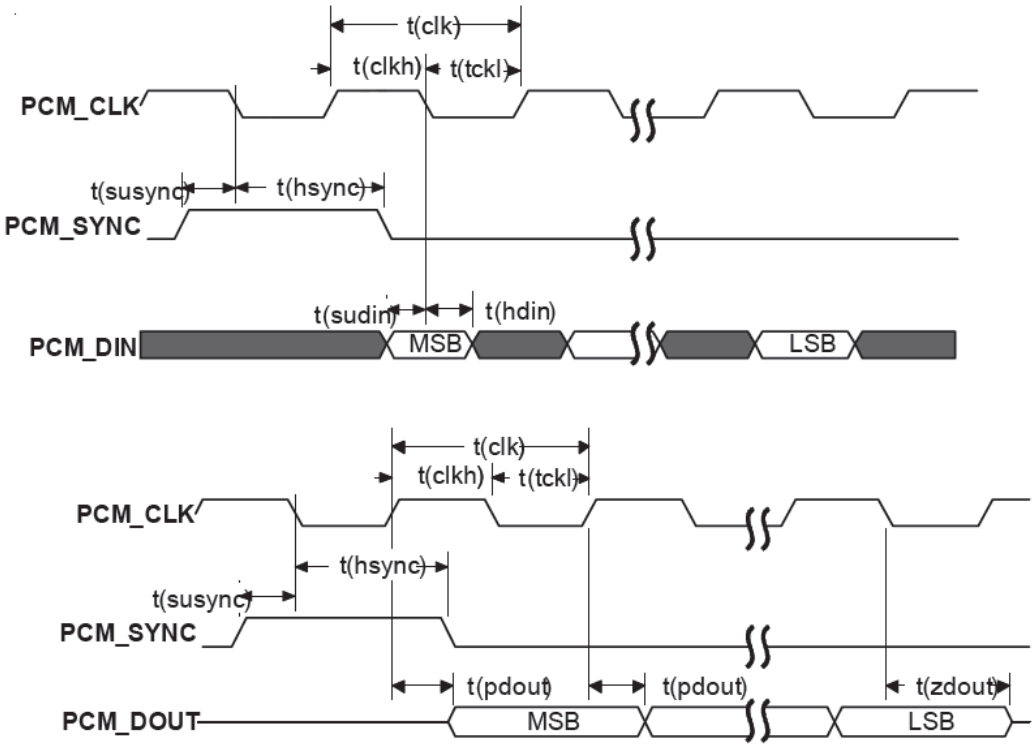


Table 3-1 The parameters of Primary PCM mode timing

Parameter	Description	Min	Typical	Max	Unit
T (sync)	PCM_SYNC cycle time	-	125	-	µs
T (synch)	PCM_SYNC high time	400	500	-	ns
T (syncl)	PCM_SYNC low time	-	124.5	-	µs
T (clk)	PCM_CLK cycle time	-	488	-	ns
T (clkh)	PCM_CLK high time	-	244	-	ns
T (clkl)	PCM_CLK low time	-	244	-	ns
T (susync)	PCM_SYNC setup time high before falling edge of PCM_CLK	60	-	-	ns
T (hsync)	PCM_SYNC hold time after falling edge of PCM_CLK	60	-	-	ns
T (sudin)	PCM_DIN setup time before falling edge of PCM_CLK	50	-	-	ns
T (hdin)	PCM_DIN hold time after falling edge of PCM_CLK	10	-	-	ns

Parameter	Description	Min	Typical	Max	Unit
T(pdout)	Delay from PCM_CLK rising to PCM_DOUT valid	-	-	350	ns
T(zdout)	Delay from PCM_CLK falling to PCM_DOUT HIGH-Z	-	160	-	ns

NOTE

The data in the table above is only for reference.

4 Reference Design

4.1 CODEC Reference

4.1.1 LM49350

General Description

The LM49350 is a high performance audio subsystem that supports both analog and digital audio functions. The LM49350 includes a high quality stereo DAC, a high quality stereo ADC, a stereo headphone amplifier that supports ground referenced output cap-less operation, a dual mode earpiece speaker amplifier and a low EMI Class D loudspeaker amplifier. It is designed for demanding applications in mobile phones and other portable devices.

The LM49350 features dual bi-directional I_2S or PCM audio interfaces for full range audio and an I_2C compatible interface for control. The stereo DAC path features an SNR of 96 dB with 24-bit 48 kHz input. The headphone amplifier delivers 69 mW_{RMS} (typical) to a 32 Ω single-ended stereo load with less than 1% distortion (THD+N) when A_V_{DD} = 3.3 V. The earpiece speaker amplifier delivers 58 mW_{RMS} (typical) to a 32 Ω bridged-tied load with less than 1% distortion (THD+N) when A_V_{DD} = 3.3 V. The loudspeaker amplifier delivers up to 495 mW into an 8 Ω load with less than 1% distortion when LS_V_{DD} = 3.3 V and up to 1.2 W when LS_V_{DD} = 5.0 V.

The LM49350 employs advanced techniques to reduce power consumption, to reduce controller overhead, to speed development time, and to eliminate click and pop. Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. It is therefore ideally suited for mobile phone and other low voltage applications where minimal power consumption, PCB area and cost are primary requirements.

Applications

- Smart Phones
- Mobile Phones and VOIP Phones
- Portable GPS Navigator and Portable Gaming Devices
- Portable DVD/CD/AAC/MP3/MP4 Players
- Digital Cameras/Camcorders

Key Specifications

- P_{HP} at A_V_{DD} = 3.3 V, Stereo 32 Ω, 1% THD 69 mW/ch (typical)
- P_{LS} at LS_V_{DD} = 5 V, 8 Ω, 1% THD 1.2 W (typical)
- P_{LS} at LS_V_{DD} = 4.2 V, 8 Ω, 1% THD 825 mW (typical)
- P_{LS} at LS_V_{DD} = 3.3 V, 8 Ω, 1% THD 495 mW (typical)
- P_{EP} at A_V_{DD} = 3.3 V, 32 Ω BTL, 1% THD 58 mW (typical)
- Supply Voltage Range
  D_V_{DD} = 1.7 V to 2.0 V
  LS_V_{DD} and A_V_{DD} = 2.7 V to 5.5 V
  I/O_V_{DD} = 1.6 V to 4.5 V
- SNR (Stereo DAC at 48 kHz) 96 dB (typical)
- SNR (Stereo ADC at 48 kHz) 94 dB (typical)
- Shutdown Current 2.3 µA (typical)
- PSRR at 217 Hz, A_V_{DD} = 3.3 V, (HP from AUX) 97 dB (typical)

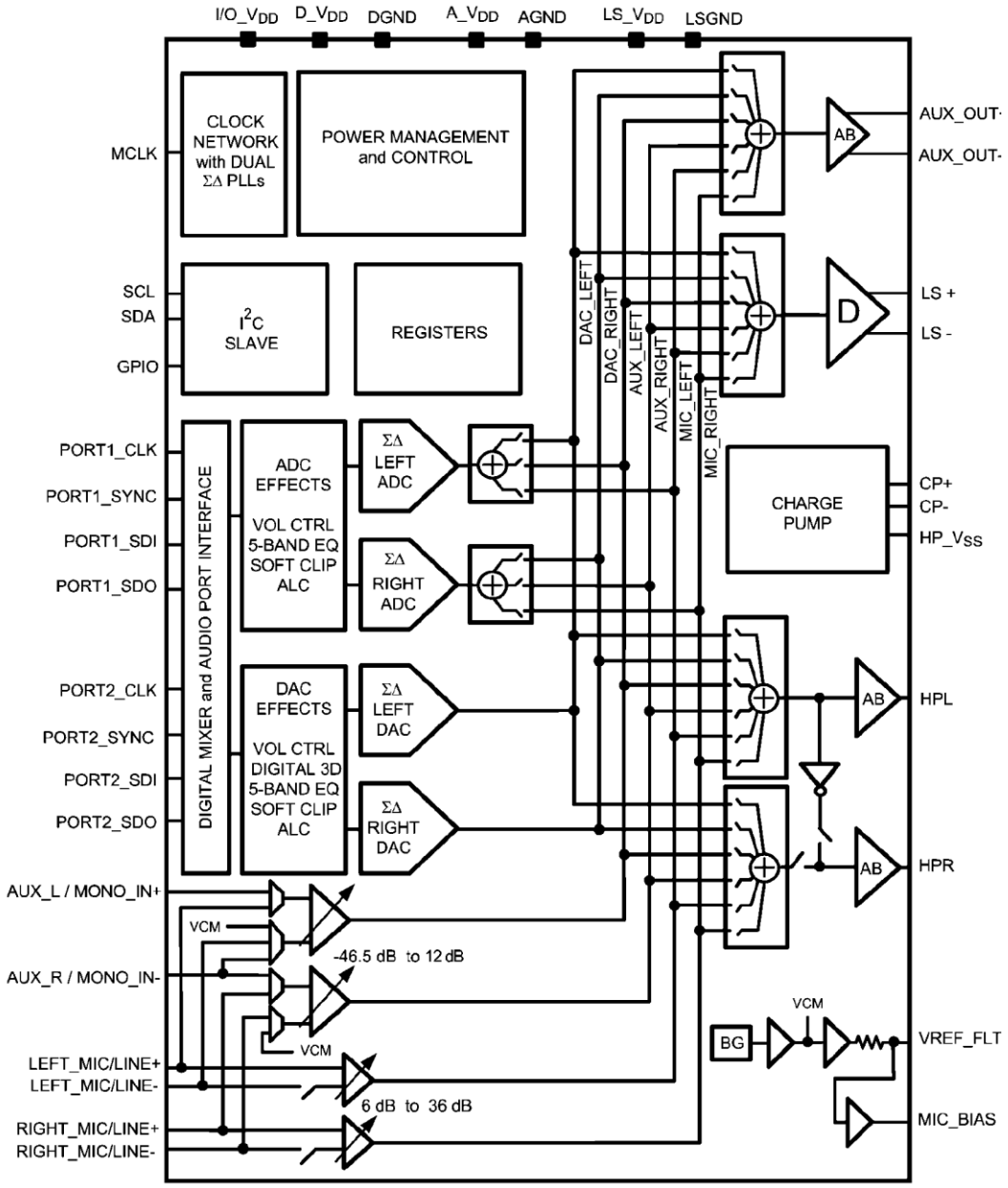
Features

- High performance 96 dB SNR stereo DAC
- High performance 94 dB SNR stereo ADC
- Up to 192 kHz stereo audio playback
- Up to 48 kHz stereo recording
- Dual bidirectional I_2S or PCM compatible audio interfaces
- Read/write I_2C compatible control interface
- Flexible digital mixer with sample rate conversion
- Dual sigma-delta PLLs for operation from any clock at any ample rate
- Digital 3D stereo enhancement
- Dual 5 band parametric equalizers
- Cascadable DSP effects that allow 10 band parametric qualization
- ALC/Compressor/Limiter on both DAC and ADC paths
- Ultra low EMI, Class D loudspeaker amplifier with spread pectrum control
- Ground referenced output cap-less headphone amplifier peration
- Earpiece speaker amplifier with reduced power onsumption mode for mono differential line out pplications
- Stereo auxiliary inputs or mono differential input
- Differential stereo microphone inputs with single-ended option
- Automatic level control for digital audio inputs, stereo microphone inputs, and stereo auxiliary inputs
- Flexible audio routing from input to output
- 16 Step volume control for microphones with 2 dB steps
- 32 Step volume control for auxiliary inputs in 1.5 dB steps
- Micro-power shutdown mode

- Available in the 3.5 mm x 3.5 mm 36 bump micro SMD package

Overview

Figure 4-1 LM49350 block diagram



Typical Application

Figure 4-2 Application in Multimedia phone with a dedicated earpiece and mono loudspeaker

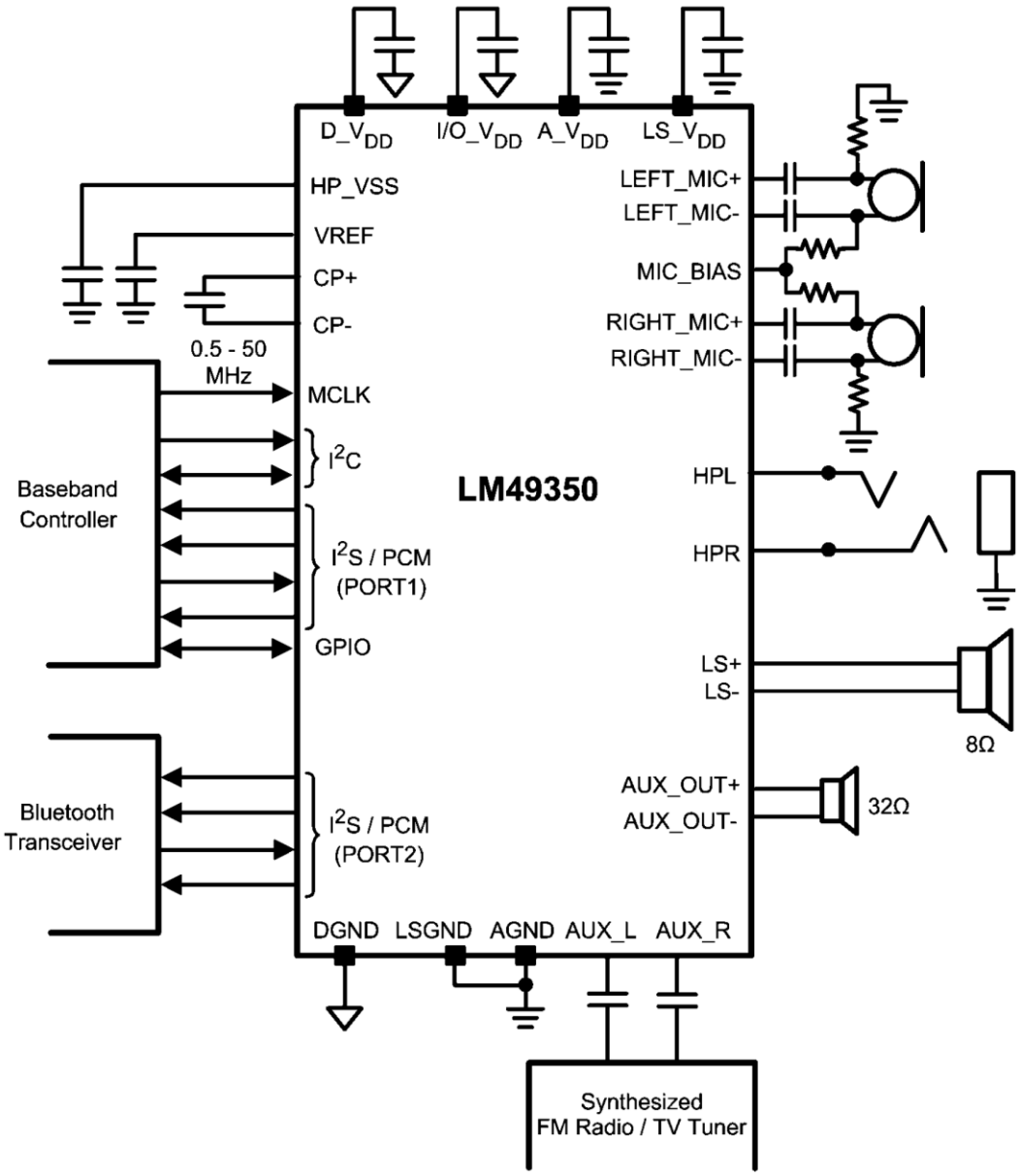


Figure 4-3 Application in multimedia phone using stereo loudspeaker

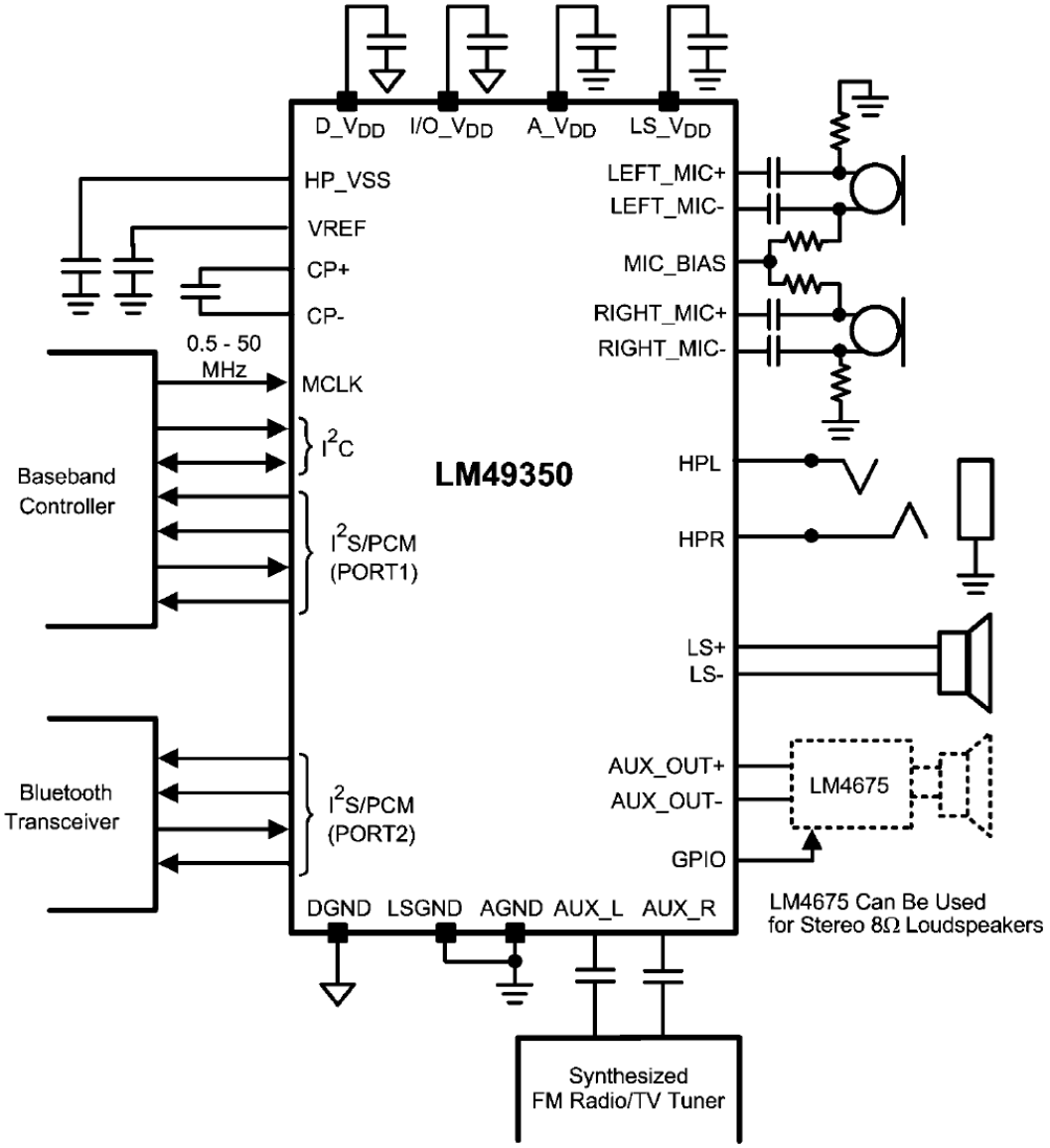


Figure 4-4 Application in a portable media player with a differential stereo line input

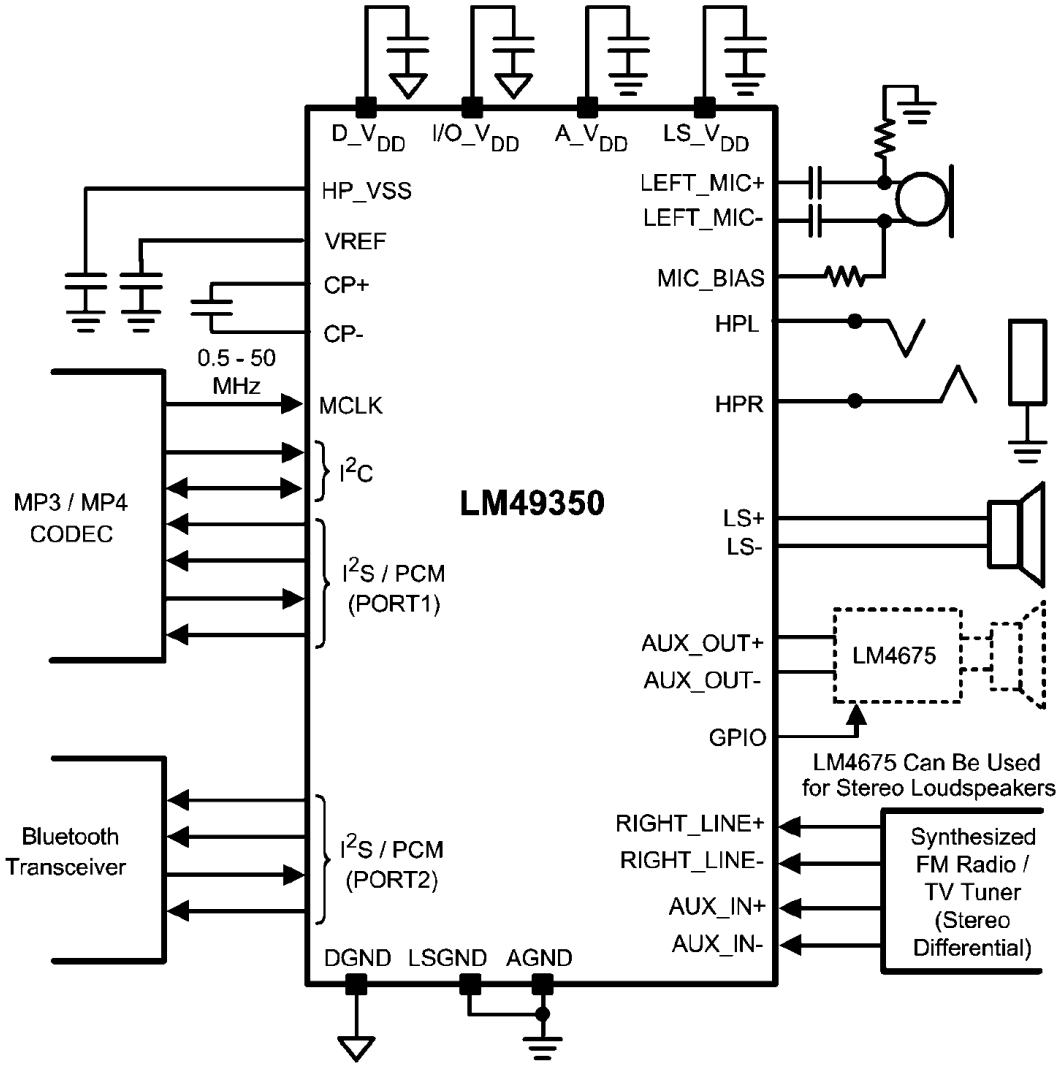
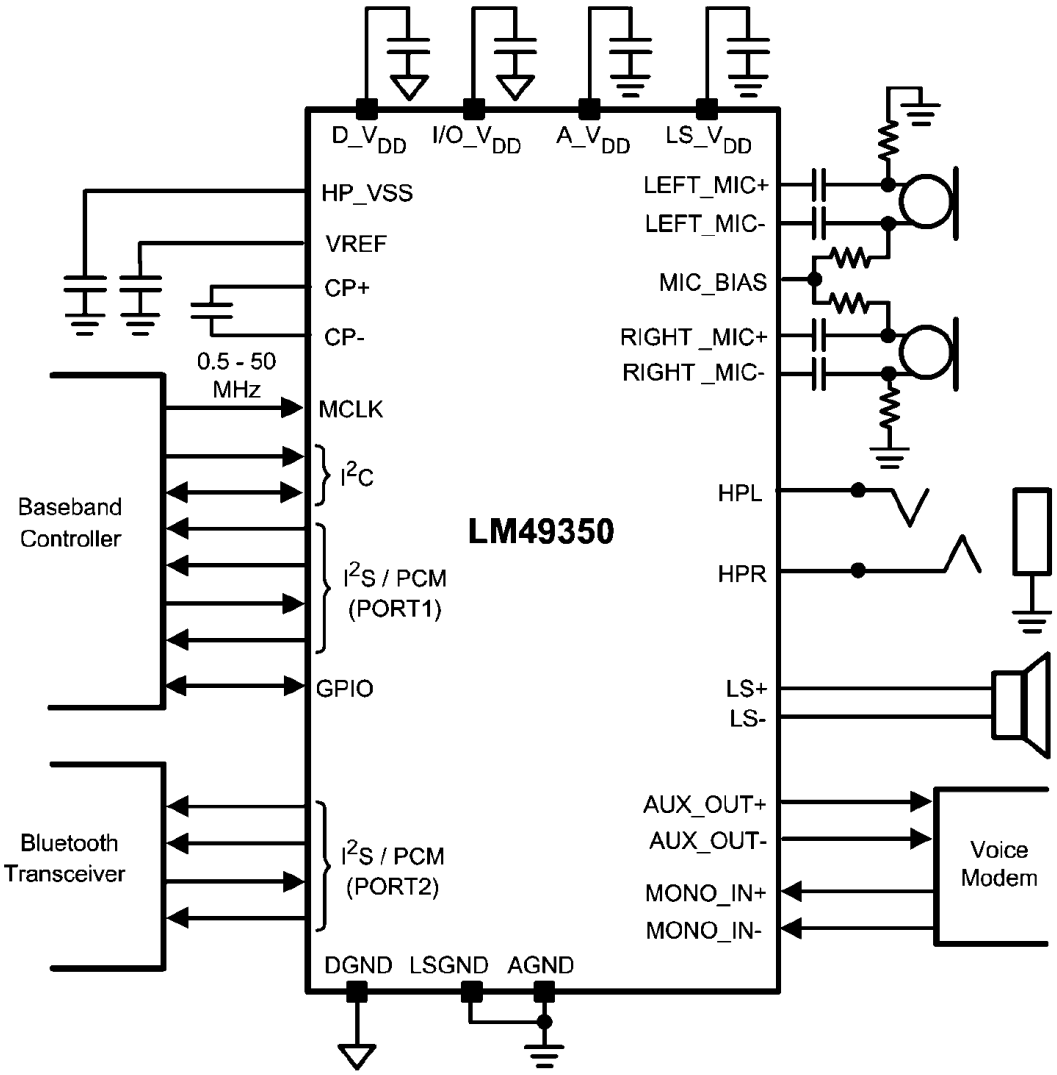


Figure 4-5 Application in a multimedia phone using a dedicated RF module for voice modern functions



4.1.2 TLV320AIC1106

Features

- Designed for Analog and Digital Wireless
- Handsets, Voice-Enabled Terminals, and Telecommunications Applications
- 2.7 V to 3.3 V Operation
- Selectable 13-Bit Linear or 8-Bit ⌠-Law Companded Conversion
- Differential Microphone Input With External Gain Setting
- Differential Earphone Output Capable of Driving a 32-∧ to 8-∧ Load
- Programmable Volume Control in Linear Mode
- Microphone (MIC) and Earphone (EAR) Mute Functions
- Typical Power Dissipation of 0.03 mW in Power-Down Mode

- 2.048 MHz Master Clock Rate
- 300 Hz to 3.4 kHz Passband
- Low Profile 20-Terminal TSSOP Packaging

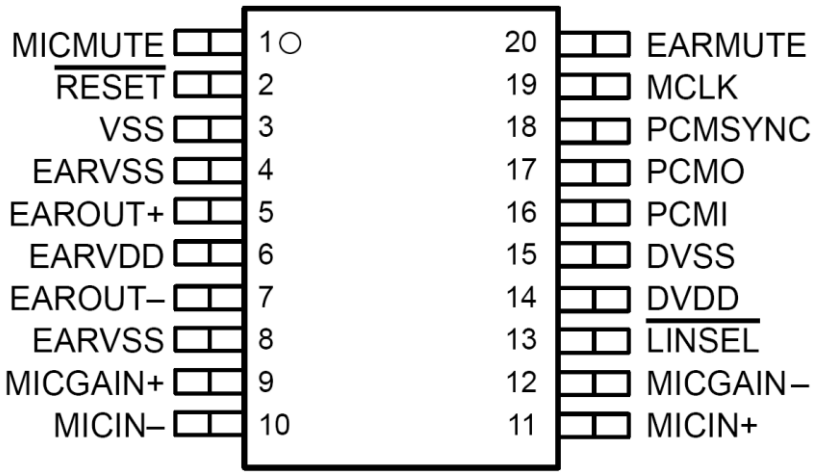
Applications

- Digital Handset
- Digital Headset
- Cordless Phones
- Digital PABX
- Digital Voice Recording

Description

The TLV320AIC1106 PCM codec is designed to perform transmit encoding analog-to-digital (A/D) conversion, receive decoding digital-to-analog (D/A) conversion, and transmit and receive filtering for voice-band communications systems. The TLV320AIC1106 device operates in either the 13-bit linear or 8-bit companded (⌠-law) mode. The PCM codec generates its own internal clocks from a 2.048-MHz master clock input.

Figure 4-6 PW package (top view)



WARNING

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either VCC or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

4.1.3 TLV320AIC20

Features

- Stereo 16-Bit Oversampling Sigma-Delta A/D Converter
- Stereo 16-Bit Oversampling Sigma-Delta D/A Converter
- Support Maximum Master Clock of 100 MHz to Allow DSPs Output Clock to be Used as a Master Clock
- Selectable FIR/IIR Filter With Bypassing Option
- Programmable Sampling Rate up to:
  - Max 26 Ksps With On-Chip IIR/FIR Filter
  - Max 104 Ksps With IIR/FIR Bypassed
- On-Chip FIR Produced 84 dB SNR for ADC and 92 dB SNR for DAC over 13 KHz BW
- Smart Time Division Multiplexed (SMARTDM®) Serial Port
  - Glueless 4-Wire Interface to DSP
  - Automatic Cascade Detection (ACD) Self-Generates Master/Slave Device Addresses
  - Programming Mode to Allow On-The-Fly Reconfiguration
  - Continuous Data Transfer Mode to Minimize Bit Clock Speed
  - Support Different Sampling Rate for Each Device
  - Turbo Mode to Maximize Bit Clock For Faster Data Transfer and Allow Multiple Serial Devices to Share the Same Bus
  - Allows up to Eight Devices to be Connected to a Single Serial Port
- Host port
  - 2-Wire Interface
  - Selectable I^2C or S^2C
- Differential and Single-Ended Analog Input/Output
- Built-In Analog Functions:
  - Analog and Digital Sidetone
  - Antialiasing Filter (AAF)

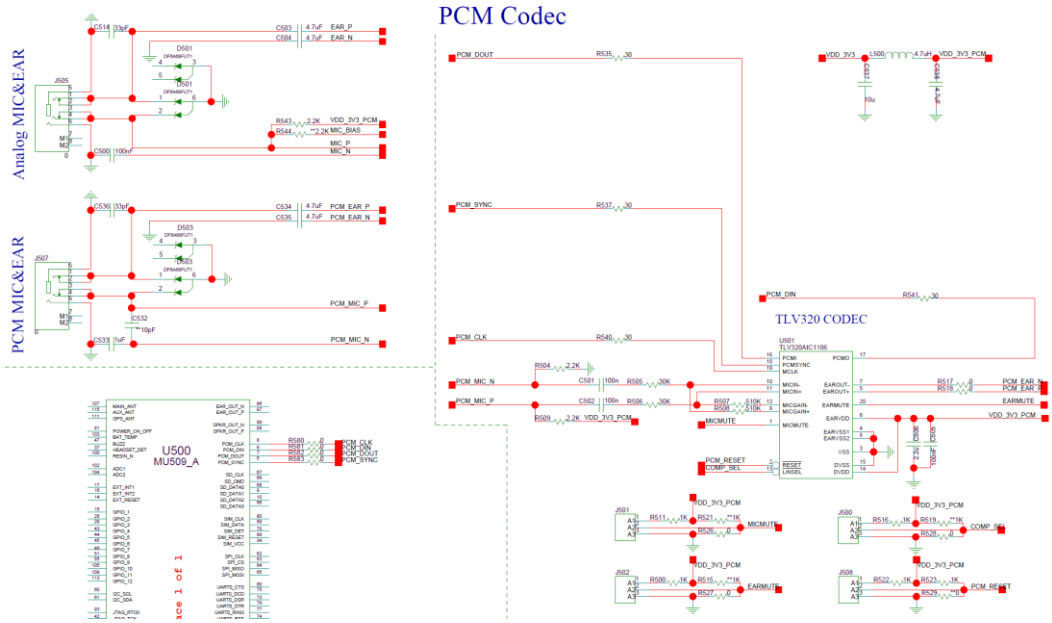
  - Programmable Input and Output Gain Control (PGA)
  - Microphone/Handset/Headset Amplifiers
  - AIC20/21/20K Have a Built-In 8 Ω Speaker Driver
  - Power Management With Hardware/Software Power-Down Modes 30 μW
- Separate Software Control for ADC and DAC Power Down
- Fully Compatible With Common TMS320® DSP Family and Microcontroller Power Supplies
  - 1.65 V - 1.95 V Digital Core Power
  - 1.1 V - 3.6 V Digital I/O
  - 2.7 V - 3.6 V Analog
- Internal Reference Voltage (V_{ref})
- 2s Complement Data Format
- Test Mode Which Includes Digital Loopback and Analog Loopback

Applications

- Wireless Accessories
- Hands-Free Car Kits
- VOIP
- Cable Modem
- Speech Processing

4.2 Reference Design

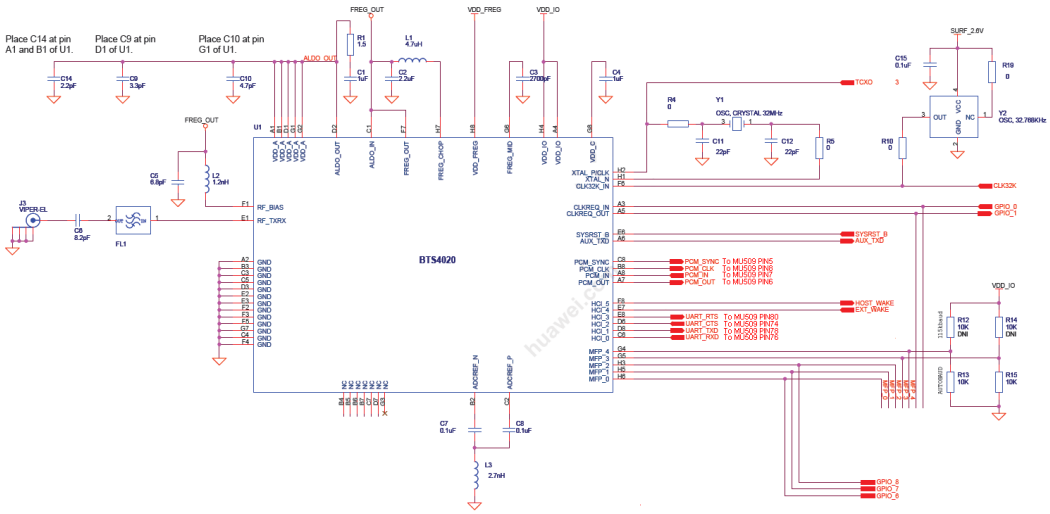
4.2.1 CODEC Reference Application



NOTE

- Set each matching resistance R580, R582, R 583, R 541, R 581, R 535, R 537 and R 540, where PCM_DOUT, PCM_DIN, PCM_CLK and PCM_SYNC placed close to LGA and Codec.
- When LGA works in master mode, R 580, R 582, R 583 and R 541 should be 0 Ω ~ 68 Ω, R 581, R 535, R 537 and R 540 should be 0 Ω。
- When LGA works in slave mode, R580, R582, R583 and R541 should be 0 Ω， R581, R535,R537 and R540 should be 0 Ω ~ 68 Ω.

4.2.2 BLUETOOTH Reference Application



5 Audio Application of PCM

5.1 PCM Initialization Setup

5.1.1 Description

This section describes the initialization setup before PCM audio service.

AT^CPCM command can be used to set the parameter values of mode, format, clock, frame and offset between module and codec.

- mode

  This parameter indicates master or slave mode between module and codec. There are three modes: MASTER_PRIM, MASTER_AUX and SLAVE modes. Currently only MASTER_PRIM mode is supported.

- format

  This parameter indicates formats of sampling and quantification, supporting three modes: linear, u-law and a-law modes. Currently linear and u-law are supported.

- clock

  This parameter indicates the clock signals between module and codec, supporting two values: 2.048MHz and 128 KHz. Currently only 2.048 MHz is supported.

- frame

  This parameter indicates the synchronous signals between module and codec, supporting two modes: short frame and long frame. Currently only short frame is supported.

- offset

  This parameter indicates the deviation between synchronous signals and clock signals, supporting three modes: offset cleared, short sync offset set and long sync offset set modes. Currently offset cleared and short sync offset set modes are supported.

5.1.2 AT Command

Command	Description
AT^CPCM	Command for PCM initialization setup

5.1.3 Indication

All the parameter set by **AT^CPCM** will be stored in the NV. Powering off the module will not change the value. Upgrading the module will restore the parameters to default values. The command of setting PCM initialization setup executes only when telephone is initialized.

The parameter settings of format rely on the used codec chip. If the codec is in the 16-bit linear mode, it is recommended to set format as the default mode that is linear mode. If not, set format as u-law mode.

5.1.4 Examples

****

Application scene: PCM initialization setup

****

****

Operate: setting linear format and offset cleared

****

Send: AT^CPCM=0,0,0,0,0

Receive: OK

****

Operate: setting u-law format and short sync offset set

****

Send: AT^CPCM=0,1,0,0,1

Receive: OK

5.2 Switching PCM Sound Path

5.2.1 Description

This section describes switching PCM sound path.

AT^SWSPATH command can be used to switch sound path to PCM path. The default path is handset path. When **AT^SWSPATH** is set to 2, the sound path will be switched to PCM path.

5.2.2 AT Command

Command	Description
AT^SWSPATH	Command for switching sound path

5.2.3 Indication

All the parameter set by **AT^SWSPATH** will be stored in the NV. Powering off the module will not change the value. Upgrading the module will restore the parameters to default values. The command of setting switch sound path executes only when telephone is initialized

5.2.4 Example

****

Application scene: switching PCM sound path

****

****

Operate: Switch sound path to PCM path after a call connection

****

Receive: RING

Send: ATA

Receive: ^CONN:1,0

OK

Send: AT^SWSPATH=2

Receive: OK