Si3220/Si3225 User Guide

Introduction

The Si3220/Si3225 is a highly-programmable linecard SLIC/codec solution comprised of the Si3220 or Si3225 dual-channel SLIC/codec IC and the Si3200 single-channel linefeed interface chip. Its operation has been optimized to reduce the amount of controller interaction during normal call processing. This document describes the connections, signals, and control required to operate the Si3220/Si3225. The instructions in this document must be followed exactly to achieve a fully-operational solution. Note every aspect of the described design process. Use this document with the Si3220/Si3225 data sheet, Si3220/Si3225 Evaluation Board data sheet, and demonstration source code as references for any Si3220/Si3225 design.

Si3220/Si3225 Layout Considerations

With appropriate layout design, the Si3220/Si3225 circuit will exhibit high-quality low-noise performance. Pins 1, 3, 4, 8, 9, 13, 14, 16–20, and 61–64 are sensitive current input pins that are susceptible to induced noise. Traces between these pins and their respective components (R1–5, R7, R8, R11–15, R17, R18) should be kept to a length of less than 0.25 inch. The connections between pins 6, 7, 10, 11 and their respective components (C5, C6, C15, C16) are of secondary concern. C5, C6, C15, and C16 should be placed immediately beyond the aforementioned resistors with the QGND traces wrapping to pin 8 from the outside. Under no circumstance should any digital traces be routed near these Si3220/Si3225 sensitive traces. The compensation capacitors, C3, C4, C13, and C14, should be placed near the respective TIP and RING outputs of the Si3200. A 0.1 μF ceramic decoupling capacitor should be placed within 0.2 inch of every VDD and VBAT power supply input pin. These capacitors are C20–25 and C30–33. Refer to the evaluation board data sheet for an illustration and example of this layout. (See Figure 1 for component placement.)

The Si3220/Si3225 and Si3200 packages utilize an exposed pad to dissipate thermal energy. To achieve the thermal rating of the Si3200 package, as stated in the data sheet, the exposed pads must be soldered to multiple ground planes. A top side, bottom side, and one inner ground plane should be used with multiple vias connecting them together. Twenty five vias should be used in a 5x5 grid under the Si3220/Si3225. A line of eight vias should be placed in a row under the Si3200. The size of the vias used for the Si3200/Si3225 and Si3200 thermal pads should be at least 10 mils. (See Figures 1, 2, and 3.)

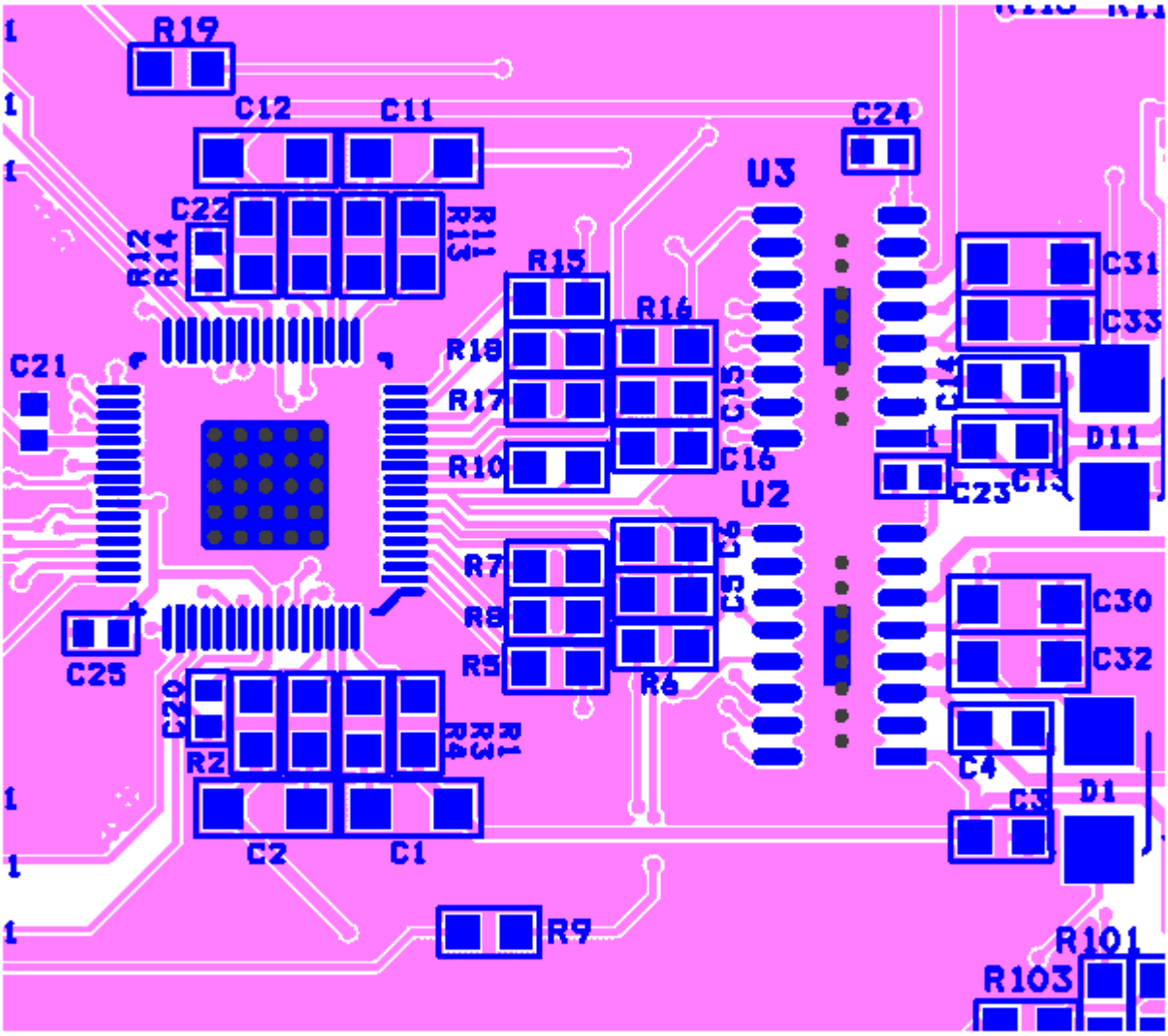

Figure 1. Top Layer (Component Side)

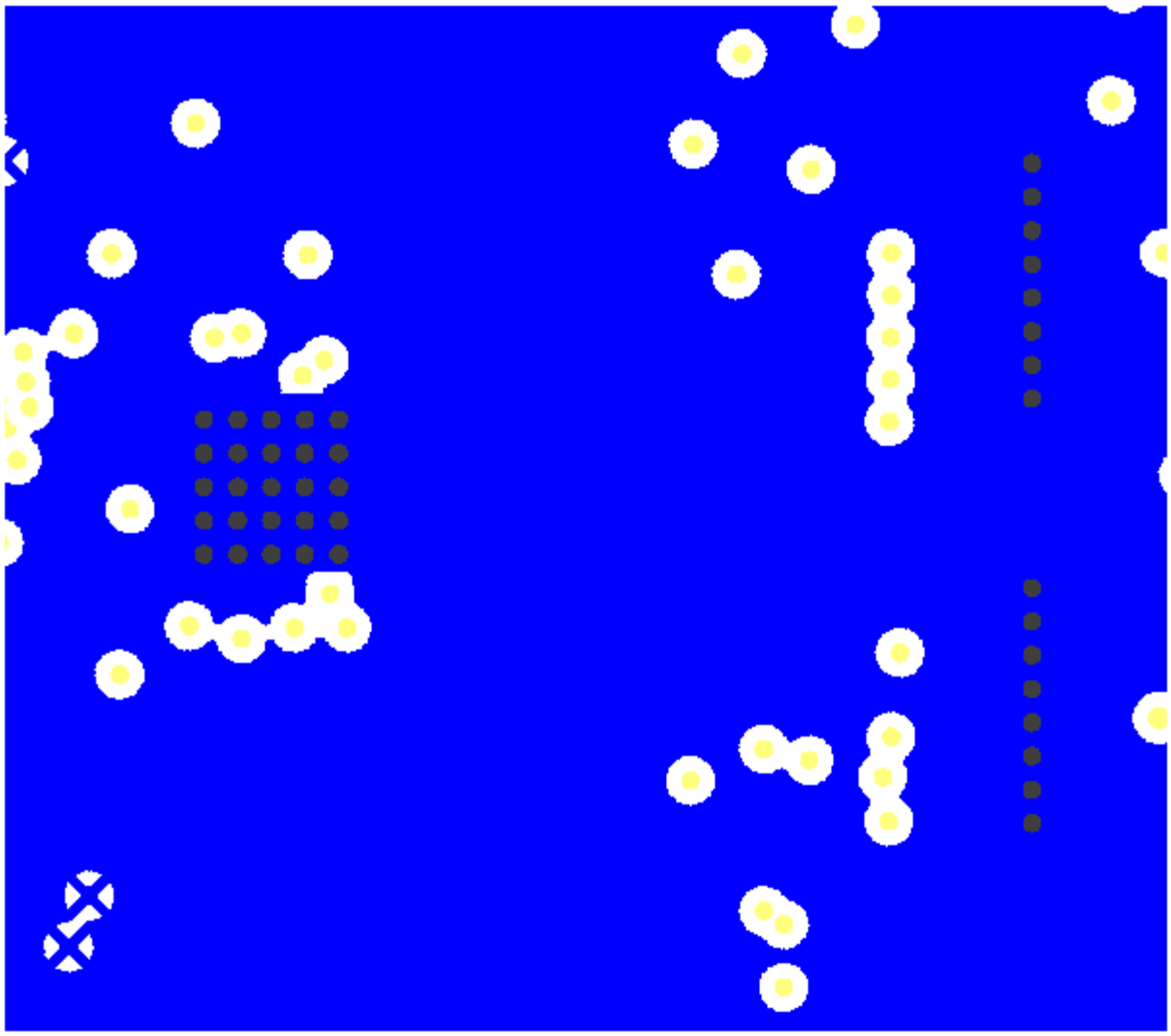

Figure 2. Ground Layer (Inner Layer)

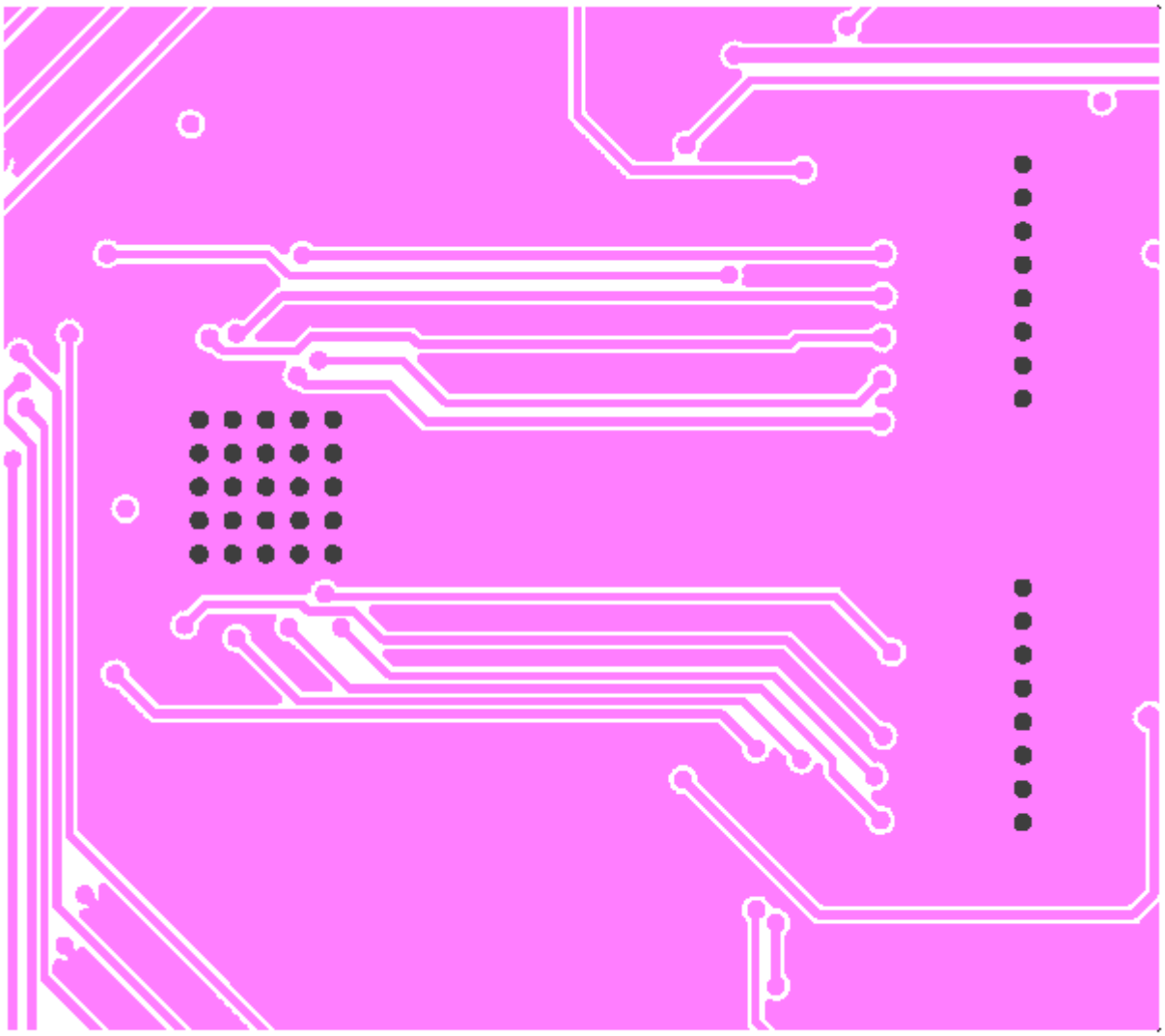

Figure 3. Bottom Layer (Solder Side)

Si3220/Si3225 Power Supply Requirements

The Si3220/Si3225 is a low-power CMOS device that can be powered by a 3.3 V or 5 V supply. All VDD pins of the Si3220/Si3225 must be connected to a common source with low impedance between each pin for optimal low-noise operation. The Si3220/Si3225 ground pins should be connected to a common ground plane. A ceramic bypass capacitor of 0.1 µF at 6 V minimum should be used between every VDD pin and ground. For power supply noise requirements, refer to the Si3220/Si3225 data sheet specifications for power supply rejection ratio (PSRR).

The Si3220/Si3225 solution requires telephony operational voltages. A negative “battery” voltage typically powers the telephone line. The Si3220/Si3225 regulates the TIP and RING voltage to achieve appropriate, programmed dc parameters for a given telephone line condition (ILIM, VOC). The Si3220/Si3225 can perform this from multiple battery sources. On the Si3220 internal ringing application, a high battery voltage (VBATH) is selected large enough to provide sufficient ringing signal. On the Si3225 external ringing application, VBATH is selected for normal on-hook operation where TIP and RING voltage are expected to be within a range of 42 V to 48 V. The VBAT pin of the Si3200 is the negative power supply input for the TIP and RING amplifiers. The VBAT pin is always monitored to ensure proper on-hook voltage (VOC). The on-hook voltage will be reduced from the

programmed value to retain sufficient overhead voltage in the case that the on-hook battery (VBATH) has decreased in value. VBATH is also used for off-hook lines that require more potential than the short loop off-hook battery (VBATL) can provide. VBATL is used to reduce power dissipation when off-hook into a short loop length. VBATL should be selected to allow operation into the longest short loop while not causing excessive power dissipation in the case of zero loop. VBATL is automatically used when the loop dc conditions are such that VBATL can provide enough operating overhead voltage. This automatic function is described in the data sheet (Registers BATxTH, BSWLPF, BATLPF).

For applications that require only one battery, the battery source should be connected to both the VBAT and VBATH pins on the Si3200.

All VBAT supplies should be low-impedance sources with bulk capacitive elements. Ceramic bypass capacitors of 0.1 μF at an appropriate voltage should be applied to the VBATH and VBAT pins per channel. There is no restriction of power-up sequence for any VBAT rail. A dv/dt limit must be observed when applying the VBATH rail. Refer to “Absolute Maximum Ratings” in the data sheet for this dv/dt limit, which can be achieved with an RC network. This dv/dt limitation is usually only an issue in “hot insertion” applications.

Si3220/Si3225 Clock Requirements

The Si3220/Si3225 programmable function is powered by an internal DSP. This DSP is clocked by a PLL that is locked to external clock sources. These clock sources are the PCM bus clock (PCLK) and frame sync (FSYNC). PCLK is the master clock for the PLL and is locked to by setting an internal counter based on PCLK counts relative to FSYNC. This lock operation begins immediately after the reset pin ($\overline{\text{RESET}}$) is brought high. Therefore, the $\overline{\text{RESET}}$ pin should be held low during power up and only released when the PCLK and FSYNC source are known to be stable. The PLL will take approximately 5 ms to achieve lock after reset is released with stable PCLK and FSYNC. Refer to the data sheet for PCM bus timing requirements.

PCLK and FSYNC status is detected and reported by the Si3220/Si3225 after $\overline{\text{RESET}}$ is released. The PLL status should be verified by reading the MSTRSTAT register before initialization of the Si3220/Si3225. Before PLL lock or during a clock-failure condition, only a limited set of registers can be accessed (see the Si3220/Si3225 data sheet).

Connecting Digital Buses

The Si3220/Si3225 utilizes a serial peripheral interface (SPI) bus hardware connection. Communicating to multiple instantiations of the Si3220/Si3225 is achieved by connecting a controller’s synchronous serial interface bus to the first Si3220/Si3225. Remaining devices should be connected to this bus in tandem with the exception of the SDITHRU pin of the first Si3220/Si3225 connecting to the SDI of the next Si3220/Si3225 and so on for up to 16 channels (one chip select for eight devices). A software channel select scheme is then used to communicate to any single channel or combination of channels. The first Si3220/Si3225 in the chain establishes itself as channel 0 and 1 for its two channels of SLIC function. The channel addressing is achieved with a control byte preceding the address/data bytes of a given command. Refer to the data sheet and “AN58: Si3220/Si3225 Programmer’s Guide” for information on communicating to the SPI port.

The PCM bus should also be connected in tandem with all devices. The DTX signal for all devices should be pulled down to ground with a single 470 kΩ resistor.

Remember to route digital signals away from sensitive analog traces mentioned earlier.

Si3220/Si3225 Registers and RAM

The Si3220/Si3225 8-bit register space automatically loads default values following a reset. These registers can be modified for desired functional effect. Refer to the listing in AN58 for the default values and suggested alternate values. Refer to the data sheet for calculation of alternate values.

The 16-bit RAM locations of the Si3220/Si3225 will initialize to 0x0000 following a reset. The RAM must be initialized with functional values to prepare the Si3220/Si3225 for operation. Refer to the RAM listing in AN58 for example RAM location values. Refer to the data sheet or ProSLIC LINC software for calculation of alternate values. Refer to AN58 for communicating to RAM locations.

Si3220/Si3225 Operation

The power supply rails applied to the Si3220/Si3225 can be brought up in any sequence. VDD power should be applied with the Si3220/Si3225 reset pin ($\overline{\text{RESET}}$) held low. The state of any Si3220/Si3225 pin is indeterminate upon power up with no reset. The PCM clock (PCLK) and PCM frame sync (FSYNC) signals must be present and stable before the $\overline{\text{RESET}}$ pin is

released to the high state. PLL lock will occur after release of RESET and should be verified in the MSTRSTAT register before continuing.

Initialization and Calibration

Certain commands must be issued to the Dual ProSLIC to prepare it for operation. A complete initialization and calibration sequence is described in “AN58: Si3220/Si3225 Programmer’s Guide”. The device ID should be read as reference for proper revision-specific operation. Appropriate initial values are then written to all 16-bit RAM locations. Alternate functional values can be written to 8-bit registers if desired. Interrupts are to be cleared and enabled. Finally, the calibration sequence should be followed to prepare the Dual ProSLIC for optimal operation.

Calibration of the Dual ProSLIC provides optimal SLIC function, measurement accuracy, and audio performance. Calibrations should be performed only during an on-hook condition. Refer to AN58 for the complete initialization and calibration method.

Document Change List

Revision 0.3 to Revision 0.4

- Added information on proper PCB heat slug design for the Si322x and Si3200.
- Added information on dv/dt limit for V_{BAT}.
- Removed initialization and calibration information referencing “AN58: Si3200/Si3225 Programmer’s Guide” where detailed initialization and calibration procedures can be found.
- Added Figures 1, 2, 3.

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