Le89156
Single Channel Wideband FXS
VE890 Series
Data Sheet

Features

- **Complete BORSCHT Functions in a Single 48-Pin QFN Package**
  - **B**attery feed, **O**ver-voltage support, integrated **R**inging, line **S**upervision, **C**odec, **H**ybrid (2W/4W), and **T**est
  - Combines *VE8910* SLIC and SLAC devices
- **Integrated Power Management**
  - Built-in DC/DC controller configurable for inverting-boost or flyback operation
  - Input voltage (V_{SW}) range: +4.4 V to +15 V
  - Low power idle mode
- **Worldwide Programmability**
  - Input impedance, balance impedance, and gain
  - DC feed voltage and current limit
  - Ringing frequency, voltage and current limit
  - Caller ID generation (FSK and DTMF)
  - Call progress tone generation
  - Sample coefficients for 44 countries
- **Ringing**
  - 5 REN support
  - Up to 92-V_{PK} internal balanced sinusoidal
- **Wideband 16 kHz Sampling Mode**
- **G.711 µ-Law, A-Law, or 16-Bit Linear Coding**
- **Three Programmable GPIO Pins**
- ***VoicePath*™ SDK and *API-II* Software Available to Implement FXS Functions**
  - Significantly reduces development and testing time
  - Configuration via *VoicePath Profile Wizard*
- ***VeriVoice*™ Software Suites Available for Manufacturing and Subscriber Loop Testing**
- **Supported by Evaluation Module and Reference Designs**
- **Small Footprint 48-Pin QFN, 7x7x0.9 mm**
- **Pb-Free, RoHS-Compliant**
- **-40°C to +85°C Operating Range**

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Ordering Information

Le89156PQC	48-pin QFN (Green)(1)	Tray(2)

1. The Green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.
2. For delivery using a tape and reel packing system, add a "T" suffix to the OPN (Ordering Part Number) when placing an order.

Applications

- **DSL Residential Gateways and Integrated Access Devices (IADs)**
- **Cable eMTAs**
- **PON Single Family Units (SFUs)**
- **Broadband VoIP Gateways**

Description

The Microsemi® Le89156 is an integrated, single channel FXS device optimized for VoIP access devices. It implements a complete BORSCHT functionality by providing the necessary voice interface functions to power, ring, signal, and connect one or more telephones. On the digital side, the Le89156 provides standard MPI and PCM interfaces to leading VoIP processors.

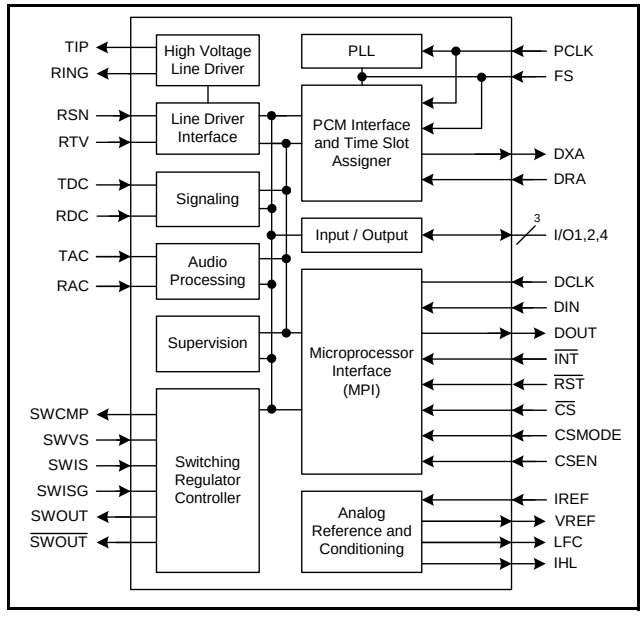

Figure 1 - Functional Block Diagram

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1.0 Le89156 VoicePath Solution Overview

The Microsemi Le89156 *VoicePath* solution consists the Le89156 FXS Device, the *VoicePath Application Programming Interface II* (*VP-API-II*), and the *Profiles* data structures (see Figure 2).

The Le89156 Single Channel Wideband FXS device is an integrated, cost effective subscriber line solution for worldwide short-loop and VoIP applications. It combines the popular and field proven *VE8910* SLIC and SLAC into a single, space saving and thermally efficient 48-pin QFN package.

The Le89156 supports all the traditional **BORSCHT** (**B**attery feed, **O**ver-voltage support, integrated **R**inging, line **S**upervision, **C**odec, **H**ybrid (2W/4W), and **T**esting) functions for interfacing to analog telephones.

The SLIC block provides the high-voltage line interface whereas the SLAC block provides higher-level functions, such as audio signal conversion and processing, impedance synthesis and call control signal generation and detection.

The Microsemi *VP-API-II* software initializes the Le89156 FXS device with *Profiles* (data structures) containing country- or system- specific AC and DC parameters, ringing and other signaling characteristics, as well as switcher settings. The *VP-API-II* software normally resides on the customer's VoIP processor or SoC and provides high-level control over the telephony functions. It is available in Full and Lite versions.

The Microsemi *VoicePath SDK* provides easy-to-use development and test tools for reliable software and a quick time to market. The SDK includes *Profile Wizard,* a *Microsoft*® *Windows*® Graphical User Interface (GUI) application for automatically generating the sets of *Profiles* based on the target system and supported country requirements.

The Microsemi *VeriVoice Auditor* and the *VeriVoice Professional* software suites provide industry-compliant line test software based on the *VP-API-II*.

The Le89156 is the latest member of the *VE890 Series*, which also features the *VE8911* (1FXS + 1FXO) and *VE8901* (1FXO). Designers can mix multiple members of the *VE880* and *VE890 Series* and have a solution with the right number of FXS and FXO interfaces. Product variants are easily supported due to the modularity of the hardware building blocks and the common software API (Application Programming Interface).

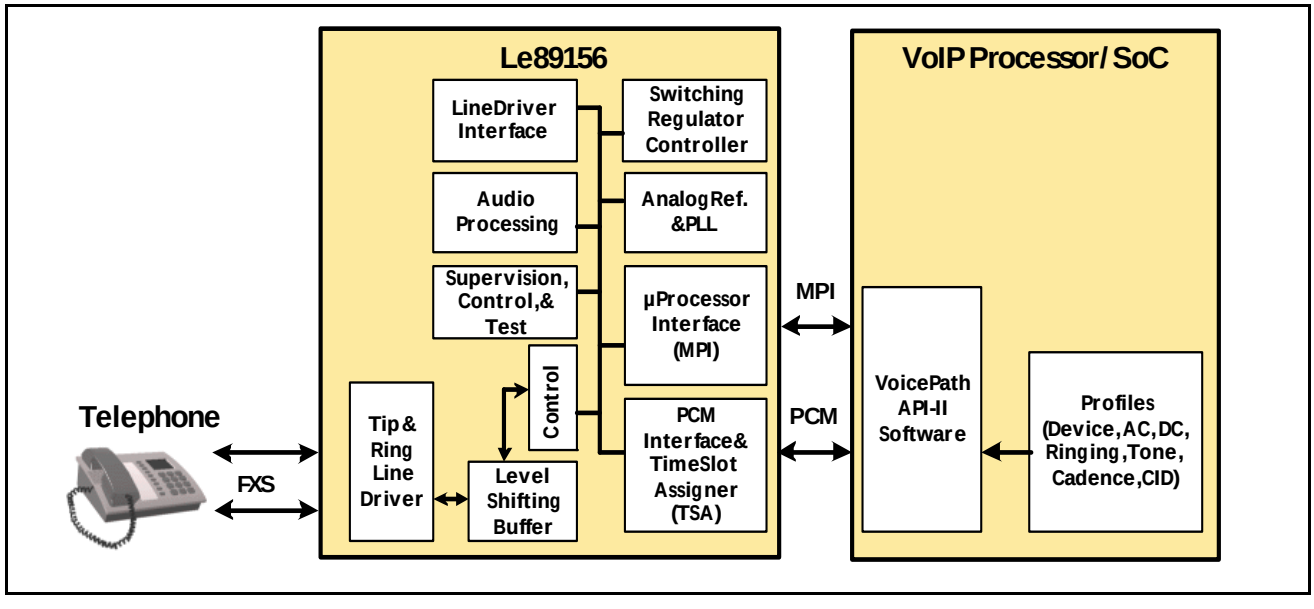

Figure 2 - Le89156 VoicePath Solution

2.0 VoicePath SDK and API-II

2.1 VoicePath SDK Overview

The *VoicePath Software Development Kit* (*SDK*) is a software package provided to simplify development using Microsemi voice products. It consists of:

1. *VoicePath API-II* or *VoicePath API-II Lite* – C source libraries to abstract the *VE890* family devices from the application code. The *VP-API-II* contains the full software and requires a Software License Agreement (SLA). The *VP-API-II Lite* is a subset of the full *VP-API-II* and allows for basic functionality for initialization and state / event handling. It does not include tone cadencing or Caller ID generation. The *VP-API-II Lite* does not require an SLA and is suitable for use in open-source applications. This data sheet and associated feature descriptions and specifications require *VP-API-II* version 2.19 or later be used.
2. *VoicePath Profile Wizard* – The *VP Profile Wizard* is a *Microsoft Windows* GUI application that aids in the organization and creation of country-specific *Profiles* used in the *VP-API-II* into a single project file.
3. Example Hardware Abstraction Layer (HAL) and System Services functions required by *VP-API-II*.
4. Example applications using *VP-API-II* functions. Provided to help the programmer verify correct implementation of the HAL, System Services, and *VP-API-II* function use.
5. Microsemi *Telephony Applications Platform* (*ZTAP*) – This optional hardware platform is used to demonstrate the capabilities of devices or chip sets in the *VE880* and *VE890* families. The *ZTAP* may also be used for software development.
6. *ZTAP Support Package* – This software package contains system files for the *ZTAP* board and *Microsoft Windows* USB drivers for communicating with it.
7. Microsemi *Voice Toolkit* – A collection of menu-driven applications to be used in conjunction with the *ZTAP* for demonstration and testing. It includes *VP-Script*, a TCL/TK-based scripting environment, and *Mini-PBX*, a call control and routing application.

The documentation in the *VoicePath SDK* includes:

1. *VoicePath API-II CSLAC Reference Guide*. This guide describes the *VP-API-II* architecture and discusses its features.
2. *VP-API-II Tutorial*. This slide presentation provides a practical introduction to *VP-API-II* and how it can be used in a wide range of applications.
3. *ZTAP User's Guide*. This document describes the use and operation of the *ZTAP*. It includes "Getting Started" using *VP-Script* and *Mini-PBX* application.

2.2 VoicePath API-II Software

2.2.1 Introduction

The Microsemi V*oicePath Application Programming Interface II* (*VP-API-II*) is a 'C' source code module designed to provide a common interface to the Microsemi family of SLIC, DAA, SOLAC, SLAC, and FXS devices. It provides a high level of abstraction while maintaining the flexibility to allow applications to provide varied voice services. The *VP-API-II* code conforms to the *ANSI* C standard making it easy to port into any embedded application written in 'C' or 'C++'. This section describes a few of the device and line control capabilities using the *VP-API-II* interface. For a complete list, refer to *VoicePath API-II CSLAC Reference Guide*.

VP-API-II uses the layered architecture shown in Figure 3, on page 8. The portion of the diagram in white is Microsemi-provided, while the gray software portions are customer-provided. Microsemi supplies example "gray" code for the *ZTAP* platform.

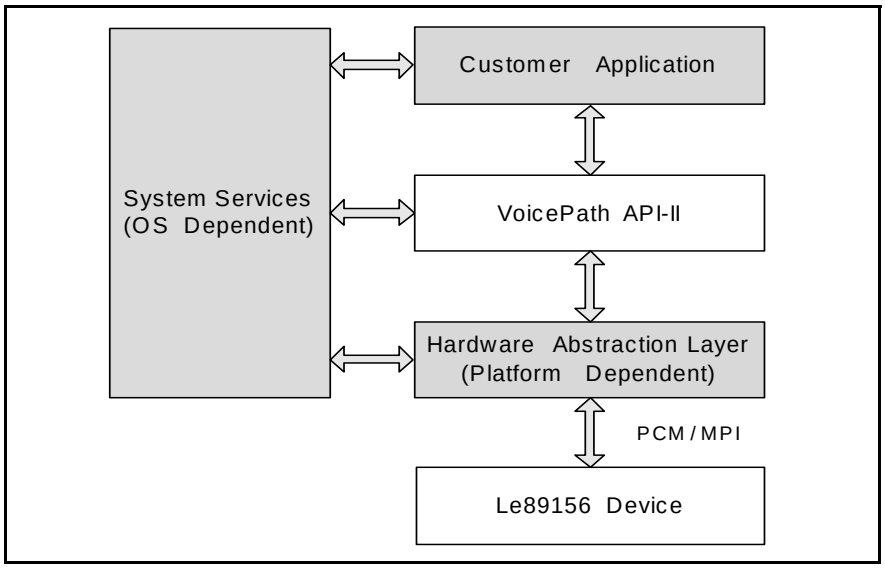

Figure 3 - VoicePath Software Architecture

2.2.2 Features Overview

The features directly supported by *VP-API-II* are dependent upon the underlying device capabilities. For the Le89156 the following features are supported:

- AC and DC coefficient programming
- Ringing parameter (amplitude, frequency, bias, type)
- Tone generation (frequency and amplitude)
- Programmable tone and ringing cadence
- Universal Caller ID generation (Types 1 and 2) with FSK and DTMF signaling
- Loop start signaling, including dial pulse detection
- Seamless integration with the Microsemi *VeriVoice* test packages for *Telcordia® GR-909-CORE* testing
- Four modes of interrupt support

2.2.3 Configuring VP-API-II for the Le89156

Two main functions in *VP-API-II* are required in all applications:

1. `VpMakeDeviceObject()` - Configures a specific device (chip select) to a device context. Provides *VP-API-II* with device specific type (`deviceType`).
2. `VpMakeLineObject()` - Configures a specific line (channel) to a line and device context. Provides *VP-API-II* with line specific type (`termType`).

When using the Le89156, the following settings must be used:

- The value for `deviceType` in `VpMakeDeviceObject()` must be: `VP_DEV_890_SERIES`
- The value for `termType` in `VpMakeLineObject()` must be:
  - `VP_TERM_FXS_GENERIC` when `channelId` = 0 and Normal Standby operation is desired
  - `VP_TERM_FXS_LOW_PWR` when `channelId` = 0 and Low Power Standby operation is desired. Note that this feature requires that the resistor RLP shown on *Le89156 Line Interface Circuit* be populated.

Please refer to *VoicePath API-II CSLAC Reference Guide* for additional details.

2.3 VoicePath Profile Wizard

The *VP Profile Wizard* is a *Windows*-based application that lets the user select the values of all the *Profiles* that are supported by the *VP-API-II*. It automatically generates the coefficient files that the API needs to operate. Figure 4 shows a typical screenshot for getting started and creating a new project. Note that the Le89116 SLAC is shown in the example since this is the SLAC block inside the Le89156.

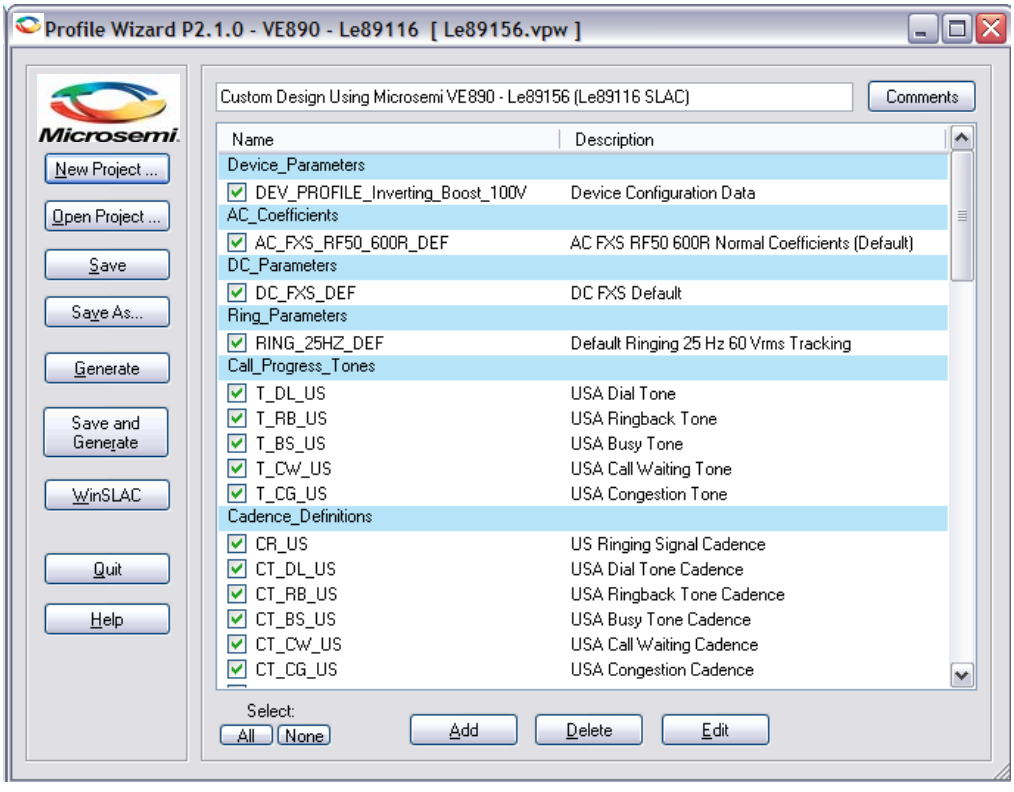

Figure 4 - Profile Wizard Screen - Creating a New Project

Using the *VoicePath Profile Wizard* a designer can easily define and generate *Profiles* meeting different country requirements. The Le89156 supports seven types of *Profiles* (see Table 1).

Profile Name	Description
Device	The *Device Profile* provides the Pulse Code Modulation (PCM) bus clock frequency and configuration information, interrupt mode, driver tick rate, maximum number of events / tick, and switching regulator configuration.
AC	The *AC Profile* is a transmission characteristic profile. The *AC Profile* holds the internal DSP gain block and filter block commands and data for the FXS channel. Multiple *AC Profiles* are provided, one for each supported country.
DC	The *DC Profile* holds the FXS device's DC feed and loop supervision parameters.
Ring	The *Ring Profile* contains the necessary commands and data to set up the ring generator of an FXS channel. Different profiles can be used to vary the ringing characteristics of a line. Options available in the *Ring Profile* include ringing waveform, frequency, amplitude, and DC offset.
Tone	The *Tone Profile* defines the various call progress tones that might be used in the FXS channel. The tones include dial tone, busy, ring-back, and re-order.

Table 1 - VoicePath API-II Profiles

Cadence	The *Cadence Profile* defines the various call progress cadences that might be used in a system. The cadences include stutter dial, busy, ring-back, and reorder.
Caller ID	The *Caller ID Profile* defines the on- and off-hook signal generation for services such as calling line identification and message waiting indication. This profile abstracts the physical and data link layers of the protocol. FSK and DTMF signaling are supported.

Table 1 - VoicePath API-II Profiles

2.4 MPI Access Layer

The MPI Access Layer encapsulates the functions needed to access a SLAC through its MPI interface. The MPI is the serial communications link between the system's VoIP processor and SLAC blocks or devices in the system. This layer encapsulates the details of the system hardware interface between the host VoIP processor and the SLAC blocks or devices. This layer is provided by the system designer and is dependent upon the customer's specific hardware design. Microsemi provides example MPI code for use with the *ZTAP* platform.

Function Name	Description
`VpMpiCmd()`	HAL function to provide buffered MPI command and data to the device, and receive MPI data from the device.

Table 2 - VP-API-II Functions for MPI Access

2.5 System Services Layer

System Services encapsulates various services provided by the system software (RTOS or BSP) such as interrupt control, queue management, and timing services. This layer translates between the system services that the *VP-API-II* requires and the underlying hardware/software environment. When porting to a different hardware/software platform, only the Systems Services and the MPI layers are expected to change. Microsemi provides example System Services code for use with the *ZTAP* platform.

Function Name	Description
`VpSysWait()`	Delay operator used to suspend program/thread execution. Delay parameter passed in 125 µs steps.
`VpSysEnterCritical()`	A semaphore operation to provide protected access to device or shared memory. Required only in multi-threaded architectures.
`VpSysExitCritical()`	A semaphore operation to release protected access to device or shared memory. Required only in multi-threaded architectures.

Table 3 - VP-API-II Functions for System Services

3.0 FXS Channel Operation

3.1 FXS Channel Overview

- Performs all **BORSCHT** (**B**attery feed, **O**ver-voltage support, Integrated **R**inging, Line **S**upervision, **C**odec, **H**ybrid (2W/4W), and **T**esting) functions
- Provides high voltage line driving, digital signal processing, and high voltage power generation
- Wideband 16 kHz and Narrowband 8 kHz sample rates
- Exceeds *Telcordia GR-909-CORE* transmission requirements
- Low Power Standby with 70 mW typical on-hook consumption
- Single hardware design meets worldwide requirements through software programming of:
  - Ringing waveform, frequency and amplitude
  - DC loop-feed characteristics and current-limit
  - Loop-supervision detection thresholds
  - Off-hook debounce circuit
  - Ground-key and ring trip filters
  - Two-wire AC impedance
  - Transhybrid balance impedance
  - Transmit and receive gains
  - Transmit and receive equalization
  - Three programmable digital I/O pins
  - µ-law/A-law and linear selection
  - Switching power supply
- On-hook transmission
- Power/service denial mode
- Supports wink function
- Neon lamp driving capability
- Smooth polarity reversal
- Overcurrent protection
- Self-contained ringing generation and control
  - Programmable ringing cadencing
  - Internal battery-backed balanced or unbalanced, sinusoidal or trapezoidal ringing
- Integrated ring-trip filter and software enabled manual or automatic ring-trip mode
- Flexible tone generation
  - Howler tone generation
  - Call progress tone generation
  - DTMF tone generation
  - Universal Caller ID generation (Types 1 and 2), FSK and DTMF signaling
- Only 3.3 V logic and single battery supply needed
- Integrated switching regulator controller
  - Programmable for Inverting-Boost, Flyback, or Buck-Boost modes
  - Allows for efficiency in all states
  - Line-feed characteristics independent of battery voltage
- Compatible with inexpensive protection networks; accommodates low-tolerance PTC's while maintaining longitudinal balance
- Monitors two-wire interface voltages and currents for subscriber line diagnostics
- Can monitor and/or drive Tip and Ring independently
- Built-in voice-path test modes
- Integrated self-test features
- 3V relay driver (external catch diode required)
- Internal hook buffer allows for up to 10 ms system polling rate
- 100% software-compatible with the Microsemi *VE8910* chipset
- Supported by *VoicePath API-II (VP-API-II)* software and *Software Development Kit (SDK)*
- Large heat sink pad for excellent thermal dissipation
- Thermal resistance (θ_{JA}): 23.5°C/W
- 48-pin QFN measuring 7x7x0.9 mm
- Lead spacing: 0.5 mm
- Lead free, RoHS compliant
- MSL 3, per *JEDEC J-STD-020*. Supports 260°C reflow
- -40°C to +85°C operation

3.2 Le89156 Device Block Diagram

Figure 5 shows the major functional blocks of the Le89156 device.

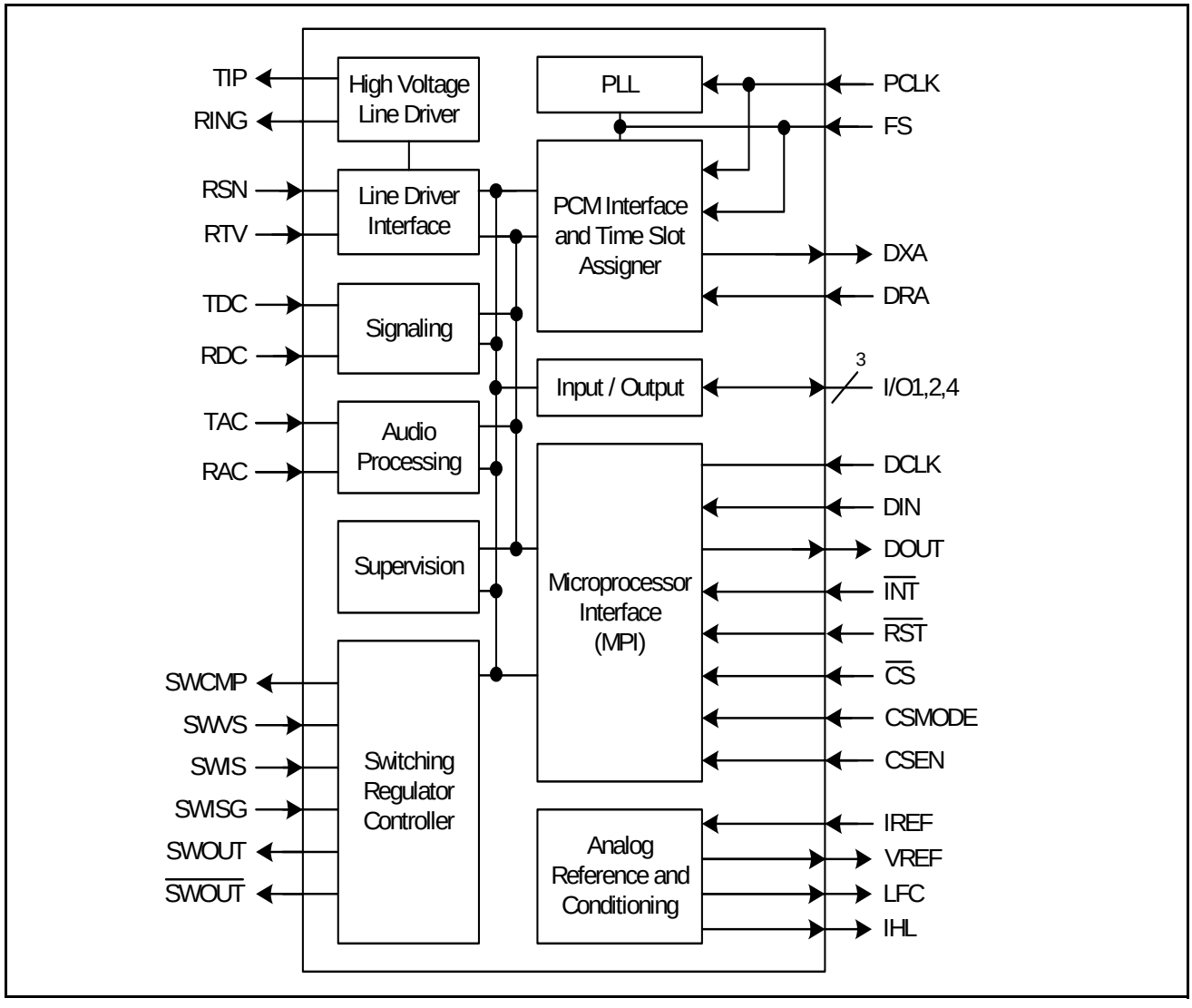

Figure 5 - Le89156 Device Block Diagram

3.3 Device Profile

3.3.1 Overview

The *Device Profile* configures device or circuit level parameters for the entire device. This profile is required to enable reliable MPI access to the device, to configure the switching regulator, and to define *VP-API-II* driver parameters. The *Device Profile* for the *VE890* chipset using *VP Profile Wizard* is shown in Figure 6.

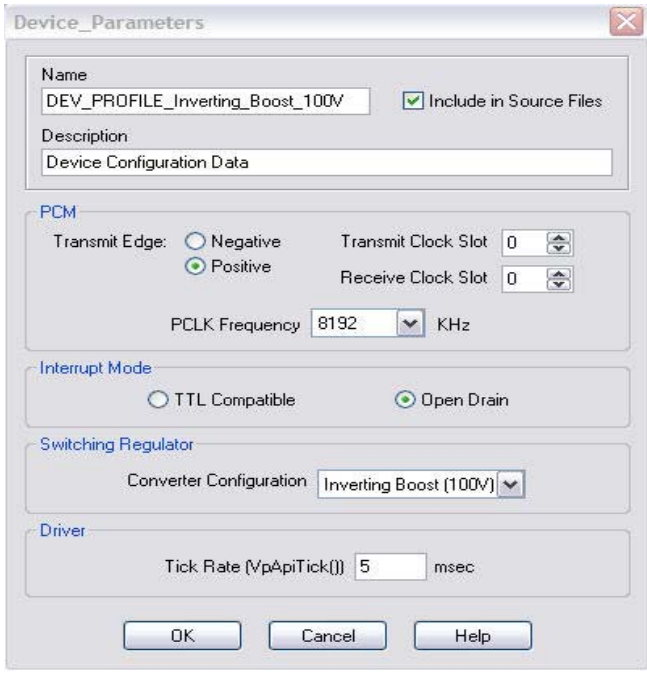

Figure 6 - Profile Wizard - Device Profile Configuration

Function Name	Description
`VpInitDevice()`	Resets and initializes device with parameters defined in *Device Profile* and optionally configures all lines on the device with AC, DC, and ringing parameters.
`VpCalLine()`	This function may need to be called under some circumstances following the above function. Refer to the *VP-API-II CSLAC Reference Guide* for more details.

Table 4 - VP-API-II Functions for Device Profile

3.3.2 Switching Regulator Controller

The Le89156 supports three options for implementing a DC-DC switching power supply to create the large negative voltage needed to drive the telephone line. The inverting-boost topology (see Figure 43, on page 60) is recommended for most applications as it is the most cost-effective while yielding high efficiency and low cost. The flyback topology (see Figure 44, on page 63) is recommended when isolation or a wider input range are required. The buck-boost topology, a transistor-based variant of the inverting-boost, is supported for legacy applications, but is not recommended for new designs as it is more expensive and less efficient than inverting-boost. Each customer can choose the topology most appropriate to his/her application.

The variable output switching regulator is used to generate the V_{BAT} supply voltage needed for the FXS line. An offset voltage (set by the V_{AS} DC feed parameter) is added to the measured Tip-Ring voltage and the resulting signal

controls the output of the switching regulator. When loop current is drawn, an additional offset defined as 200 * Iloop is added, to ensure overhead is maintained with up to 100 Ω of total fuse resistance present in the DC feed loop. This architecture enables the switching regulator output voltage to generate the required voltage to feed the line whether in the *On-Hook*, *Off-Hook* or *Ringing* states. The result is maximum power efficiency and minimum power dissipation in all states because the regulator output is always optimum for the current state.

The switching regulator controller on the Le89156 allows the negative voltage used for driving and ringing the line to be generated from a single external power supply of typically +12 V_{DC}. Various combinations of power supply can be configured depending on the requirements of the target application. See the applications section for details of the switcher reference designs. The switcher topology, operating frequency, and the battery voltage levels are set in the *Device Profile* as shown in Figure 6, on page 13.

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3.4 Functional Description

3.4.1 AC Profile

AC Profiles are used to define the input impedance, receive and transmit frequency response, hybrid balance, and initial values for receive and transmit gain. *VP Profile Wizard* provides example FXS *AC Profiles* for over 44 countries including the following:

Input Impedance	Notes
150 Ω + (510 Ω // 47 nF)	Russia
200 Ω + (680 Ω // 100 nF)	China
220 Ω + (820 Ω // 115 nF)	Austria, Bulgaria, and Germany
220 Ω + (820 Ω // 120 nF)	Australia and South Africa
270 Ω + (750 Ω // 150 nF)	*ETSI ES 203 021* (EU countries not listed elsewhere + Iceland, Israel, Norway, and Switzerland
270 Ω + (910 Ω // 120 nF)	Finland
370 Ω + (620 Ω // 310 nF)	New Zealand and United Kingdom
600 Ω	USA, Argentina, Canada, Chile, Hong Kong, India, Korea, Singapore, and Taiwan. It is also the default selection if no countries are specified.
600 Ω + 1.0 µF	Japan and PBX
900 Ω	Brazil
900 Ω + 2.16 µF	*Telcordia GR-57-CORE* Non-Loaded Loop

Table 5 - Supported AC Source Impedances

Notes:

1. *Table 5 provides suggested AC FXS input impedances for the listed countries and standards and are believed to be accurate as of the date of publication of this document. However, standards can and do change from time to time or new ones may be introduced which may differ from the examples provided by Microsemi. Some countries may support more than one standard impedance. Customers are responsible for making sure that they are using the appropriate AC Profiles for their application.*
2. *VP Profile Wizard makes it easy to add additional countries as long as they are based on the supported impedances.*
3. *The standard files provided with VP Profile Wizard are for FXS interfaces with two 25 ohm series resistors or PTC's. Please contact Microsemi CMPG Customer Applications if alternate series resistor or PTC resistance values are planned.*
4. *Narrowband and Wideband versions of these Profiles are available.*

Function Name	Description
`VpInitDevice()`	Resets and initializes device with parameters defined in *Device Profile* and optionally configures all lines on the device with AC, DC, and ringing parameters.
`VpInitLine()`	Resets and initializes line with AC, DC, and ringing parameters.
`VpConfigLine()`	Configures line with AC, DC, and ringing parameters. Similar to `VpInitLine()` but line is not reset. Values not provided in function call result in line retaining previously set parameters.
`VpCalLine()`	This function may need to be called under some circumstances following the functions listed above. Refer to the *VP-API-II CSLAC Reference Guide* for more details.

Table 6 - VP-API-II Functions for AC Profile

The hardware sections of the device programmed by *AC Profiles* are described in the following sections.

3.4.2 Voice Signal Processor

This block, shown in *Voice Signal Processing Block Diagram,* on page 16, performs digital signal processing for the transmission and reception of voice. It includes *G.711* compression/decompression, filtering, gain scaling, general-purpose tone generators, Caller ID FSK generation, and DTMF generation.

This block performs the codec and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters perform the following functions:

- Sets the receive and transmit gain
- Performs the transhybrid balancing function
- Permits adjustment of the two-wire termination impedance
- Provides frequency attenuation adjustment (equalization) of the receive and transmit paths

All programmable digital filter coefficients can be calculated using the Microsemi *WinSLAC*™ software. The PCM codes can be either 16-bit linear two's-complement or 8-bit companded µ-law or A-law.

Besides the codec functions, the integrated voice processing block provides all the sensing, feedback, and clocking necessary to completely control SLIC block functions with programmable parameters. System-level parameters under programmable control include active loop current limits, open circuit feed voltages, and loop supervision thresholds.

The Le89156 is architected in such a way as to reduce the real time demands on the host processor. An integrated cadencer/sequencer controls ringing and call progress tone generation. This feature can also generate timed interrupts and substantially reduces the user’s need to implement time critical functions.

For subscriber line diagnostics, AC and DC line conditions can be monitored by connecting analog currents and voltages to the voice A/D converter. This gives the system’s host processor the ability to configure the system and make system and line tests. Both longitudinal and metallic resistance and capacitance can be measured. This allows identification of leakage resistance, line capacitance, and the presence and status of telephones. These tests are all supported by the Microsemi *VeriVoice* software.

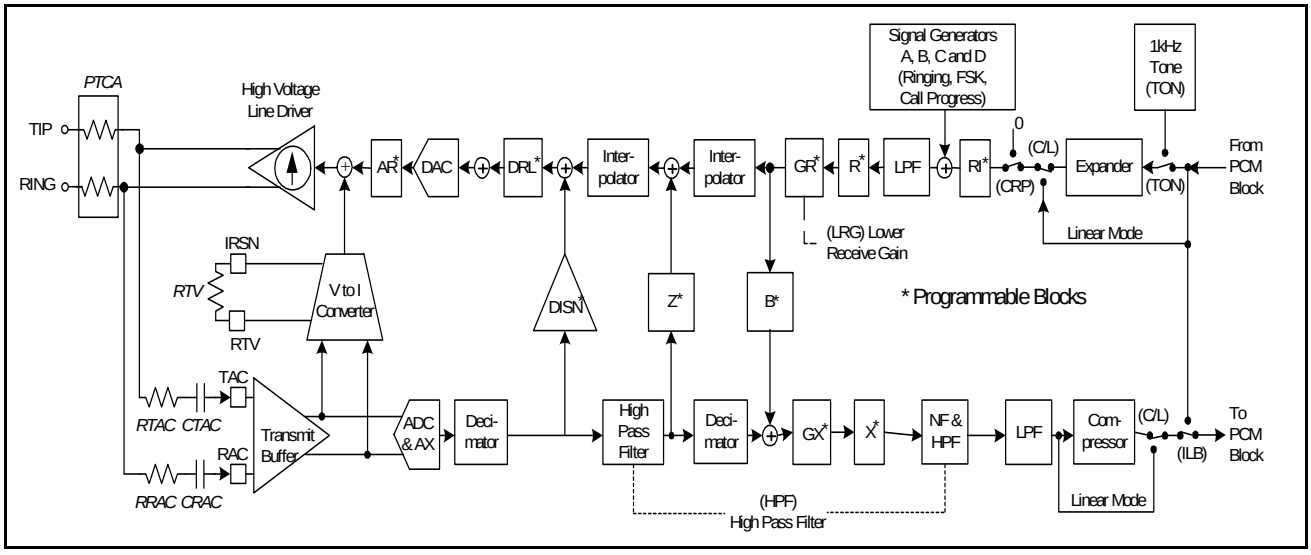


Figure 7 - Voice Signal Processing Block Diagram

3.4.2.1 Impedance Synthesis

The analog impedance synthesis loop is comprised of the SLIC block, the AC sense path components, the transmit amplifier, and a voltage to current converter. An external resistor, R_{TV}, synthesizes the nominal impedance in the analog domain. Additional refinement of the impedance is done in the DSP via the Digital Impedance Scaling Network (DISN) and Z-blocks.

The DISN path is comprised of the voice A/D and its first stage of decimation, a DISN, and the voice DAC. The 8-bit DISN synthesizes a portion of the AC impedance which appears in parallel with R_{TV} and is used to modify the impedance set by the external analog network.

The Z Filter is a programmable digital filter providing an additional path and programming flexibility over the DISN in modifying the transfer function of the synthesis loop. Together R_{TV} , DISN, and the Z Filter enable the user to synthesize virtually all required telephony device input impedances.

3.4.2.2 Frequency Response Correction and Equalization

The voice signal processor contains programmable filters in the receive (R) and transmit (X) directions that may be programmed for line equalization and to correct any attenuation distortion caused by the Z Filter.

3.4.2.3 Transhybrid Balancing

The voice signal processor's programmable B Filter is used to adjust transhybrid balance. The filter has a single pole Infinite Impulse Response (IIR) section and an eight-tap Finite Impulse Response (FIR) section, both operating at 16 kHz.

3.4.2.4 Gain Adjustment

The transmit path of the FXS has two programmable gain blocks. Gain block AX is an analog gain of 0 dB or 6.02 dB (unity gain or gain of 2.0), located immediately before the A/D converter. GX is a digital gain block that is programmable from 0 dB to +12 dB, with a worst-case step size of 0.1 dB for gain settings below +10 dB, and a worst-case step size of 0.3 dB for gain settings above +10 dB. The filters provide a net gain in the range of 0 dB to 18 dB. The receive voice path has three programmable gain blocks. GR is a digital loss block that is programmable from 0 dB to 12 dB, with a worst-case step size of 0.1 dB. DRL is a digital loss block of 0 dB or 6.02 dB. AR is an

analog gain of 0 dB or 6.02 dB (unity gain or gain of 2) or a loss of 6.02 dB (gain of 0.5), located immediately after the D/A converter. This provides an attenuation in the range of 0 dB to 18 dB.

The gain adjustment block can also be accessed by a *VP-API-II* function directly, without using an *AC Profile*.

Function Name	Description
`VpSetRelGain()`	Adjusts transmit and/or receive gain up to +/-6 dB. Relative gain of 1 (0 dB) defined as initial value programmed by *AC Profile*. Note that the supplied *AC Profiles* have initial FXS gains of -6 dBr receive and 0 dBr transmit
`VpSetOption()`	`VP_OPTION_ID_ABS_GAIN` -- Programs absolute gain

Table 7 - VP-API-II Functions for Gain Adjustment

3.4.3 Transmit Signal Processing

In the transmit path (A/D) of the FXS, the AC Tip - Ring analog input signal is sensed by the TAC and RAC pins, buffered, amplified by the analog AX gain and sampled by the A/D converter, filtered, companded (for µ-law or A-law), and made available to the PCM blocks. If linear format is selected, the 16-bit data will be transmitted in two consecutive time slots starting at the programmed time slot. The B, X, and GX digital filter blocks are user-programmable digital filter sections. The first high-pass filter is for DC rejection, and the second high pass and notch filters reject low frequencies such as 50 Hz or 60 Hz. In Wideband mode, the second high pass and notch filters are bypassed.

3.4.3.1 Receive Signal Processing

In the receive path (D/A) of the FXS port, the digital signal is expanded (for µ-law or A-law), filtered, interpolated, converted to analog, and driven onto TIP and RING by the SLIC block. The AR, DRL, DISN, Z, R, and GR blocks are user-programmable filter sections.

3.4.4 Speech Coding

3.4.4.1 Linear and Compressed

The A/D and D/A conversion follows either the µ-law or the A-law standard as defined in *ITU-T Recommendation G.711.* Alternate bit inversion is performed as part of the A-law coding. Linear code is an option on both the transmit and receive sides of the device. Two successive time slots are required for linear code operation. The linear code is a 16-bit two's-complement number which appears sign bit first on the PCM highway.

3.4.4.2 Wideband Codec Mode

The Le89156's SLAC block can be operated in a Wideband mode under software API control. In the Wideband mode, the nominal voice bandwidth is doubled to 150 Hz to 6800 Hz to provide better voice quality. The *AC Profiles* in the Le89156's SLAC block must be reprogrammed from the values used in Narrowband mode. In the Wideband mode, the increased data rate is processed by accessing a second set of timeslots equally spaced in the frame. While linear is the usual codec mode, µ-law or A-law companding may also be used in Wideband mode.

Function Name	Description
`VpSetOption()`	`VP_OPTION_ID_TIMESLOT` -- Programs transmit and receive timeslot. `VP_OPTION_ID_CODEC` -- Programs speech coding mode.
`VpGetOption()`	`VP_OPTION_ID_TIMESLOT` -- Retrieves current values of transmit and receive timeslot. `VP_OPTION_ID_CODEC` -- Retrieves current speech coding mode.

Table 8 - VP-API-II Functions for Speech Coding

3.4.5 DC Profile

DC Profiles are used to define the feed and loop supervision conditions of the line. The default *DC Profile* for *VE890* devices using *VP Profile Wizard* is shown in Figure 8.

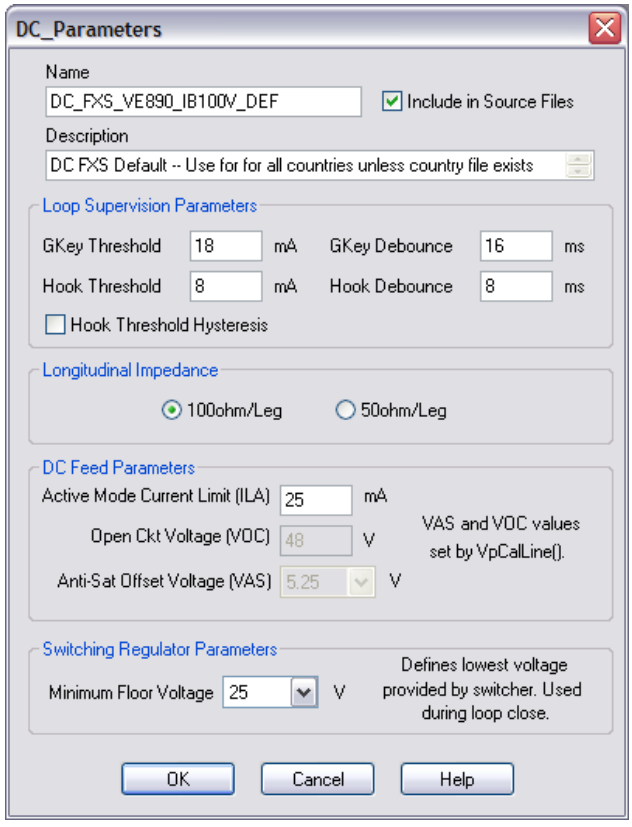


Figure 8 - Profile Wizard - DC Profile Configuration

Function Name	Description
`VpInitDevice()`	Resets and initializes device with parameters defined in *Device Profile* and optionally configures all lines on the device with AC, DC, and ringing parameters.
`VpInitLine()`	Resets and initializes line with AC, DC, and ringing parameters.
`VpConfigLine()`	Configures line with AC, DC, and ringing parameters. Similar to `VpInitLine()` but line is not reset. Values not provided in function call result in line retaining previously set parameters.
`VpCalLine()`	This function may need to be called under some circumstances following the functions listed above. Refer to the *VP-API-II CSLAC Reference Guide* for more details.

Table 9 - VP-API-II Functions for DC Profile

DC feed is active in the `VP_LINE_STANDBY`, `VP_LINE_ACTIVE`, `VP_LINE_TALK`, `VP_LINE_OHT`, `VP_LINE_TIP_OPEN`, and all equivalent polarity reversal states. The *Idle* and *Active* feed characteristics appear between Tip and Ring in all states except `VP_LINE_TIP_OPEN`, where the characteristic appears from Ring to ground in that state. V_{AS} is chosen to ensure that sufficient headroom is available for the amplifiers when On-Hook to support On-Hook transmission with the programmed open circuit (V_{OC}) voltage. Values programmed in device for V_{AS}, V_{OC}, and I_{LA} are determined during `VpCalLine()` to ensure circuit performance.

The *DC Profile* produces a DC feed curve at Tip and Ring when the fuse resistors are inside the feedback loop formed by the RTDC and RRDC feedback network. Refer to *DC Feed I / V Characteristic*, on page 19.

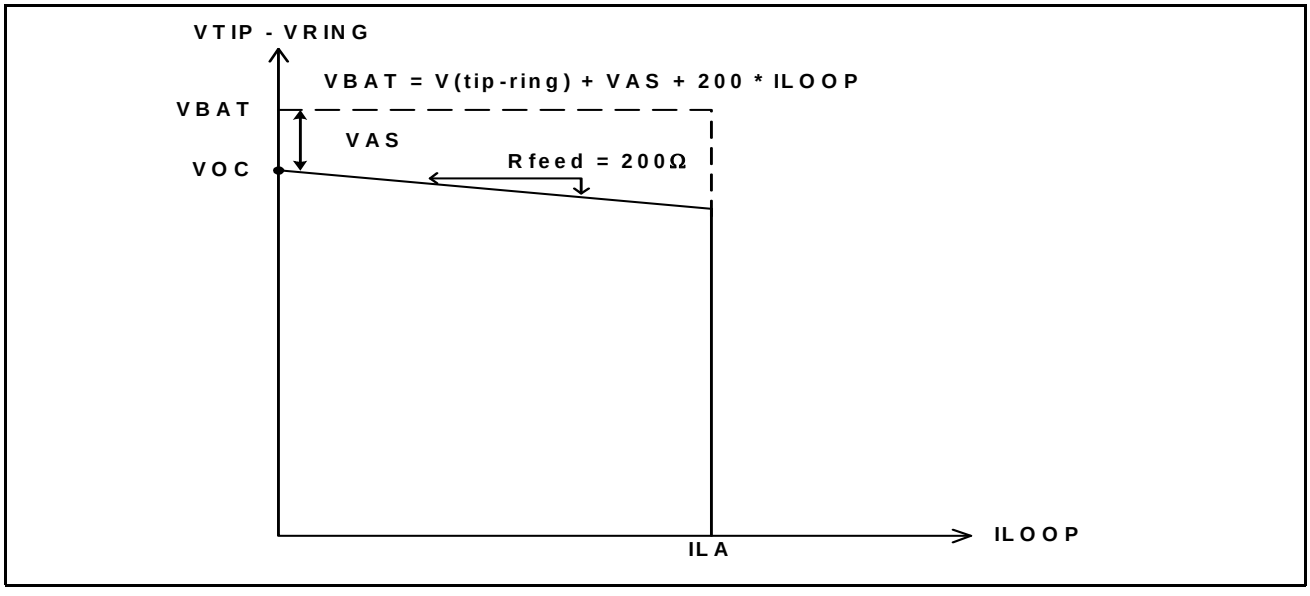


Figure 9 - DC Feed I / V Characteristic

3.4.6 Ring Profile

The *Ring Profile* is used to define the type of ringing, ringing frequency, amplitude, offset, ring trip threshold, and ringing current limit. An example *Ring Profile* for the VE890 chipset using *VP Profile Wizard* is shown in Figure 10.

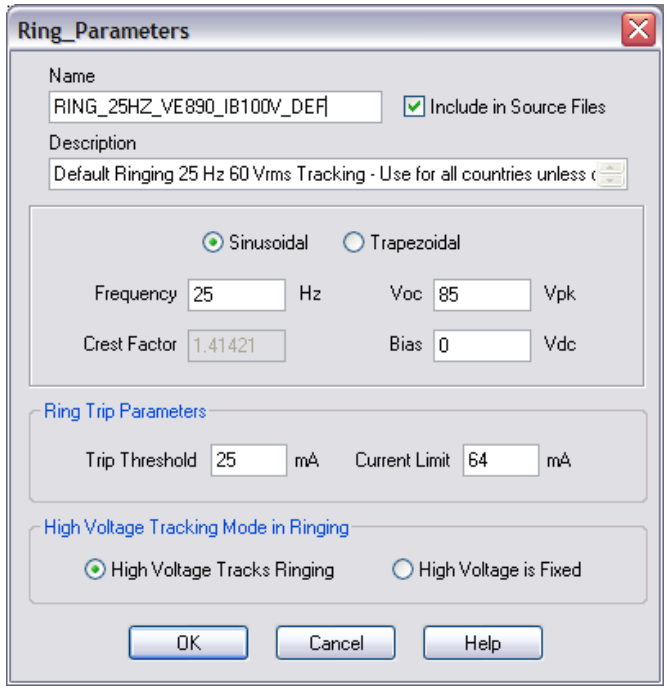


Figure 10 - Profile Wizard - Ring Profile Configuration

Function Name	Description
`VpInitDevice()`	Resets and initializes device with parameters defined in *Device Profile* and optionally configures all lines on the device with AC, DC, and ringing parameters.
`VpInitLine()`	Resets and initializes line with AC, DC, and ringing parameters.
`VpConfigLine()`	Configures line with AC, DC, and ringing parameters. Similar to `VpInitLine()` but line is not reset. Values not provided in function call result in line retaining previously set parameters.
`VpCalLine()`	This function may need to be called under some circumstances following the functions listed above. Refer to the *VP-API-II CSLAC Reference Guide* for more details.

Table 10 - VP-API-II Functions for Ring Profile

The primary hardware section of the device programmed by *Ring Profiles* is Signal Generator A. Signal generators are used for several purposes and will be discussed in section *Tone Profile*, on page 20.

3.4.7 Tone Profile

Tone Profiles provide the capability to program up to four simultaneous tones on the line. An example *Tone Profile* for the *VE890* chipset using *VP Profile Wizard* is shown in Figure 11.

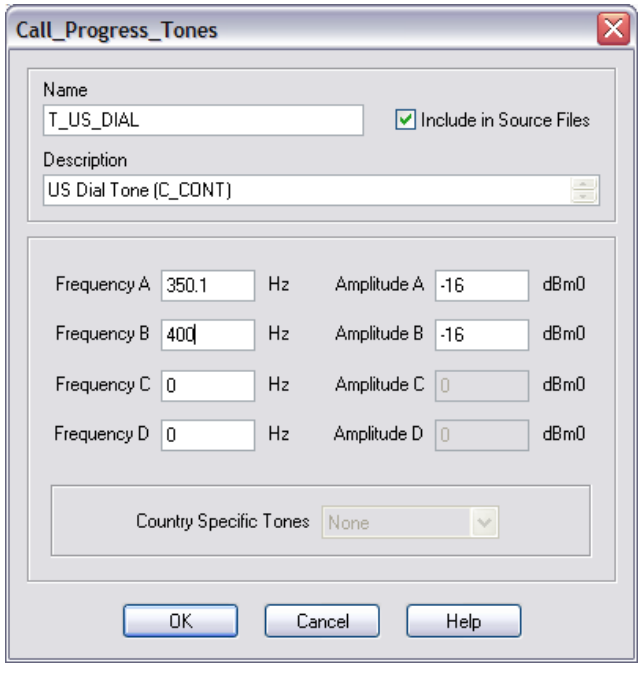


Figure 11 - Profile Wizard - Tone Profile Configuration

Function Name	Description
`VpSetLineTone()`	Starts a tone on the line. The tone can be cadenced or “always on”.

Table 11 - VP-API-II Functions for Tone Profile

Tone generation is performed using highly programmable device signal generators (discussed in *Signal Generation*, on page 21. As discussed later, the signal generators are used for several other *VP-API-II* functions to meet system level requirements.

3.4.7.1 Signal Generation

Up to four digital signal generators are available for the FXS channel. The signal generators are summed into the output path, as shown in Figure 12. The Bias generator produces a DC bias that can be used to provide DC offset during ringing or DC test signals during diagnostics. This generator is automatically enabled when entering the VP_LINE_RINGING state (when ringing is applied to the line). Mentioned previously, the Signal Generators are used by several *VP-API-II* operations.

Function Name	Description
VpSetLineTone()	Provides simultaneous generation of up to four tones. Note that with Tone Cadencing, tones can be enabled/disabled individually to provide Special Indication Tone (SIT).
VpSetLineState()	VP_LINE_RINGING and VP_LINE_RINGING_POLREV -- Uses Signal Generator A (and B for trapezoidal type ringing) with user selected frequency, offset, amplitude, and type.
VpSendSignal()	VP_SENDSIG_DTMF_DIGIT -- Generates a DTMF digit on the line.
VpInitCid()	Sending Caller ID (FSK and DTMF message data supported) on an FXS line. Providing Type 2 CID Alerting tone.
VpSendCid()	
VpContinueCid()	

Table 12 - VP-API-II Functions Using Signal Generators

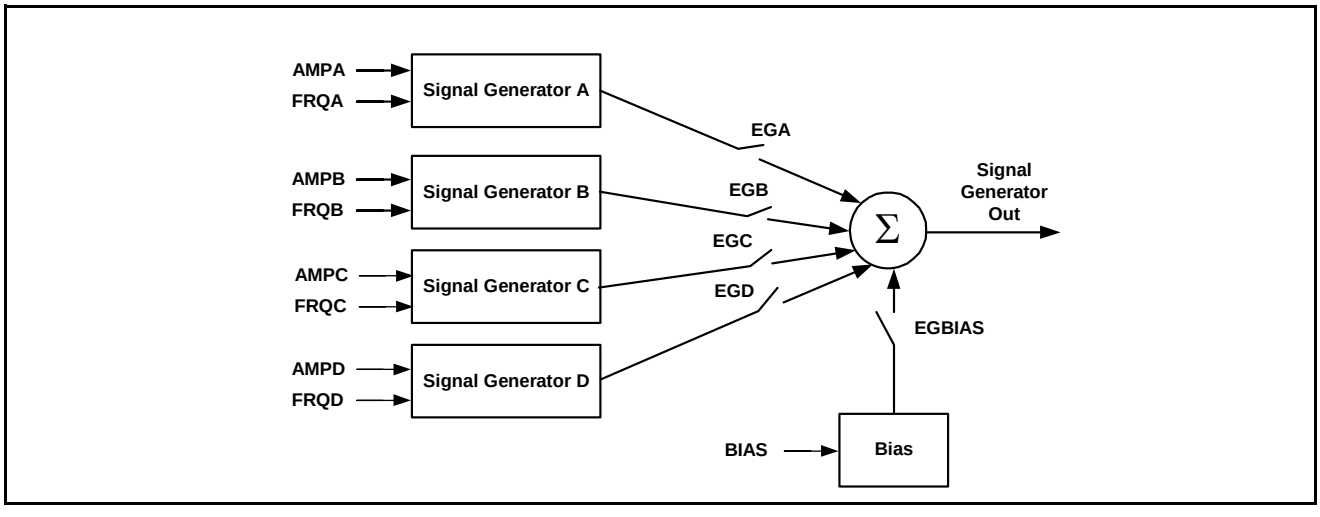


Figure 12 - Programmable Signal Generators

Signal Generator A is also used by the Microsemi *VeriVoice* test suites to produce slow ramps. This allows a complex sequence of diagnostic test voltages to be generated in a controlled manner without generating unwanted transients on the line.

Each generator has independent frequency and amplitude parameters. The frequency accuracy is basically the same as the crystal accuracy of the system.

The EGA/B/C/D bits are controlled by the *VP-API-II* Cadencing engine, described next.

3.4.8 Cadencing

VP-API-II Cadencing is a highly flexible set of operators the user selects to implement any country-specific ringing or tone cadence requirements including Special Information Tones (SIT) and howler tones. Figure 13 shows an example *Cadence Profile* for a busy signal created with *VP Profile Wizard*.

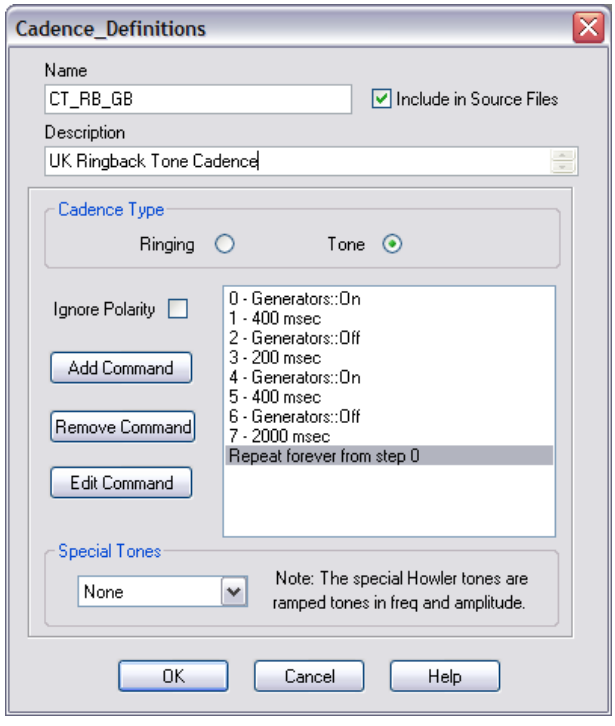


Figure 13 - VP Profile Wizard - Cadence Profile Example Definition

The *VP-API-II* Cadencer supports the following operations:

1. Time -- Delays (in a non-blocking fashion) program execution.
2. Generator Control -- Enable/Disable selection on a per-generator basis.
3. Branch -- Forces the cadencing to return to a previous step with "repeat" for *n* number of times. If *n* == 0, repeat forever.
4. Line State -- Sets line to specific *VP-API-II* Line State.
5. Send CID -- Starts Caller ID (CID) on the line while continuing to run cadence. Used for Type 1 Caller ID when CID occurs after first regular ringing cycle in order to achieve a precise delay between the first and second rings.
6. Wait On Caller ID -- Starts Caller ID on the line and suspends currently running cadence. Used for Type 1 Caller ID when CID occurs prior to the first regular ringing cycle.

Function Name	Description
`VpSetLineTone()`	Provides tone cadencing for up to four tones. Also supports country-specific howler tone cadencing (AUS, UK, NTT) with ramp frequency and amplitude.
`VpSetLineState()`	`VP_LINE_RINGING` and `VP_LINE_RINGING_POLREV` for ringing cadence.
`VpInitRing()`	User function to provide ringing cadence. Also allows use selection of *Caller ID Profile* associated with ringing.

Table 13 - VP-API-II Functions Using Cadencing

3.4.9 Caller ID Generation

The Caller ID block uses Generators C and D to generate phase-continuous 1200 baud FSK tones for on- or off-hook information such as Calling Line ID and Visual Message Waiting Indication. The duration of each (bit) tone is fixed at 0.833 ms (1200 baud).

Bell 202 frequencies are used in the North American market, and the *ITU V.23* frequencies are used in most other international markets. The signal generator amplitude may need to be adjusted depending on the programmed loss plan. Data transmission levels are normally specified as -13.5 dBm +/-1.5 dB. The default amplitude is -7 dBm0.

Exact preamble and mark sequences are generated by adjusting the framing mode and sending the appropriate number of characters. The *VP-API-II* abstracts this into a simple driver level interface. *VP Profile Wizard* enables the user to select the Caller ID parameters and build them into the *Caller ID Profile*, which generates the necessary coefficients and instructions for the API. Please see example in Figure 14 below.

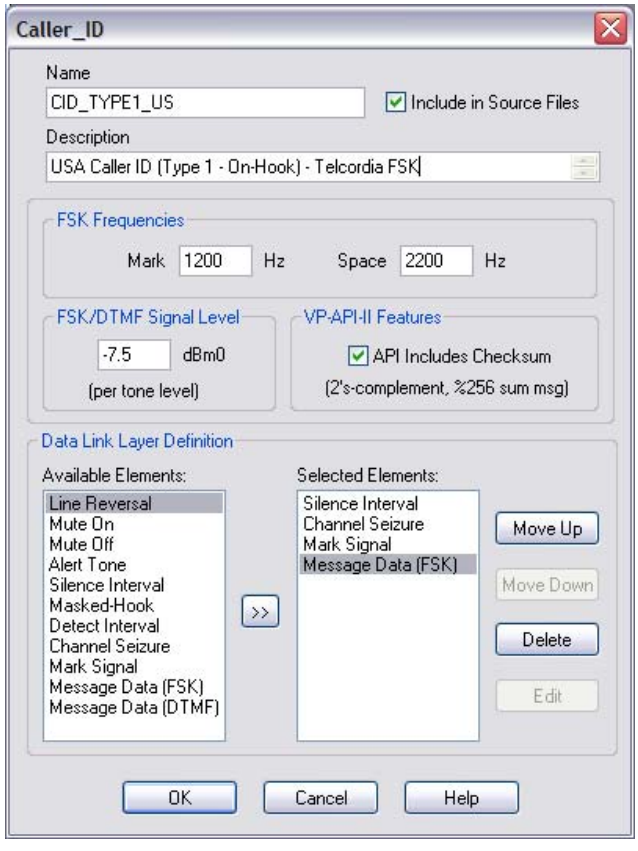


Figure 14 - VP Profile Wizard - Type 1 Caller ID Profile Example Definition

Function Name	Description
`VpInitRing()`	User function to provide *Caller ID Profile* associated with ringing.
`VpSendCid()`	Configures and starts Caller ID immediately. Used for Type 2 Caller ID.
`VpInitCid()`	Input for Caller ID Message Data up to 32 bytes.
`VpContinueCid()`	Input for Caller ID Message Data up to 16 bytes. Called after `VpInitCid()` or `VpSendCid()` when event `VP_LINE_EVID_CID_DATA` is generated.

Table 14 - VP-API-II Functions to Support Caller ID

3.5 VP-API-II Operation States

3.5.1 Calibration

Calibration of certain battery and line parameters is necessary to meet datasheet specifications.

Function Name	Description
`VpCalLine()`	Runs non-blocking calibration routines necessary to meet datasheet specifications. When complete, generates `VP_EVID_CAL_CMP` event. This function must be called after any FXS line initialization function is executed.

Table 15 - VP-API-II Functions for Calibration

3.5.2 Line State Control

The Signaling Control blocks process the Line State information to perform related control functions such as DC feed, ringing generation, and line test for each channel. Eight system states are possible for the operation of the FXS channel on the Le89156: *Shutdown*, `VP_LINE_DISCONNECT`, `VP_LINE_STANDBY`, `VP_LINE_TIP_OPEN`, `VP_LINE_OHT`, `VP_LINE_ACTIVE`, `VP_LINE_TALK`, `VP_LINE_RINGING`, and reverse polarity of each state.

Function Name	Description
`VpSetLineState()`	Sets line to state specified. After `VpInitDevice()` or `VpInitLine()`, the default line state is `VP_LINE_DISCONNECT`.

Table 16 - VP-API-II Functions for Line State Control

3.5.2.1 Shutdown

Shutdown is the power-up and hardware reset state of the device. The System State register is in *Shutdown*, the voice channel is deactivated and the switching regulator is off. No transmission or signaling is possible. Note that *Shutdown* is not a *VP-API-II* line state, but rather a device state upon power up and before the start of execution of the *VP-API-II* software.

3.5.2.2 VP_LINE_DISCONNECT

In the `VP_LINE_DISCONNECT` state, the SLIC block outputs are shut off providing a high impedance to the line. This state can be used for denial of service. The switching regulator is active and outputs the programmed SWFV floor voltage. The voice channel is normally deactivated, but can be activated and used with the converter configuration command to monitor the voltages on Tip or Ring for line diagnostics.

3.5.2.3 VP_LINE_STANDBY

The VP_LINE_STANDBY state is used when On-Hook. This state behaves differently based on the FXS line termination type selected in *Configuring VP-API-II for the Le89156,* on page 8.

If the termination type VP_TERM_FXS_GENERIC is selected, the DC feed is active, and hook supervision functions are enabled. The loop feed polarity is controlled by the *VP-API-II*. The high voltage switching regulator only generates the voltage needed to support the DC line voltage defined by the DC feed. The DC feed drives Tip and Ring to the programmed V_{OC}. Voice transmission is disabled to save power.

If the termination type VP_TERM_FXS_LOW_PWR is selected, a special Low Power Standby state is supported to reduce on-hook power consumption to about 70 mW, while still being able to detect off-hook transitions. In this mode, the DC feed is not active and an external voltage is presented to the Ring lead through the resistor RLP. The line voltage is monitored so that any transitions to off-hook state can be detected. Voice transmission is disabled.

3.5.2.4 VP_LINE_OHT

In the VP_LINE_OHT states, the DC feed is activated and voice transmission is enabled. VP_LINE_OHT allows the transmission of Caller ID information. Hook supervision functions are operating. The switching regulator only generates the negative high voltage needed to support the DC line voltage defined by the DC feed. In this way, power dissipation is minimized.

3.5.2.5 VP_LINE_ACTIVE, VP_LINE_TALK

In the VP_LINE_ACTIVE and VP_LINE_TALK states, the DC feed is activated. Voice transmission is enabled in VP_LINE_TALK and disabled in VP_LINE_ACTIVE. VP_LINE_TALK allows the transmission of Caller ID information for Type 2 Caller ID. Hook supervision functions are operating. The switching regulator only generates the negative high voltage needed to support the DC line voltage defined by the DC feed. In this way, power dissipation is minimized.

3.5.2.6 VP_LINE_RINGING

In the VP_LINE_RINGING state, the voice DAC is used to apply the ringing signal generated from Signal Generator A and the Bias generator to the SLIC block. Internal feedback maintains a low (200 Ω) system output impedance during ringing. The current limit is increased in the *Ringing* state and is programmable via the parameter, ILR. In order to minimize line transients, entry and exit from the VP_LINE_RINGING states are intelligently managed by the Le89156. When ringing is requested by the user, the corresponding signal generators are started but not applied to the subscriber line until the ringing voltage is equal to the on-hook Tip-Ring voltage. This algorithm, known as *Ring Entry*, assures that there is a smooth line transition when entering the VP_LINE_RINGING state. *Ring Entry* is guaranteed to occur within one period of the programmed ringing frequency. *Ring Exit i*s an analogous procedure whereby the ringing signal is not immediately removed from the line after a ring trip or new state request. The ringing signal will persist until its voltage is equal to the required line voltage. The peak ringing voltage that can be generated is equal to |SWRV| - 5 V, in fixed ringing mode. This is automatically calculated by *VP Profile Wizard*.

While in the VP_LINE_RINGING state, the integrated switching regulator may be programmed to behave in one of two ways: tracking or fixed. In tracking mode, the inverting boost or flyback topologies are used in order to generate just enough headroom to support the instantaneous ringing voltages. In fixed regulator mode, the buck-boost topology is used to generate a fixed user-programmed voltage. Note that these three topologies require different external switching power supply components. See *Device Profile,* on page 13 and *Ring Profile,* on page 19 for information on setting the switcher topology.

3.5.2.7 Balanced Ringing

Internal balanced ringing drives the subscriber line with balanced ringing voltage waveforms (see Figure 15 and Figure 16). In the balanced ringing mode, the ringing signal is driven differentially, thus maximizing the ringing signal swing. In this mode, the high-voltage driver appears to the subscriber line as a voltage source with an output impedance of 200 Ω. The maximum ringing signal possible in the balanced mode is 92-V_{PK}, corresponding to the maximum AC + DC voltages.

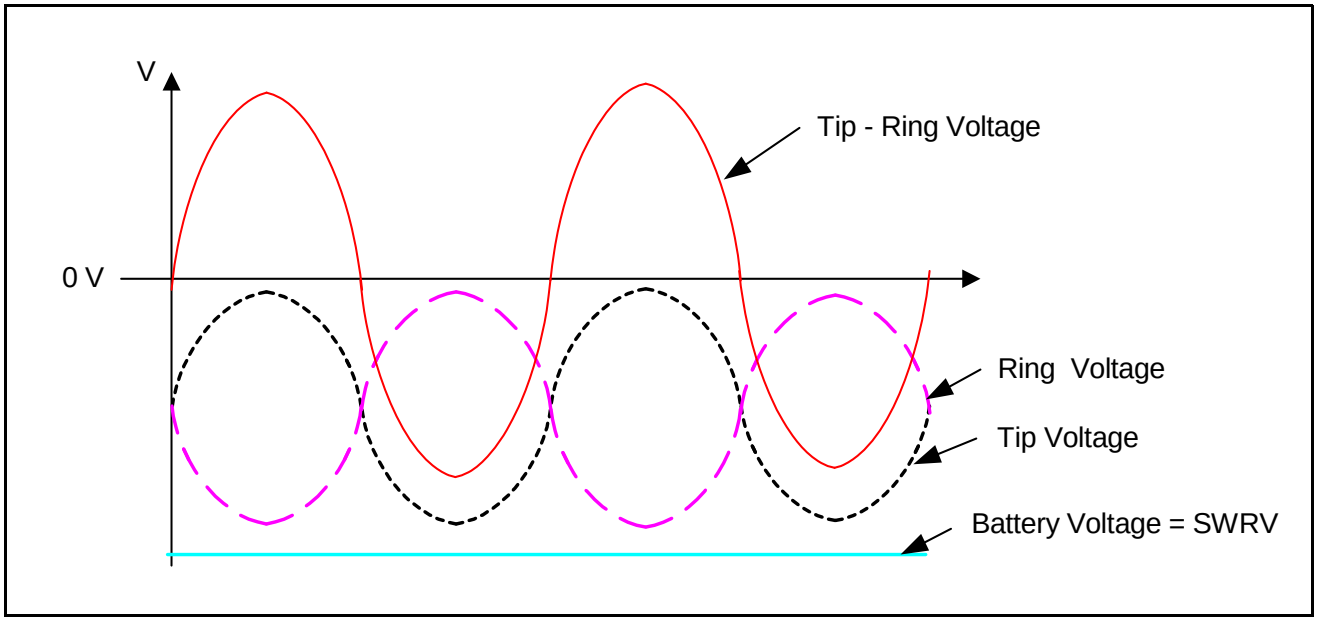


Figure 15 - Balanced Ringing with Fixed Supply

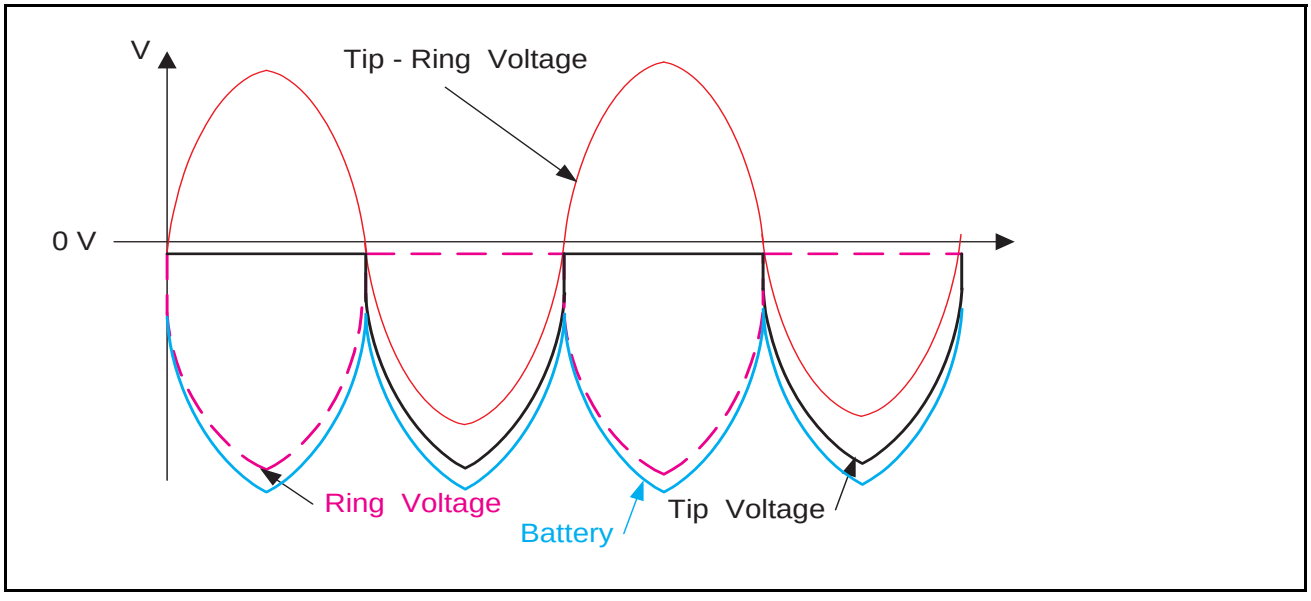


Figure 16 - Balanced Ringing with Tracking Supply

3.6 Supervision Processing

Applications can use either an event generation method for monitoring FXS line status or polling.

Function Name	Description
`VpGetEvent()`	Typically used to implement event driven method to monitor line status. Provides event queue such that a single event reported for each instance function is called (when an event is active).
`VpGetLineStatus()`	Typically used to implement polling method to monitor line status.
	• `VP_INPUT_HOOK` -- Hook Status with mask during dial pulse.
	• `VP_INPUT_RAW_HOOK` -- Real time hook status. Changes during dial pulse
	• `VP_INPUT_GKEY` -- Real time ground key status.

Table 17 - VP-API-II Functions for Line Status Monitoring

3.6.1 Switch Hook Detection

The FXS supervision circuits of the Le89156's SLAC block provides debounced off-hook indications to an external processor via the MPI. The supervision circuit compares a scaled version of the Tip-Ring current to a programmed off-hook threshold, TSH. The output of the comparator is debounced by a programmable debounce timer, DSH. A debounced *Off-Hook* indication generates an interrupt to the user's host processor.

3.6.2 Ring Trip Detection

Ring Trip is the process of sensing a subscriber's off-hook event during *Ringing*. This is accomplished by sensing the rise in loop current which occurs when a phone goes Off-Hook. The Le89156 can detect *Ring Trip* when the ringing signal is purely AC and/or when the ringing signal has a DC bias on it. To do so, the *Ring Trip* algorithm is automatically altered internally by the Le89156 based on the user-programmed parameters.

The *Ring Trip* detector uses the Tip-Ring current as an input. This current is rectified so that AC + DC *Ring Trip* can be detected. The output of the rectified signal is compared to a programmable *Ring Trip* threshold and the output digitally debounced. The output is blanked upon ring entry to avoid false Ring Trips.

The *Ring Trip* detection circuit provides debounced *Ring Trip* indications to an external processor via the MPI. The *Ring Trip* circuit compares a scaled version of the Tip-Ring current to a programmed Ring Trip Threshold (RTTH). The output of the comparator is processed by the *Ring Trip* algorithm on a cycle by cycle basis to provide immunity to false *Ring Trips*. In addition, spending more than 66% of the time in ringing current limit will generate a trip indication. A positive *Ring Trip* occurs if a trip indication is present for two complete ring cycles, and an interrupt can be raised to the host VoIP processor. For AC-only ringing, the signal is half-wave rectified.

The following equations can be used to select new ring trip settings when using different ringing waveforms and different loads. They allow the ratio of the open circuit ringing voltage to the ringing threshold current to vary by +/-20%, which is conservative.

Name	Description
AMPA	Amplitude of signal generator A which is used for ringing
FREQA	Frequency of signal generator A which is used for ringing
BIAS	DC bias for ringing
RTDCAC	Ringing trip based on AC only or battery-backed (DC) ringing
RTTH	Ringing trip threshold in 0.5 mA steps from 0 to 63.5 mA
ILR	Ringing current limit programmed in 2 mA steps. ILR=0 represents 50 mA. ILR = 31 represents 112 mA
HOOK	Interrupt in signalling register indicating a ring trip occurred

Table 18 - Ring Trip Parameters

For AC only ringing, RTDCAC is 1 and the ringing current is half-wave rectified and averaged over a ringing cycle. If this result exceeds the RTTH threshold for two successive cycles, the HOOK bit will be set. This method limits the supported loop length depending on the minimum must not trip ringing impedance (Rmnt in Ohms) and allowing for errors in the applied ringing voltage and trip level. The maximum loop resistance is given by:

$$RLOOP(max) = 0.67 \cdot Rmnt - Rphone - 66 \cdot \Omega$$

$RLOOP_{(max)}$ excludes the DC resistance of the phone (Rphone, typically 430 Ω in the U.S.), and the fuse resistance if DC line sensing is behind the fuse resistors.

For a sinusoidal ringing waveform of VRING RMS volts, and Rmnt impedance, the following ring trip settings should be used:

$$RTTH = \frac{0.54 \cdot VRING}{Rmnt + 200 \cdot \Omega}$$

$$ILR = \frac{1.4 \cdot VRING}{Rmnt + 200 \cdot \Omega}$$

In general for short loop applications, it is recommended to use AC ring trip even in the presence of a DC bias that could allow a DC based ring trip, and the above equations still apply. Note that the ringing source impedance is nominally 200 Ω.

3.7 Analog Reference Circuits

The analog reference circuit generates a reference voltage and reference current for use by the analog portion of the Le89156. The reference current is generated through the external resistor RREF, which is typically 75.0 kΩ. The external capacitor, CREF is typically a 1.0 F or a 4.7 µF ceramic and provides filtering on the reference voltage.

3.8 Subscriber Line Testing

TheLe89156 provides the ability for the user to perform some of the *Telcordia GR-909-CORE / TIA-1063* diagnostic testing for FXS subscriber lines. In Test mode, a variety of input signals can be read from the voice A/D converter. These signals include the switching regulator voltage and the line DC and AC voltages. Two software packages are available from Microsemi for FXS line testing:

3.8.1 VeriVoice Auditor

VeriVoice Auditor is a basic outward line testing package with pass / fail results. It includes the following tests:

- Line Voltage: Checks for hazardous and foreign AC and DC voltages
- Receiver Off-Hook: Checks for longitudinal fault, off-hook resistive fault and receiver off-hook
- Regular REN: Tests the impedance of the line and returns a fail if the Ringer Equivalence Number (REN) is too low or high
- Resistive Fault: Measures three-element resistance
- *GR-909 / TIA-1063:* Performs all of the *Telcordia GR-909-CORE / TIA-1063* outward tests in the correct sequence

3.8.2 VeriVoice Professional

VeriVoice Professional is a more advanced test suite featuring the same outward line tests as *VeriVoice Auditor*, but with measured results (not just pass / fail), enhanced REN test, and the following additional tests:

- Electronic REN: Provides REN Tip to Ring, Tip to ground and Ring to ground based on capacitance
- Capacitance: Measures three element capacitance
- Master Socket: Detects master socket terminations

- Cross Connect: Detects cross connected FXS
- Loopback: Enables receive-to-transmit signal loopback using two different methods
- Read Loop Conditions: Measures voltages between Tip and Ring, Tip to ground, Ring to ground, and V_{BAT} to ground. Also measures metallic and longitudinal line currents in supported states
- Read Battery Conditions: Reads the battery voltages connected to the line circuit
- DC Voltage Self-Test: Verifies that the line circuit has the ability to drive the voltage ranges required for the normal operation of the line circuit
- DC Feed Self-Test Measures the voltage and current across a known test termination using the *DC Profile* that has been programmed
- Ringing Self-Test Verifies ring signal generation, drive capability, and ring trip
- On/Off Hook Self Test Creates on-hook and off-hook conditions on the line using the test termination and verifies that they are properly reported

3.9 Manufacturing Testing

TheLe89156 is supported by the *VeriVoice Manufacturing Test Package (VVMT),* a platform-independent 'C' source code module which facilitates factory testing and calibration of assembled boards with this and other Microsemi voice products.

4.0 Digital Interfaces

4.1 Digital Interfaces Functional Description

The Le89156 interfaces with a PCM backplane and can be controlled over a serial MPI interface. It supports most required PCM clock frequencies from 1.024 MHz to 8.192 MHz, plus three general purpose I/O pins, one of which may be used to drive a relay.

Voice data is interfaced via a PCM highway with time slot assignment capability and control information is communicated over the Microprocessor Interface (MPI). The PCM/MPI interface is flexible and allows a wide range of DCLK (MPI data clock) and PCLK (PCM data clock) frequencies. PCM/MPI interface also allows use of the INT interrupt pin to signal pending interrupts to the external controller.

4.2 Digital Interfaces Features

- PCM and MPI interfaces
  - Selectable PCM clock (PCLK) frequencies: 1.024 MHz, 1.536 MHz, 2.048 MHz, 3.072 MHz, 4.096 MHz, 6.144 MHz, and 8.192 MHz
  - PCM Frame Sync (FS) frequency is set at 8 kHz
- Internal relay driver
  - 3 V, up to 150 mW nominal operating power. Note that an external catch diode is required to protect against inductive kick-back
- Three general purpose I/O pins

4.3 PCM/MPI Interface and Time Slot Assigner (PCM)

The PCM/MPI Interface and Time Slot Assigner (PCM) is a synchronized serial mode of communication between the system and the Le89156 device. In PCM mode, data can be transmitted/received on a serial PCM highway. This highway uses Frame Synch (FS) and PCLK as reference.

Data is transmitted out of the DXA pin and received on the DRA pin. The Le89156 device transmits/receives single 8-bit time slot (µ-law/A-law) compressed voice data or two contiguous time slot 16-bit two's complement linear voice data. The PCLK is a data clock supplied to the device that determines the rate at which the data is shifted in/out of the PCM ports. The FS pulse identifies the beginning of a transmit/receive frame and all time slots are referenced to it. For the Le89156 device, the frequency of the FS signal is 8 kHz. In Wideband mode, two evenly spaced sets of time slots are exchanged in each frame. The PCLK frequency can be a number of fixed frequencies as defined by the *VP-API-II*. Please refer to *Profile Wizard - Device Profile Configuration,* on page 13 for an example setting of the Transmit and Receive Clock Slots, PCM Transmit Edge, and PCLK Frequency.

The *VP-API-II* allows the time slots to be offset to eliminate any clock skew in the system. The Transmit Clock Slot and Receive Clock Slot fields are each three bits wide to offset the time slot assignment by 0 to 7 PCLK periods. The Transmit and Receive Clock Slot is a global command that is applied at the device level. Thus, for each channel, two time slots must be assigned: one for transmitting voice data and the other for receiving voice data. Figure 17 shows the PCM highway time slot structure.

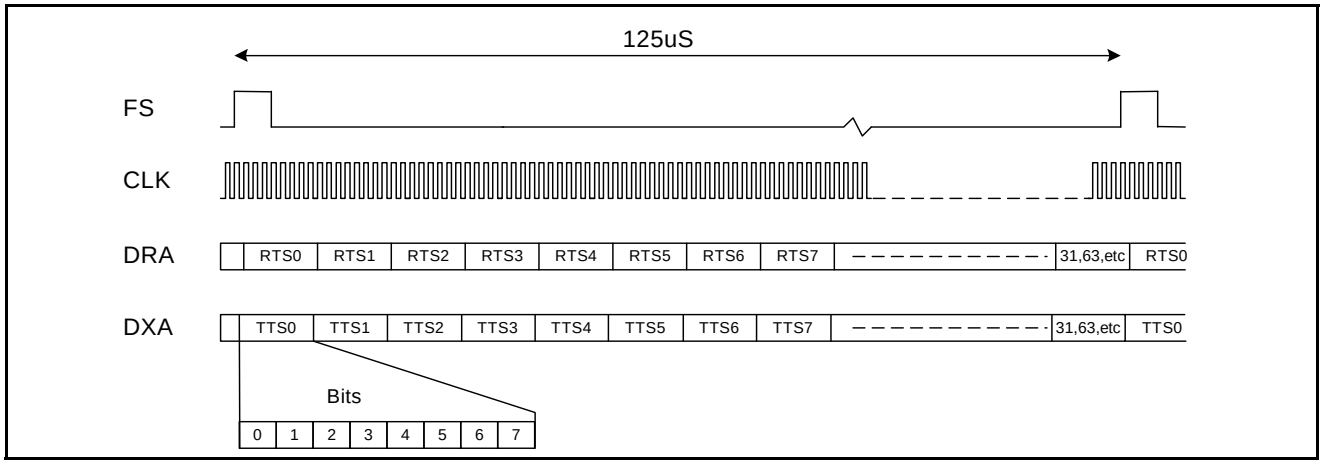


Figure 17 - PCM Highway Structure

4.3.1 Transmit PCM Interface

The Transmit PCM interface receives an 8-bit compressed code (µ-law/A-law) or a 16-bit two's complement linear code from the voice signal processor (compressor). The transmit PCM interface logic (Figure 18) controls the transmission of the data onto the PCM highway through the output port selection circuitry and the time and clock slot control block. The data can be transmitted on either edge of the PCLK, as selected in *VP Profile Wizard* shown in Figure 6, on page 13.

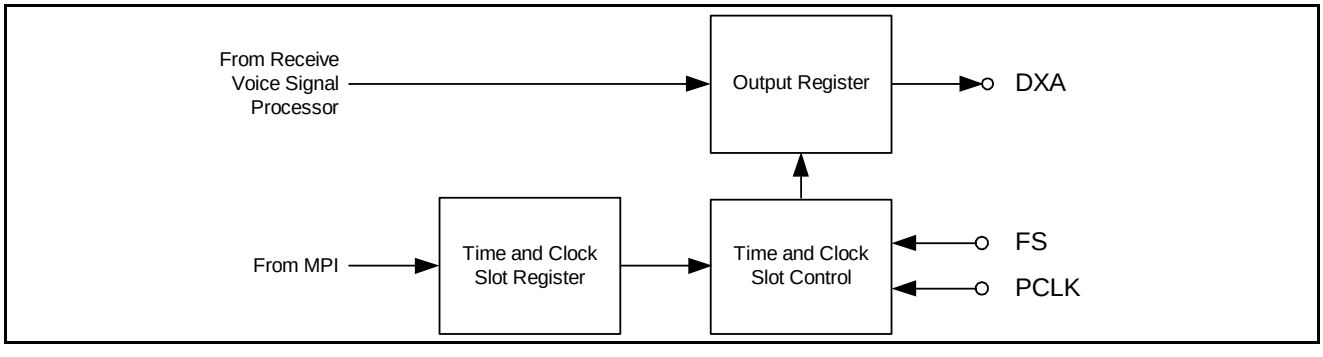


Figure 18 - Transmit PCM Interface

The *VP-API-II* allows the time slot of the selected channel to be programmed. The Transmit Time Slot Register is 7 bits wide and allows up to 128 8-bit time slots in each frame, depending on the value of the PCLK frequency, the encoding scheme, and whether Narrowband or Wideband modes are selected. Refer to Table 19 below for the maximum number of available channels. Please note that linear mode requires two back-to-back time slots to transmit one voice channel. The data is transmitted in bytes with the most significant bit first. Wideband mode requires twice the number of transmit time slots as Narrowband linear mode.

Audio Mode	Encoding	1.024 MHz	2.048 MHz	4.096 MHz	8.192 MHz
Narrowband (8 kHz sampling)	8-bit compressed µ-law/A-law	16	32	64	128
	16-bit linear	8	16	32	64
Wideband (16 kHz sampling)	16-bit linear	4	8	16	32

Table 19 - Maximum Number of Transmit or Receive Channels

4.3.2 Receive PCM Interface

The receive PCM interface logic (see Figure 19) controls the reception of data bytes from the PCM highway. 8-bit compressed (µ-law/A-law) or 16-bit two's complement linear data is formatted and passed to the voice signal processor (expander).

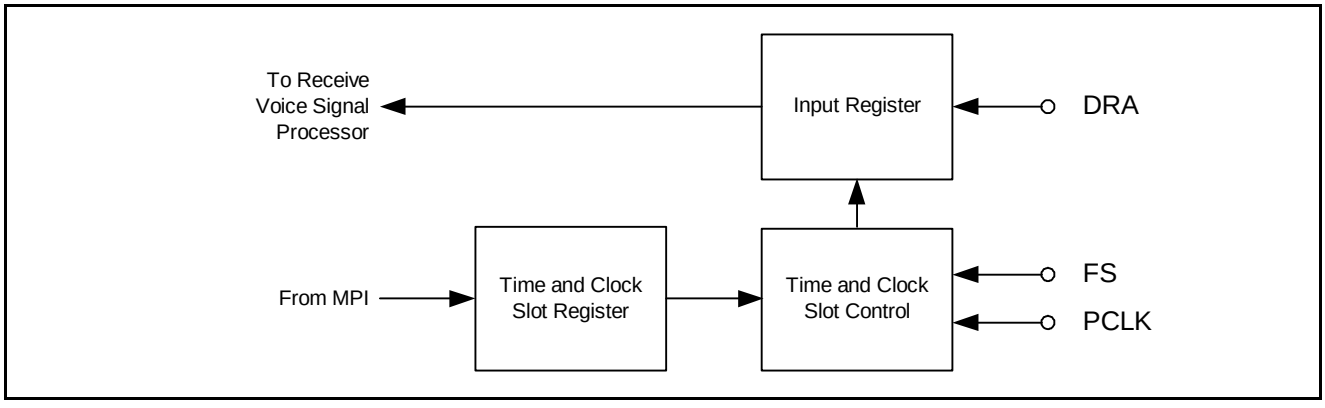


Figure 19 - Receive PCM Interface

The *VP-API-II* allows the time slot of the selected channel to be programmed. The Receive Time Slot Register is 7 bits wide and allows up to 128 8-bit time slots in each frame. Refer to Table 19 above for the maximum number of available channels. Please note that linear mode requires two back-to-back time slots to transmit one voice channel. The data is transmitted in bytes with the most significant bit first. Wideband mode requires twice the numbers of receive time slots as Narrowband linear mode. Please refer to *VP-API-II Functions for Speech Coding, on page 17* for more details about setting the codec mode and transmit and receive time slots.

Figure 20 illustrates data flow on the PCM highway.

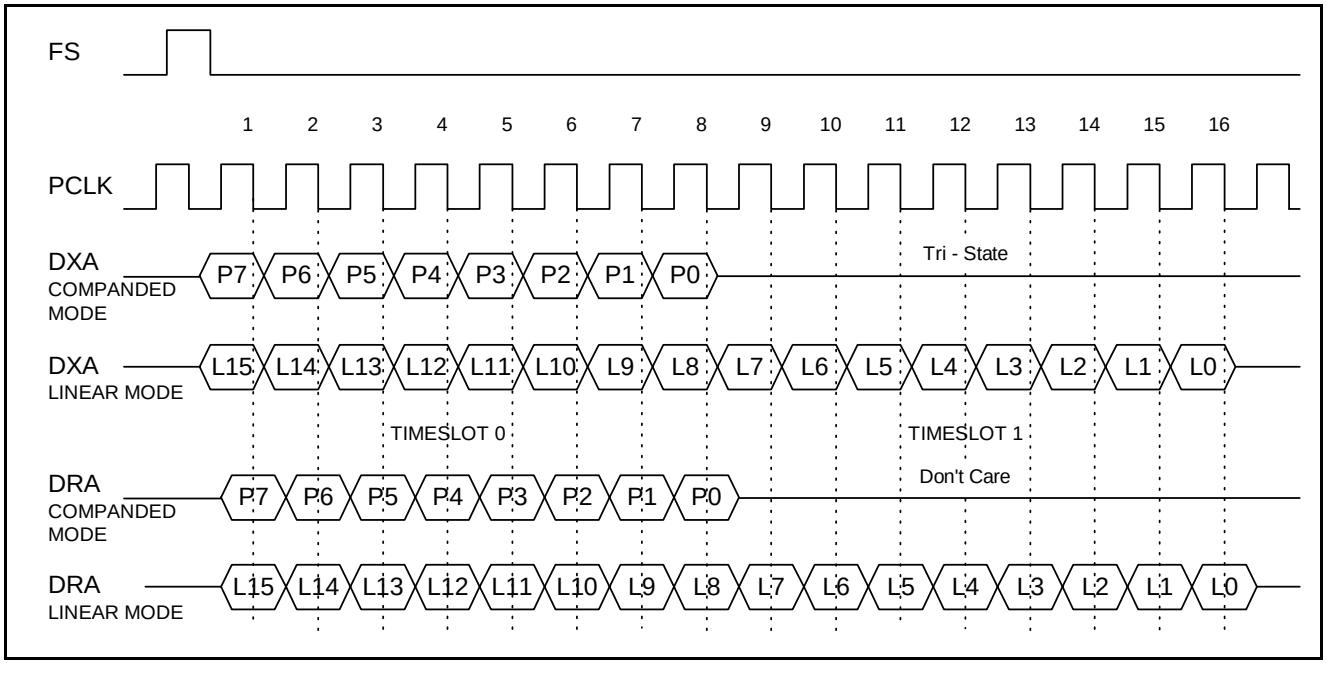


Figure 20 - PCM Data Flow Transmit and Receive Data

4.4 Microprocessor Interface (MPI)

The Microprocessor Interface (MPI) block communicates with external VoIP processors over a synchronous serial interface. It passes user control information to the other blocks, and it passes status information back to the external host.

The MPI physically consists of a serial data input (DIN) serial data output (DOUT), a data clock (DCLK), a chip select ($\overline{CS}$) and an interrupt signal ($\overline{INT}$) (see Figure 21). The serial input consists of 8-bit commands that can be followed with additional bytes of input data, or can be followed by the Le89156 device sending out bytes of data. All data input and output is MSB (D7) first and LSB (D0) last. All data bytes are read or written one at a time, with $\overline{CS}$ going high for at least a minimum off period before the next byte is read or written. Only a single channel should be enabled during read commands. There are two other pins that can be used in conjunction with chip select $\overline{CS}$ to qualify the selection for commands. The CSEN and CSMODE pins can be used as additional qualifiers to permit a host controller to select more than one SLAC device with only one chip select and another GPIO.

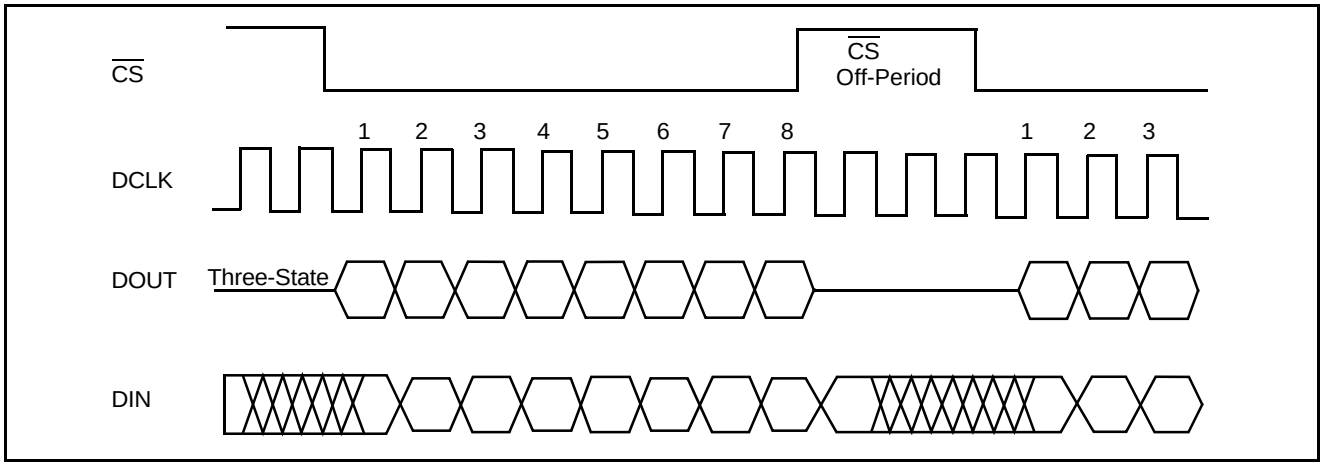


Figure 21 - Microprocessor Interface Timing

All commands that require additional input data to the device must have the input data as the next N words written into the device (for example, framed by the next N transitions of $\overline{CS}$). All unused bits must be programmed to 0 to ensure compatibility with future parts. All commands that are followed by output data will cause the device to output data for the next N transitions of $\overline{CS}$ going low. The Le89156 will not accept any commands until all the data has been shifted out. The output values of unused bits are not specified.

An MPI cycle is defined by transitions of $\overline{CS}$ and DCLK. If the $\overline{CS}$ lines are held in the high state between accesses, the DCLK may run continuously with no change to the internal control data. Using this method, the same DCLK can be run to a number of Le89156 devices and the individual $\overline{CS}$ lines will select the appropriate device to access. Between command sequences, DCLK can stay in the high state indefinitely with no loss of internal control information regardless of any transitions on the $\overline{CS}$ lines. Between bytes of a multi byte read or write command sequence, DCLK can also stay in the high state indefinitely. DCLK can stay in the low state indefinitely with no loss of internal control information, provided the $\overline{CS}$ line remains at a high level. If the system controller has a single bi-directional serial data pin, the DOUT pin of the Le89156 device can be connected to its DIN pin.

If a low period of $\overline{CS}$ contains less than 8 positive DCLK transitions, it is ignored. If it contains 8 to 15 positive transitions, only the last 8 transitions matter. If it contains 16 or more positive transitions, a hardware reset in the part occurs. If the chip is in the middle of a read sequence when $\overline{CS}$ goes low, data will be present at the DOUT pin even if DCLK has no activity.

The CSEN and CSMODE pins are XORed together and act as an enable to the $\overline{CS}$ signal. See the state table below for the logic. Normal MPI Mode operation is possible with both pins tied high or low. For two-device operation, the first device would have CSMODE grounded and the second device would have CSMODE raised to VCC. To talk to device one in this two device configuration, the controller takes CSEN to ground prior to taking $\overline{CS}$

low. After communicating with device A, $\overline{CS}$ is high, and at that time CSEN can be raised to VCC to enable communication with device B. When $\overline{CS}$ goes low, device B receives the command and device A ignores it. The advantage of this special mode is that the CSEN signal can be a slow signal, while CS must be intimately timed with the Start and Stop of DCLK. This special mode is compatible with many processors and DSPs made by Texas Instruments®.

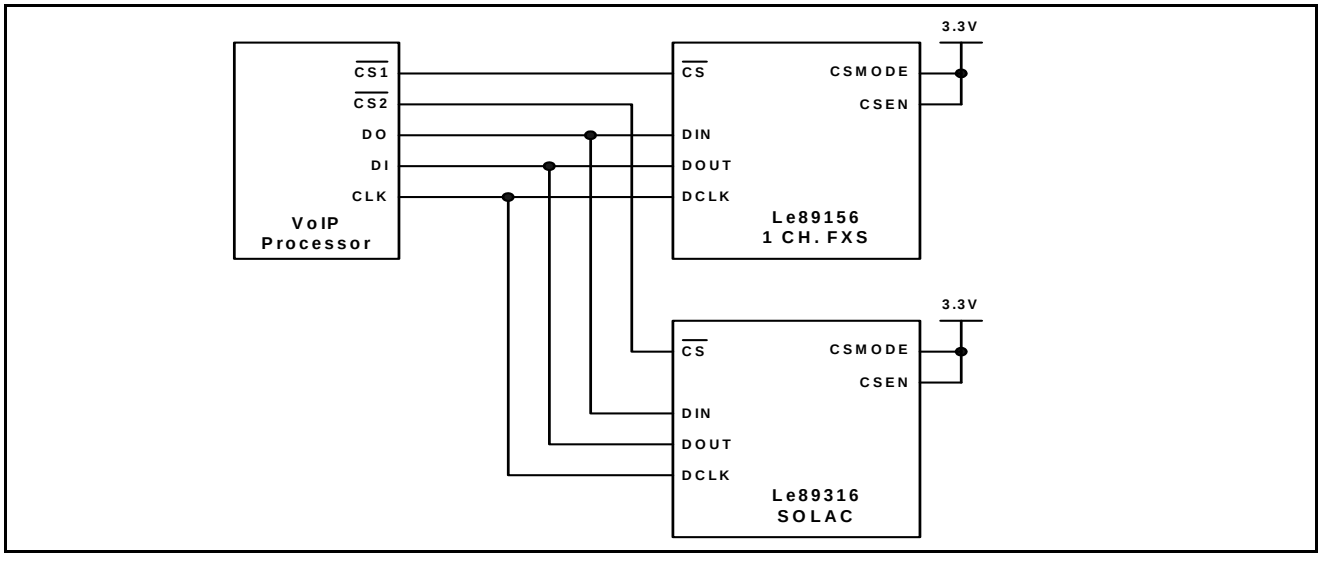


Figure 22 - Normal MPI Mode Device Connection

CSEN	CSMODE	CS	Action	MPI
0	0	0	Chip accepts or outputs data on DIN/DOUT using DCLK	Normal MPI action
0	1	0	Chip ignores DIN/DOUT during DCLK	No MPI action
1	0	0	Chip ignores DIN/DOUT during DCLK	No MPI action
1	1	0	Chip accepts or outputs data on DIN/DOUT using DCLK	Normal MPI action
X	X	1	Chip ignores DIN/DOUT during DCLK	No MPI action

Table 20 - Normal MPI Mode Truth Table

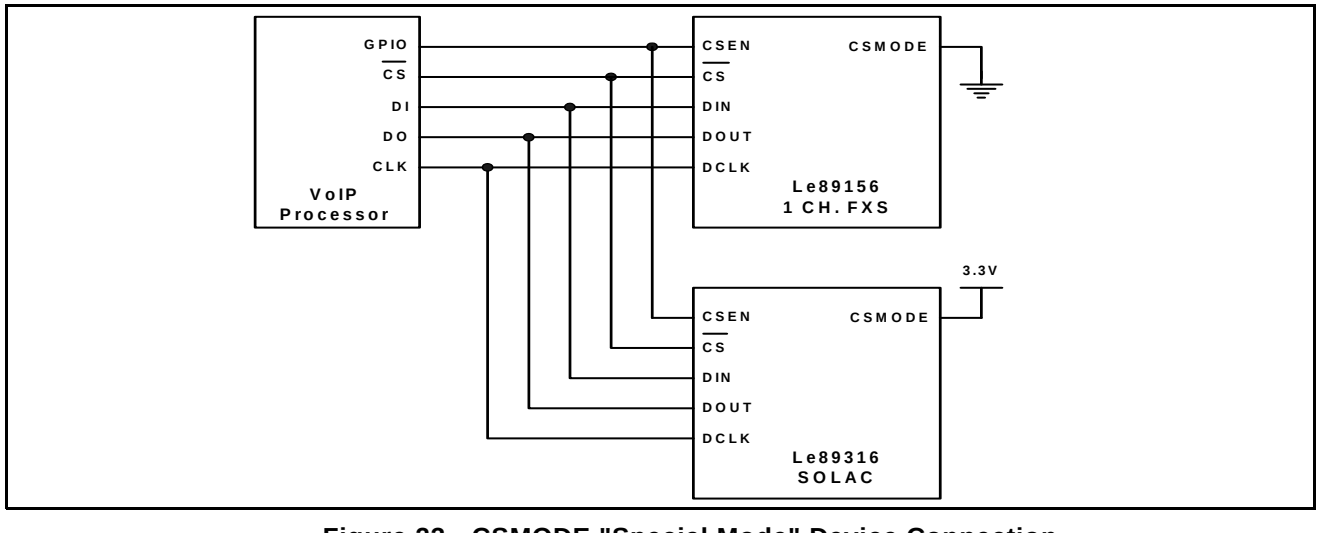


Figure 23 - CSMODE "Special Mode" Device Connection

4.5 Interrupt Servicing

The Le89156 device has a well-defined interrupt structure. Interrupts are caused only when a status bit is unmasked and the status bit is subsequently set or toggles (depending on the interrupt). The interrupts can also be masked by the software.

4.6 Input / Output Block

This block controls general-purpose pins that can be configured by the user as inputs, outputs, or relay drivers. Three CMOS-compatible I/O pins (I/O1, I/O2, and I/O4) are provided for the device. I/O1 can act as a standard digital input, CMOS output, or can be configured as a 3 V relay driver (an external protection diode is required). I/O2 is a standard digital I/O pins that can also generate interrupts when configured as input, while I/O4 is a standard digital I/O pin. All I/O pins are accessed through the *VP-API-II*.

Function Name	Description
`VpSetOption()`	`VP_DEVICE_OPTION_ID_DEVICE_IO` - Used to configure pins individually as input or output. The *`directionPins_31_0`* parameter is used to set pin as input (0) or output (1). The bit in *`directionPins_31_0`* corresponding to I/O is (I/O1 = 0x1, I/O2 = 0x2, and I/O4= 0x8). Other bits in *`directionPins_31_0`* are ignored. Configuring output type done by setting corresponding bit location in *`outputTypePins_31_0`* with **`VP_OUTPUT_DRIVEN_PIN`** (driven). Note that when writing a '1' to a driven pin results in voltage being present on the corresponding I/O pin.
`VpGetOption()`	`VP_DEVICE_OPTION_ID_DEVICE_IO` - Retrieves current I/O pin configuration. When calling `VpGetOption()`, an event (Response Category, Event ID `VP_LINE_EVID_RD_OPTION`) is generated and must be processed by the host application. Host application then calls `VpGetResults()` with pointer to structure of type `VpOptionDeviceIoType` that is filled in by *VP-API-II* with current I/O configuration data.

Table 21 - VP-API-II Functions for Configuring I/O Lines

Function Name	Description
`VpDeviceIoAccess()`	Parameter *`accessMask_31_0`* provides bit field access to the I/O pins as (I/01 = 0x01, I/02 = 0x02, and I/O4=0x8). Access is by 'OR' combination, so *`accessMask_31_0`* = 0x0F provides access to all lines simultaneously. Parameter accessType indicates read (`VP_DEVICE_IO_READ`) or write (`VP_DEVICE_IO_WRITE`) operation. For write operation, *`deviceIOData_31_0`* is used to set lines to '0' or '1'. Bit mask is same as *`accessMask_31_0`* (I/O1 is set to value in *`deviceIOData_31_0`* location 0x1, I/O in *`deviceIOData_31_0`* location 0x2, and so on). All other parameters (*`accessMask_63_32`* and *`deviceIOData_63_32`*) are ignored for the Le89156)

Table 22 - VP-API-II Functions for Write/Read I/O Lines

5.0 Electrical Specifications

5.1 Absolute Maximum Ratings

Stresses above those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Ambient temperature, under bias	-40°C < T_A < +85°C
DVDD with respect to DGND	–0.4 V_{DC} to + 4.0 V_{DC}
AVDD with respect to AGND	–0.4 V_{DC} to + 4.0 V_{DC}
AVDD with respect to DVDD	–0.4 V_{DC} to + 0.4 V_{DC}
DGND with respect to AGND	–0.05 V_{DC} to + 0.05 V_{DC}
BGND with respect to AGND	-0.4 V_{DC} to +0.4 V_{DC}
V_{BAT} with respect to BGND	+0.4 V_{DC} to -105 V_{DC}
TIP or RING with respect to BGND (continuous)	V_{BAT} to + 1.0 V_{DC}
TIP or RING with respect to BGND (10 ms, F = 0.1Hz)	V_{BAT} – 5 V_{DC} to + 5.0 V_{DC}
TIP or RING with respect to BGND (1 µs, F = 0.1Hz)	V_{BAT} – 10 V_{DC} to + 8.0 V_{DC}
TIP or RING with respect to BGND (250 ns, F = 0.1Hz)	V_{BAT} – 15 V_{DC} to + 12 V_{DC}
Current from Tip to Ring	± 150 mA
Digital pins with respect to DGND	–0.4 V_{DC} to the smaller of +4.0 V_{DC} or DVDD + 0.4 V_{DC}
I/O1 current sink to DGND	70 mA
Latch up immunity (any pin)	± 100 mA
Maximum power dissipation, Continuous[(1)]: T_A = 85° C	1.7 W
Junction to ambient thermal resistance[(1)]: θ_{JA}	23.5°C/W
Junction to board thermal resistance[(1)]: θ_{JB}	6.6°C/W
Junction to case bottom (exposed pad) thermal resistance[(1)]: $\theta_{JC\ (BOTTOM)}$	3°C/W
Peak Reflow temperature per *IPC/JEDEC J-STD-020*	MSL 3 @ 260°C
ESD immunity (Human Body Model)	*JESD22 Class 1C* compliant

Note:

1. See Thermal Resistance, on page 36

5.1.1 Thermal Resistance

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to a large internal copper plane. Thermal

performance depends on the number of PCB layers and the size of the copper area. Please refer to Microsemi's application note *QFN Package (Document ID#: 080791)* for design and layout guidelines and follow the *Recommended Land Pattern*, on page 67 as closely as possible. Continuous operation above 125ºC may degrade device reliability.

5.1.2 Package Assembly

The 'Green' package devices are assembled with enhanced, environmental and compatible lead- (Pb), halogen-, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer Pb-free board assembly processes. The peak soldering temperature should not exceed 260°C during printed circuit board assembly.

Refer to *IPC/JEDEC J-STD-020* for the recommended solder reflow temperature profile.

5.2 Operating Ranges

Microsemi guarantees the performance of this device over industrial (-40ºC to 85ºC) temperature range by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with the *Telcordia GR-357-CORE Generic Requirements for Assuring the Reliability of Components Used in Telecommunications Equipment.*

5.2.1 Recommended Operating Conditions

Ambient temperature	-40°C < T_A < +85°C
Ambient relative humidity	15 to 85%
AGND	0 V_{DC}
DGND with respect to AGND	±10 mV_{DC}
BGND with respect to AGND	±100 mV_{DC}
AVDD with respect to AGND	+3.3 V_{DC} ± 5%
DVDD with respect to AVDD	±50 mV_{DC}
V_{BAT} with respect to BGND	-15 V_{DC} to -100 V_{DC}
Digital pins	DGND to 3.465 V_{DC}
Analog pins	AGND – 0.3 V_{DC} to AVDD +0.3 V_{DC}

6.0 Electrical Characteristics

6.1 Test Conditions

Unless otherwise noted, test conditions are:

- Typical values are for T_A = 25 ºC and nominal supply voltages. Minimum and maximum values are over the temperature and supply voltage ranges shown in *Operating Ranges*, on page 37, except where noted.
- FXS Measurements are based on the test circuit shown in Figure 24
- V_{BAT} = -57 V_{DC} for Idle (On-Hook), On-Hook Transmission (OHT) and OHT with Reverse Polarity line states
- V_{BAT} = -30 V_{DC} for Talk (Off-Hook) line state and the DC feed programmed to I_{LA} = 26 mA, V_{OC} = 48 V_{DC}, V_{AS} = 9 V_{DC}, and ILR = 60 mA
- AC and DC load resistance R_L = 600 Ω
- 0 dBm0 = 0 dBm (600 Ω) = 0.7746 V_{RMS}. Digital gains GX0 and GR0 to achieve 0 dBr relative levels are:
  - GX0 = +6.797 dB (7A20h) A-law or linear and GX0 = +6.737 dB (2A20h) µ-law to set A/D transmit gain to 0 dB
  - GR0 = -1.793 dB (6AA0h) A-law or linear and GR0 = -1.720 dB (3AA0h) µ-law to set D/A receive gain to 0 dB
- Default (unity) gain in X, R, DRL, AX and AR blocks
- Default coefficients in DISN, Z- and B-Filters
- Ringing tests were conducted with ILR = 58 mA and RTTH =23 mA_{AC}
  - C1 programmed ringing 71 V_{PK} (50 V_{RMS}) 0 V_{DC} offset and 1 REN (7000 Ω + 8-µF) load
  - C2 programmed ringing 71 V_{PK} (50 V_{RMS}) 0 V_{DC} offset and 3 REN (2333 Ω + 24-µF) load
  - C3 programmed ringing 71 V_{PK} (50 V_{RMS}) 0 V_{DC} offset and 5 REN (1386 Ω + 40-µF) load

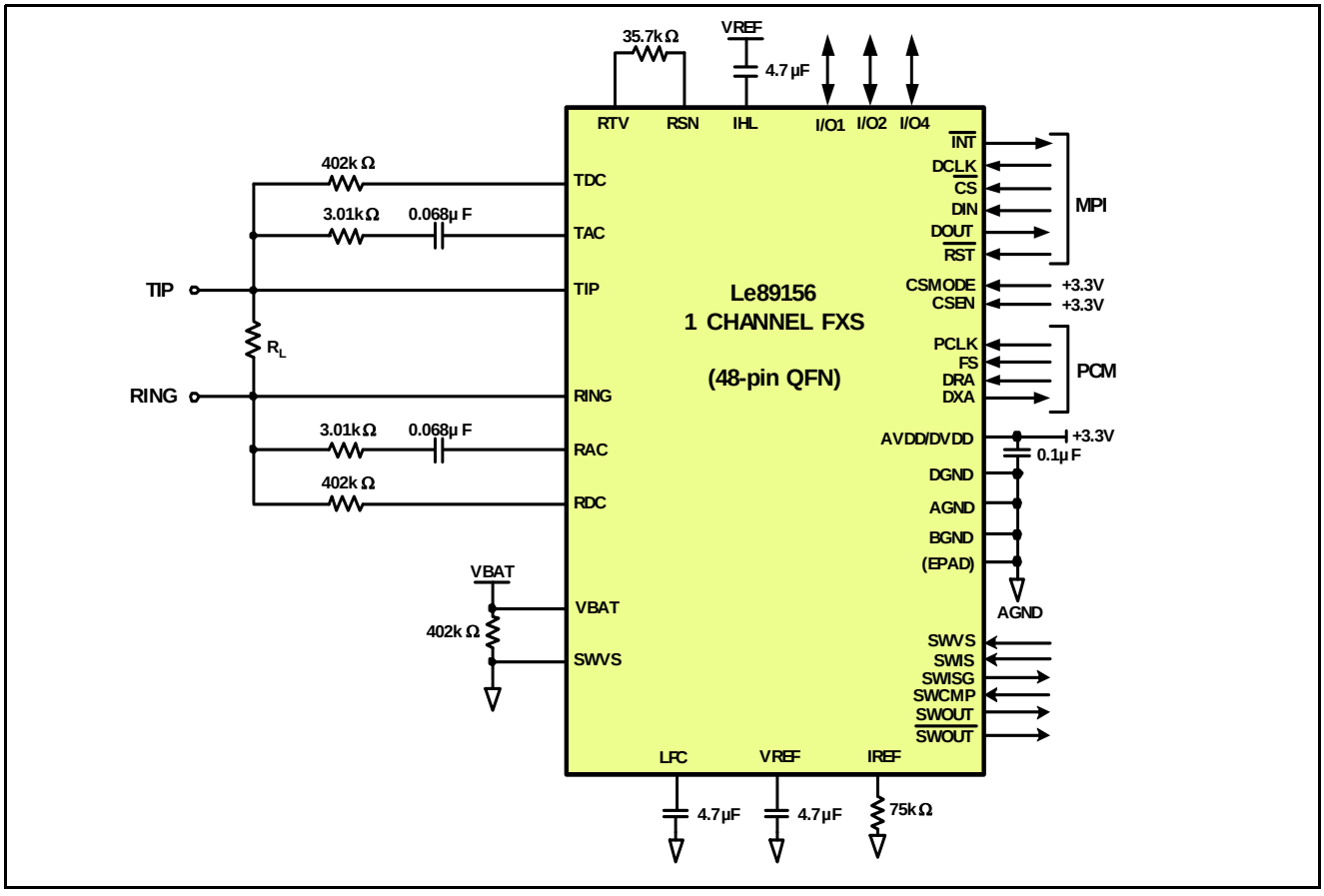


Figure 24 - Le89156 Test Circuit

6.2 Supply Currents and Power Dissipation

- External switcher circuit as shown in Figure 43, on page 60 with input voltage V_{SW} = 12 V_{DC}
- Device or package power does not include power delivered to the load
- Fuse resistors for power tests are R_F = 25 Ω

Operational State	Condition	I_{DD} mA (Note 1)	I_{BAT} mA (Note 2)	Package Power mW (Note 3)	I_{VSW} mA (Note 4)	Note
		Typ	Typ	Typ	Typ	
Shutdown	Power-up condition with the switcher off	6	0.0	20	0.2	*5.*
Disconnect	Switcher on, but no DC feed to the line. V_{BAT} = -25 V_{DC}	7	0.1	26	1	
Low Power Idle	Switcher on with limited feed to the line	12	0.1	46	3	
Idle		14	0.8	86	8	
	On-Hook Transmission	25	1.8	190	17	
Active (normal or reverse polarity)	Off-Hook, 300 Ω	24	28	453	61	
	Off-Hook, 600 Ω	24	28	468	80	
Ringing	C1	28	9	290	65	*6., 7.*
	C2	28	21	442	146	*6., 7.*
	C3	28	31	583	220	*6., 7.*

Notes:

1. *I_{DD} supply current is the sum of I_{AVDD} and I_{DVDD} for the package. Wideband mode increases I_{DD} by 10mA at the device level*
2. *Measured output of switching regulator feeding into VBAT pin*
3. *Package power dissipation does not include power delivered to the load*
4. *12V supply current feeding the external switching regulator*
5. *Shutdown is a device state and not a VP-API-II line state*
6. *Full tracking ringing regulation mode was used for these measurements*
7. *Ringing signal must be cadenced to produce an average power that can be handled by the Le89156 package*

6.3 DC Characteristics

Symbol	Parameter Descriptions	Min.	Typ.	Max.	Unit	Note
V_{IL}	Digital Input Low voltage			0.8	V	
V_{IH}	Digital Input High voltage	2.0				
I_{IL}	Digital Input leakage current	–7		+7	µA	*1.*
I_{AIL}	Analog input leakage current	–1		+1		
V_{HYS}	Digital Input hysteresis	0.16	0.25	0.34	V	*1.*
V_{OL}	Digital Output Low voltage I/O1 (I_{OL} = 50 mA) I/O2, I/O4 (I_{OL} = 4 mA) I/O2, I/O4 (I_{OL} = 8 mA) Other digital outputs (I_{OL} = 2 mA)			 0.8 0.4 0.8 0.4	V	*2.*
V_{OH}	Digital Output High voltage I/O1,I/O2,and I/O4 (I_{OH} = 4 mA) I/O1,I/O2,and I/O4 (I_{OH} = 8 mA) Other digital outputs (I_{OH} = 400 µA)	 V_{CCD} – 0.4 V V_{CCD} – 0.8 V 2.4			V	*2.*
I_{OL}	Digital Output leakage current (High-Z state) 0 < V < DVDD	 –7		 +7	µA	
V_{REF}	VREF output open circuit voltage	1.43	1.5	1.57	V	
C_{IREF}	IREF pin maximum load capacitance			20	pF	*1.*
C_I	Digital Input capacitance			10		*1.*
C_O	Digital Output capacitance			10		*1.*
$PSRR_1$	AVDD, DVDD Power supply rejection ratio (1.02 kHz, 100 mV_{RMS}, either path, GX = GR = 0 dB)	30			dB	

Notes:

1. Guaranteed by characterization or correlation to other tests. Typical values are not tested in production.

2. The GPIO outputs are resistive for less than a 0.8 V_{DC} drop. Total current must not exceed absolute maximum ratings.

6.3.1 DC Feed and Signaling

Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Note
On-Hook Characteristics						
Open Circuit Tip to Ring Voltage		-52	-48	-44	V_{DC}	*2.*
Ringing Voltage Range				92	V_{PK}	*1.*
Programmed Ringing Voltage Accuracy	R_L = open	-7		+7	%	*1.*
V_{AB}, Ringing DC offsets	R_L = open, V_{RING} = 0 V	-7		+7	V	*1.*
Ringing harmonic distortion	Case C1		3	5	%	
Ringing current limit accuracy	R_L = 300 Ω	-10		10	%	*1.*
Ringing source impedance			200		Ω	*1.*
AC Ring Trip accuracy	EGBIAS = 0	-15		+15	%	*3.*
Ring Trip delay	Periods of ringing	1		3	cycles	*1.*
Ring Frequency Range		15		67	Hz	
Maximum Ring Drive	65 V_{RMS}			5.0	REN	
Off-Hook Characteristics						
Tip to Ring Line Current, I_{LA}	2 Kft. 26 AWG local loop	20		40	mA	
I_{LA}, Loop-current accuracy, Active state	I_L in constant-current region	-10		+10	%	*2.*
TDC, RDC input offset current		3.3	3.7	4.1	µA	*1.*
Switch-hook accuracy		-15%-2mA		+15%+2mA	mA	
Switch-hook threshold range	1 mA steps	8		14	mA	

Notes:

1. *This parameter is guaranteed by characterization or correlation to other tests. Typical values not tested in production.*
2. *Calibration is required to achieve these values.*
3. *If the ringing current in the loop is near the current limit more than 50% of the time, a Ring Trip will occur regardless of the average current.*

6.4 Switching Regulator Controller

Description	Test Conditions	Min.	Typ.	Max.	Unit	Note
Switcher Input Voltage VSWIB (Inverting Boost Mode)		4.4	12	15	V_{DC}	
Switcher Input Voltage VSWFL (Flyback Mode)		4.75	12	16	V_{DC}	
SWIS shutdown threshold	Referenced to SWIG		79		mV	
SWIS input bias current		-10		10	µA	
SWIS shutdown delay	V_{SWIS} > 100 mV	12		88	ns	*1., 2.*
SWCMP output current		-200		200	µA	
SWCMP operating range		0.4		2.6	V	
SWVS to SWCMP gain		0.4		40	V/nA	
SWVS to SWCMP bandwidth		100			kHz	
SWVS input offset current		3.3	3.7	4.1	µA	*3.*
LFC output impedance			80		kΩ	
SWRV output voltage accuracy	SWRV = -95 V_{DC}	-4		+4	V_{DC}	*1.*

Notes:

1. *Guaranteed by characterization or correlation to other tests. Typical values are not tested in production*
2. *Time from SWIS exceeding threshold difference from SWISG to SWOUT passing though VDD/2*
3. *Analog input pad leakage can add to this value- see specification under DC Characteristics. Requires ABV calibration*

6.5 External Signal Sense Accuracy

Description	Test Conditions	Min.	Typ.	Max.	Unit	Note
Metallic AC coupled voltage		- 4		+ 4	%	*1.*
Switcher input at SWVS	V_{BAT} = -95 V_{DC}	- 5%		+ 5%	V	*1., 2.*
Tip voltage to ground	-26 V_{DC} applied between Tip/Ring and Ground	- 6%		+ 6%	V	*1.,2.*
Ring voltage to ground		- 6%		+ 6%	V	
Metallic DC line voltage	-1.5 V_{DC} applied to Tip and -21.5 V_{DC} applied to Ring	- 7%		+ 7%	V	
Metallic loop current	V_{BAT} = -30 V_{DC} , ± 130 µA applied at IM	-1.5 mA - 5%		1.5 mA + 5%	mA	*1.*
Total longitudinal current		-2.5 mA - 5%		2.5 mA + 5%	mA	*1.*
Voice DAC (Full loopback)	0 dBm reference signal	-1.0		+1.0	dB	

Notes:

1. *The % limits are defined as the% of the actual voltage on Tip / Ring. The offset and percentage errors are independent and combine as RMS errors.*
2. *This is measured in production by first calibrating offset voltage and applying the listed test voltages on Tip and/or Ring. Accurately measuring smaller voltages requires care in offset calibration.*

6.6 Transmission Characteristics - Narrowband Codec Mode

Description	Test Conditions	Min.	Typ.	Max.	Unit	Note
TAC - RAC overload level	Active state, GX = AX = 0 dB	3.4			V_{PK}	*1. 2.*
Transmit level, A/D	0 dBm, 1014 Hz		0		dBm0	
Receive level, D/A	0 dBm0, 1014 Hz		0		dBm	
Gain accuracy, D/A	0 dBm0, 1014 Hz	–0.5		+0.5	dB	
Gain accuracy, A/D	0 dBm0, 1014 Hz	–0.5		+0.5		
Attenuation distortion	300 to 3000 Hz	–0.25		+0.25		*1.*
Single frequency distortion				–46		*3., 6.*
Second harmonic distortion, D-A	GR = 0 dB, linear mode			–55		*6.*
Idle channel noise V_{TIP} - V_{RING} DXA, Digital out	 DRA, Digital input = 0, A-law, 0 dBr DRA, Digital input = 0, µ-law, 0 dBr V_{TIP} - V_{RING} = 0 V_{AC}, A-law, 0 dBr V_{TIP} - V_{RING} = 0 V_{AC}, µ-law, 0 dBr			 –71 19 –65 19	 dBm0p dBrnC0 dBm0p dBrnC0	 *4.* *1., 4.* *4.* *1., 4.*
End-to-end absolute group delay	B = Z = 0; X = R = 1, C/L = 0			678	µs	*1., 5.*
Two-wire return loss	200 to 3400 Hz	26	30		dB	*1.*
Longitudinal to Metallic balance TIP - RING or DXA	200 to 3400 Hz	46	58		dB	*1.*
DRA to Longitudinal signal generation	300 to 3400 Hz	40				*1.*
Longitudinal current capability, TIP or RING	Active state	8.5			mA_{RMS}	*1.*
Longitudinal impedance at TIP or RING	0 to 100 Hz		100		Ω/pin	*1.*

Notes:

1. *This parameter is guaranteed by characterization or correlation to other tests. Typical values not tested in production.*
2. *Overload level is defined when THD = 1%.*
3. *0 dBm0 input signal, 300 Hz to 3400 Hz measurement at any other frequency, 300 Hz to 3400 Hz.*
4. *No single frequency component in the range above 3800 Hz may exceed a level of –55 dBm0.*
5. *The End-to-End Group Delay is the absolute group delay of the echo path with the B Filter turned off.*
6. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*

6.7 Transmission Characteristics - Wideband Codec Mode

Description	Test Conditions	Min.	Typ.	Max.	Unit	Note
TAC - RAC overload level	Active state GX = AX = 0 dB	3.4			V_{PK}	*1., 2.*
Transmit level, A/D	0 dBm, 1014 Hz		0		dBm0	
Receive level, D/A	0 dBm0, 1014 Hz		0		dBm	
Gain accuracy, D/A or A/D	0 dBm0, 1014 Hz	–0.5		+0.5	dB	
Attenuation distortion	100 Hz to 6.0 kHz	–0.25		+0.25		*1.*
Single frequency distortion	50 Hz to 7.0 kHz			–46		*3., 6.*
Second harmonic distortion, D-A	GR = 0 dB, linear mode			–55		*6.*
Idle channel noise, 7 kHz Flat V_{TIP} - V_{RING} DXA, Digital out	 DRA, Digital input = 0, A-law, 0 dBr DRA, Digital input = 0, µ-law, 0 dBr V_{TIP} - V_{RING} = 0 V_{AC}, A-law, 0 dBr V_{TIP} - V_{RING} = 0 V_{AC}, µ-law, 0 dBr			 -67 23 -67 23	 dBm0p dBrnC0 dBm0p dBrnC0	 *1., 4.* *1., 4.* *1., 4.* *1., 4.*
End-to-end absolute group delay	B = Z = 0; X = R = 1, C/L = 0			678	µs	*1., 5.*
Two-wire return loss	50 to 7000 Hz	20	30		dB	*1.*
Longitudinal to Metallic balance TIP - RING or DXA	50 to 7000 Hz	46	58		dB	*1.*
DRA to Longitudinal signal generation	300 to 7000 Hz	40				*1.*
Longitudinal current capability, TIP or RING	Active state	8.5			mA_{RMS}	*1.*
Longitudinal impedance at TIP or RING	0 to 100 Hz		100		Ω/pin	*1.*

Notes:

1. *This parameter is guaranteed by characterization or correlation to other tests. Typical values not tested in production.*
2. *Overload level is defined when THD = 1%.*
3. *0 dBm0 input signal, 50 Hz to 7000 Hz measurement at any other frequency, 50 Hz to 7000 Hz.*
4. *No single frequency component in the range above 7600 Hz may exceed a level of –55 dBm0.*
5. *The End-to-End Group Delay is the absolute group delay of the echo path with the B Filter turned off.*
6. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*

6.8 Typical Transmission Plots

The following graphs illustrate typical *VE890* FXS transmission graphs using a *W&G PCM-4* tester. The measured responses for 600 ohms and *ETSI TBR21/ ES 203 021* complex AC impedances both with normal headroom are shown and are compared to the corresponding *ITU Q.552* templates.

6.8.1 Return Loss

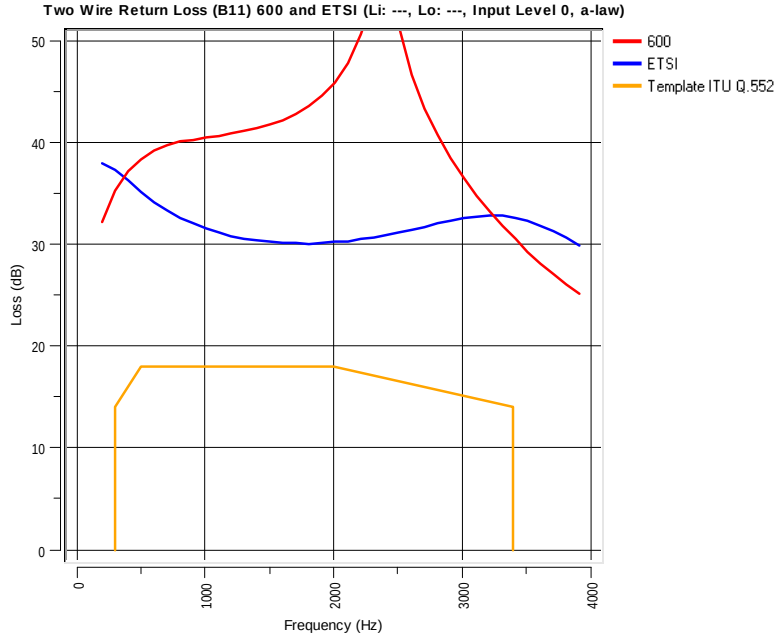


Figure 25 - Two-Wire Return Loss

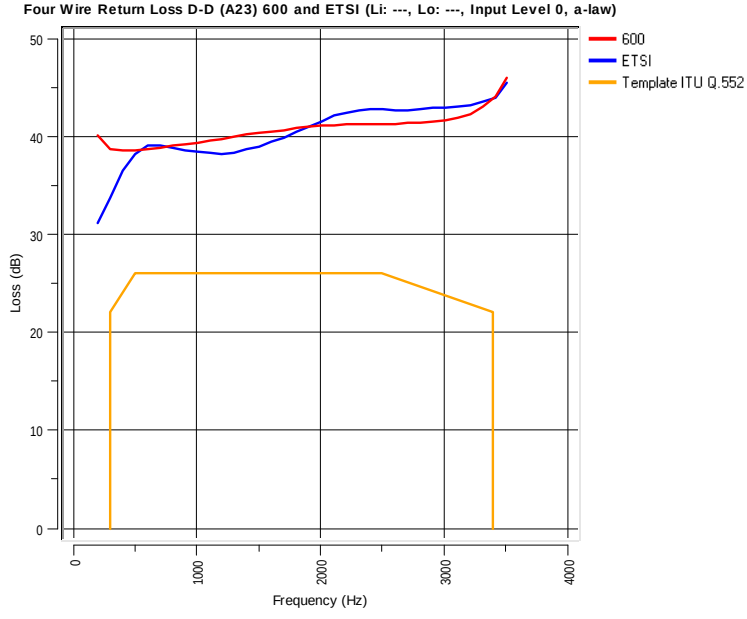


Figure 26 - Four-Wire Return Loss

6.8.2 Attenuation Distortion and Gain

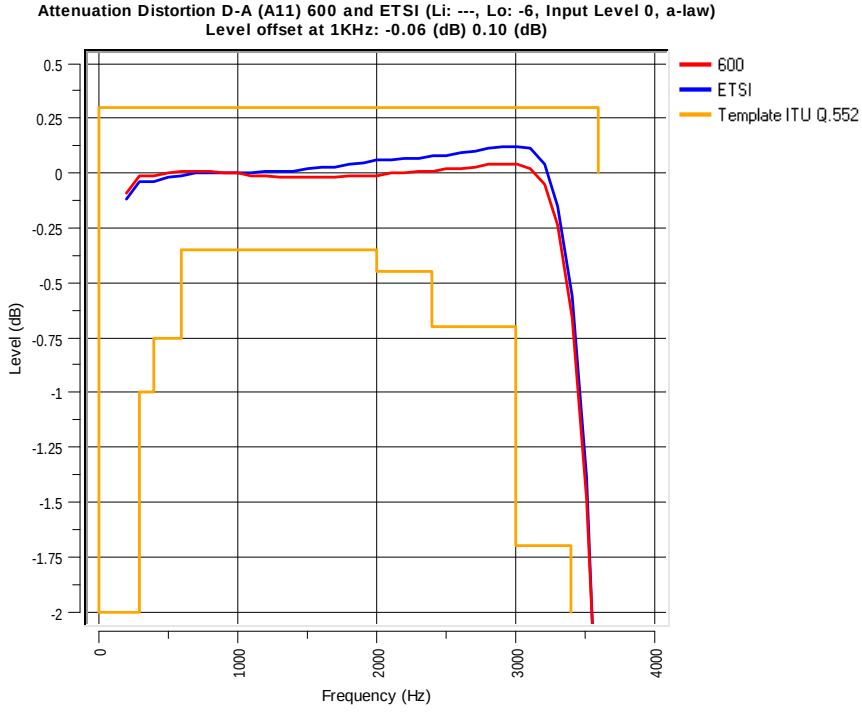


Figure 27 - Receive Path Attenuation Distortion

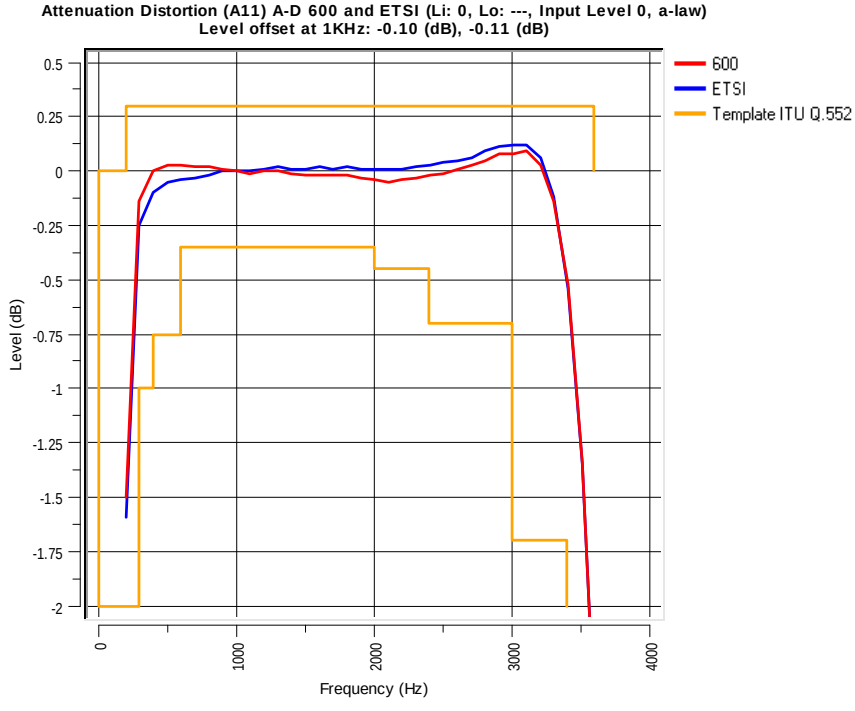


Figure 28 - Transmit Path Attenuation Distortion

6.8.3 Gain Tracking and Noise

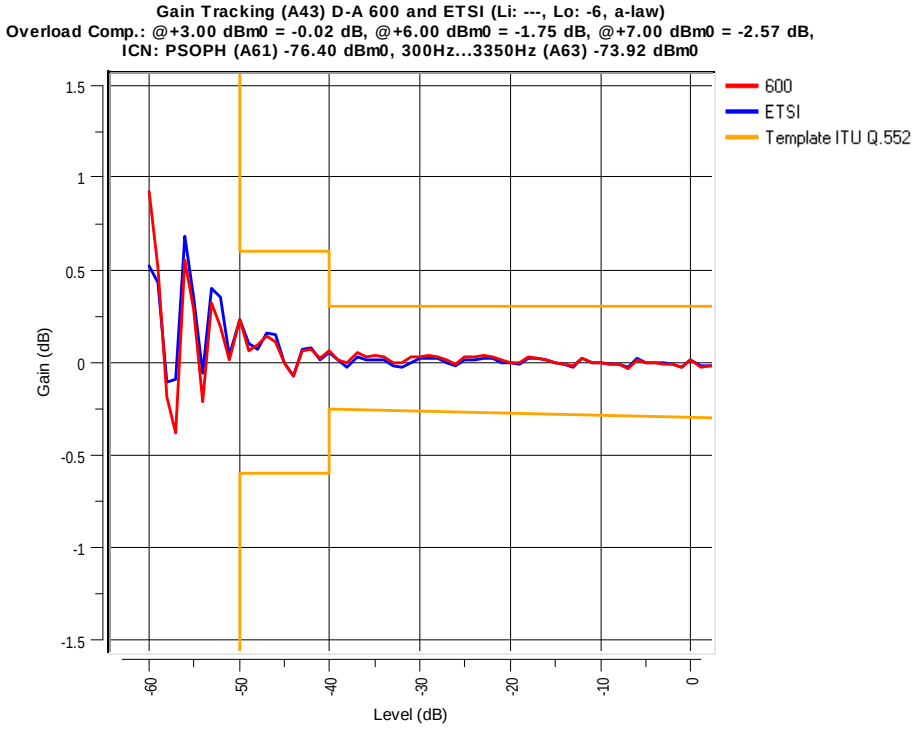


Figure 29 - Receive Path Gain Tracking

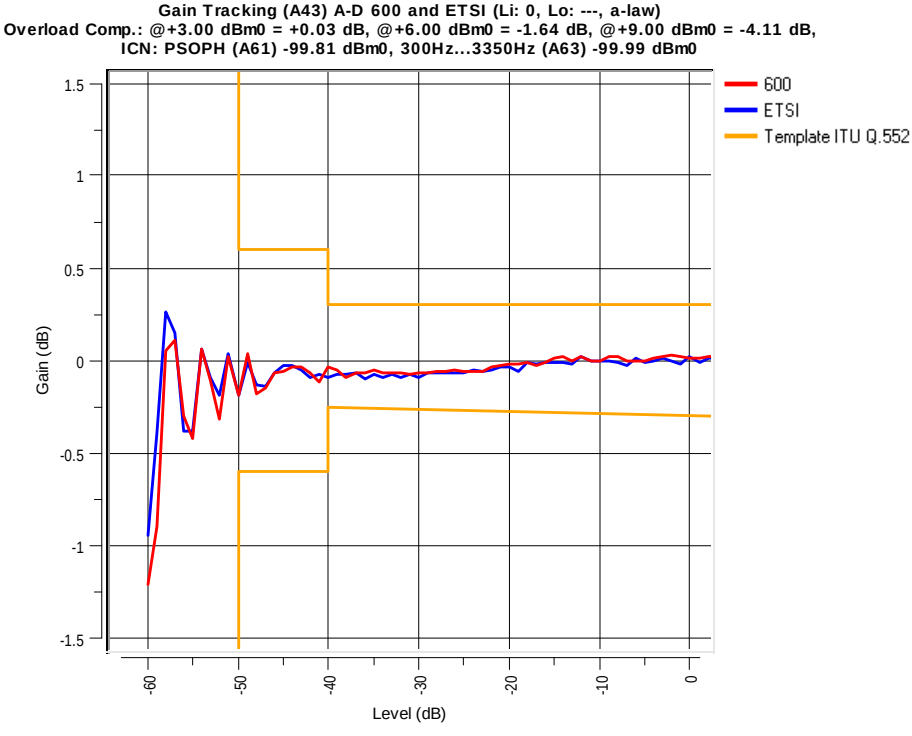


Figure 30 - Transmit Path Gain Tracking

6.8.4 Total Distortion and Harmonic Distortion

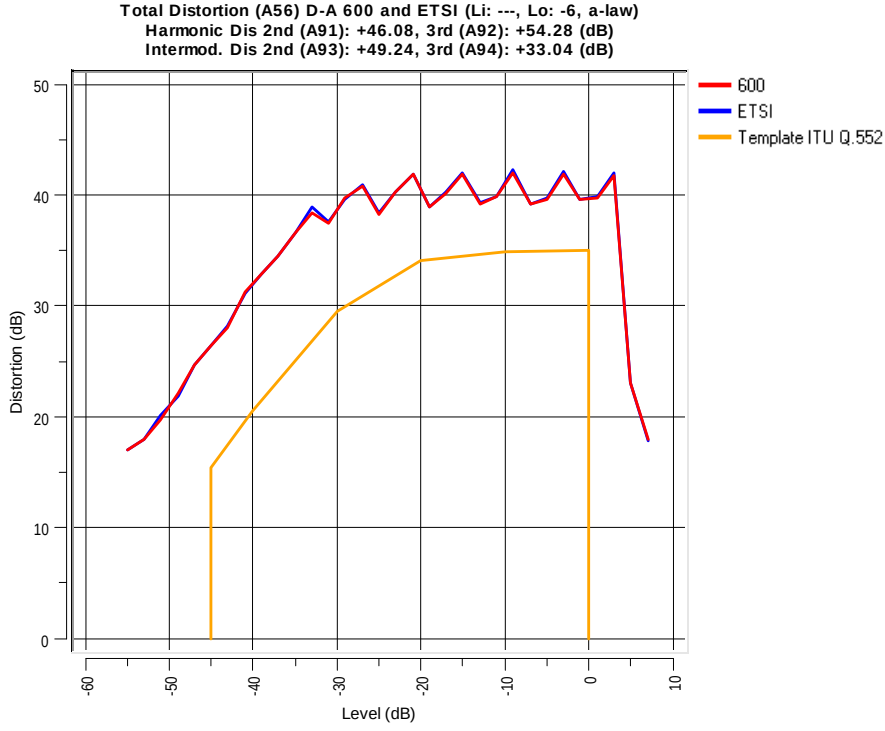


Figure 31 - Receive Path Total Distortion

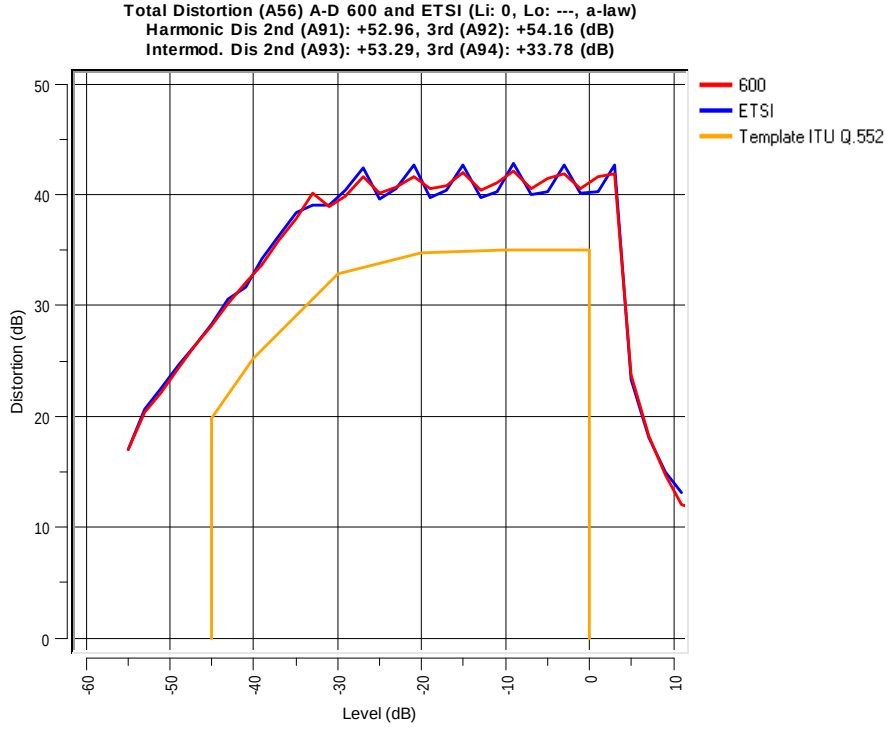


Figure 32 - Transmit Path Total Distortion

6.8.5 Longitudinal Balance

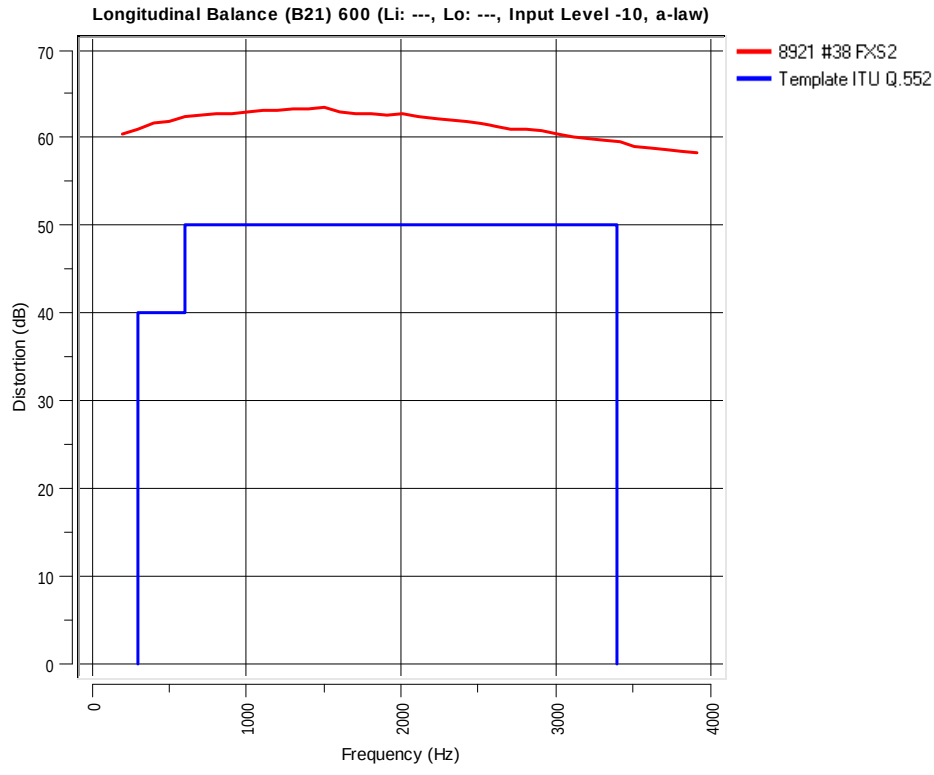


Figure 33 - Longitudinal Balance

7.0 Switching Characteristics and Waveforms

The following are the switching characteristics over operating range, unless otherwise noted. Minimum and maximum values are valid for all digital outputs with a 115 pF load. (See Figure 34 and Figure 35 for the MPI timing diagrams).

7.1 Microprocessor Interface

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
1	t_{DCY}	Data clock period	122			ns	
2	t_{DCH}	Data clock HIGH pulse width	48				
3	t_{DCL}	Data clock LOW pulse width	48				
4	t_{DCR}	Rise time of clock			25		
5	t_{DCF}	Fall time of clock			25		
6	t_{ICSS}	Chip select setup time, Input mode	30		t_{DCY} –10		
7	t_{ICSH}	Chip select hold time, Input mode	0		t_{DCH} –20		
8	t_{ICSL}	Chip select pulse width, Input mode		$8t_{DCY}$			
9	t_{ICSO}	Chip select off time, Input mode	2500				
10	t_{IDS}	Input data setup time	25				
11	t_{IDH}	Input data hold time	20				
12	t_{OLH}	I/O1, I/O2, I/O4 output latch valid			2500		
13	t_{OCSS}	Chip select setup time, Output mode	30		t_{DCY} –10		
14	t_{OCSH}	Chip select hold time, Output mode	0		t_{DCH} –20		
15	t_{OCSL}	Chip select pulse width, Output mode		$8t_{DCY}$			
16	t_{OCSO}	Chip select off time, Output mode	2500				
17	t_{ODD}	Output data turn on delay			50		*1.*
18	t_{ODH}	Output data hold time	3				*2.*
19	t_{ODOF}	Output data turn off delay			50		
20	t_{ODC}	Output data valid			50		
–	t_{RST}	Reset pulse width	50			µs	

Notes:

1. The first data bit is enabled on the falling edge of $\overline{CS}$ or the falling edge of DCLK, whichever occurs last.

2. This parameter is guaranteed by characterization or correlation to other tests.Typical values not tested in production.

)

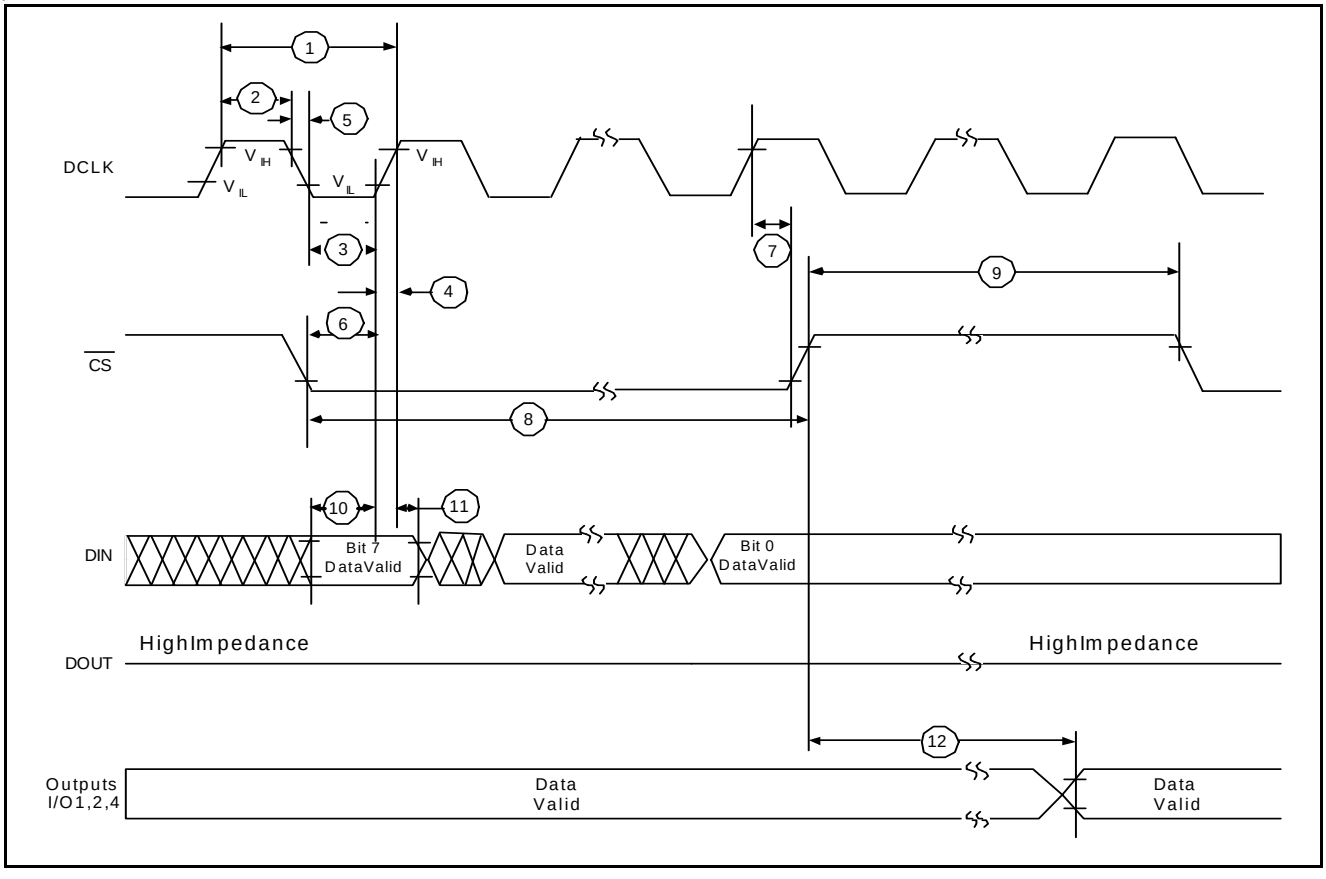


Figure 34 - Microprocessor Interface (Input Mode)

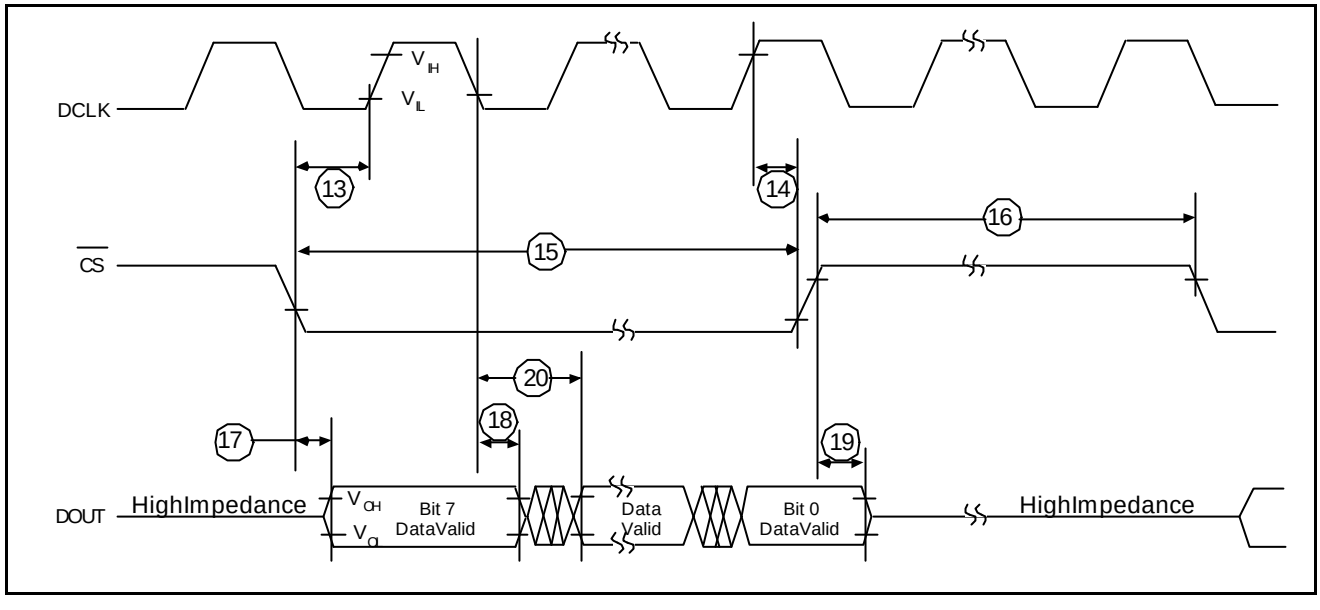


Figure 35 - Microprocessor Interface (Output Mode)

7.2 PCM Interface

PCLK shall not exceed 8.192 MHz.
(See Figure 36 through Figure 39 for the PCM interface timing diagrams.)

No.	Symbol	Parameter	Min.	Typ	Max	Unit	Note
21	t_{PCY}	PCM Clock (PCLK) period	122		977	ns	*1.*
22	t_{PCH}	PCLK HIGH pulse width	48				
23	t_{PCL}	PCLK LOW pulse width	48				
24	t_{PCR}	PCLK rise time			15		
25	t_{PCF}	PCLK fall time			15		
26	t_{FSS}	FS setup time	25		t_{PCY}–30		
27	t_{FSH}	FS hold time	50				
–	t_{FSTN}	Allowed PCLK or FS jitter time - Narrowband	–50		50		*1.*
–	t_{FSTW}	Allowed PCLK or FS jitter time - Wideband	–25		25		*1.*
28	t_{DXD}	PCM data output delay			70		
29	t_{DXH}	PCM data output hold time	5				
30	t_{DXZ}	PCM data output delay to high Z	10		70		
31	t_{DRS}	PCM data input setup time	25				
32	t_{DRH}	PCM data input hold time	5				
–	t_{FSL}	FS LOW pulse width	1.5 t_{PCY}				*2.*

Notes:

1. *The PCLK frequency must be an integer multiple of the frame sync (FS) frequency. Frame sync is expected to be an accurate 8 kHz pulse train. The actual PCLK rate depends on the CSEL bit setting in the Chip Configuration register. The minimum frequency is 1.024 MHz and the maximum frequency is 8.192 MHz. If PCLK has jitter, care must be taken to ensure that all setup, hold, and pulse width requirements are met*
2. *Applies only when FS is active LOW*

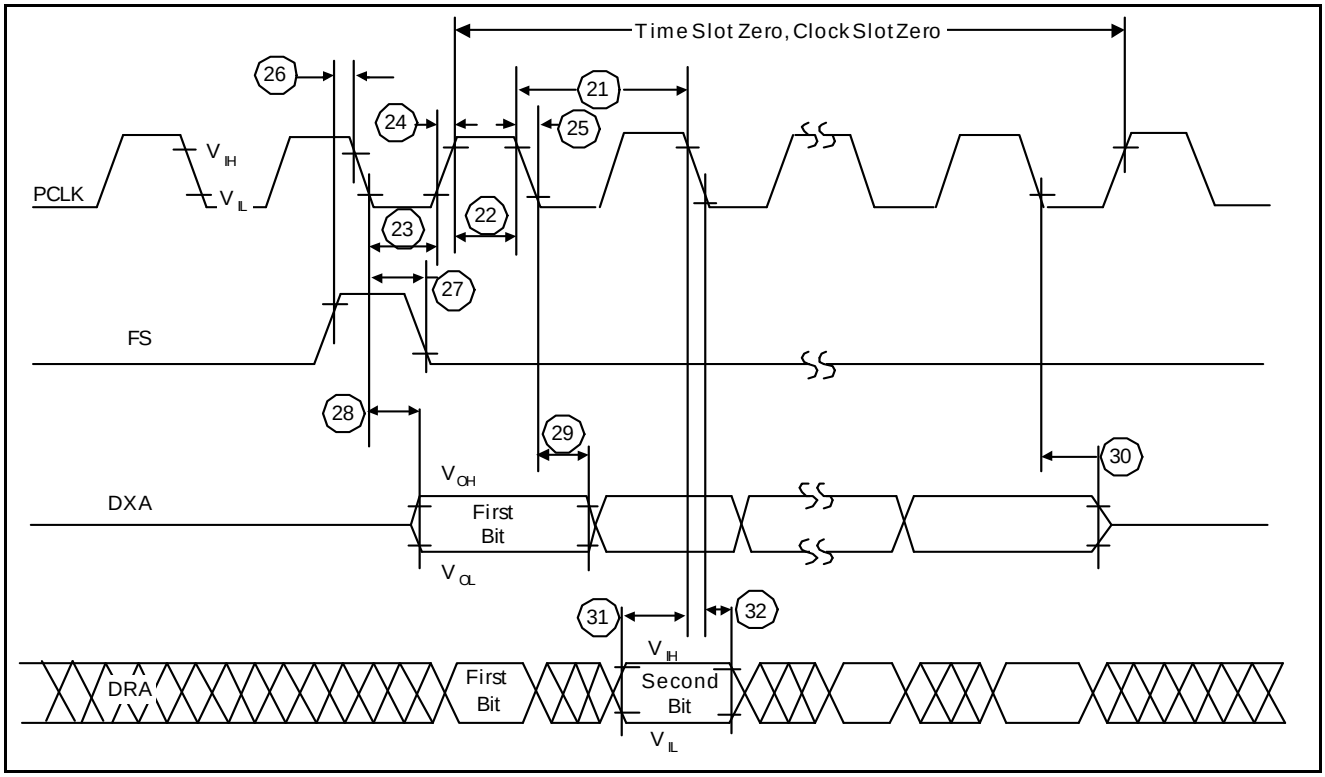


Figure 36 - PCM Highway Timing for XE = 0 (Transmit on Negative PCLK Edge)

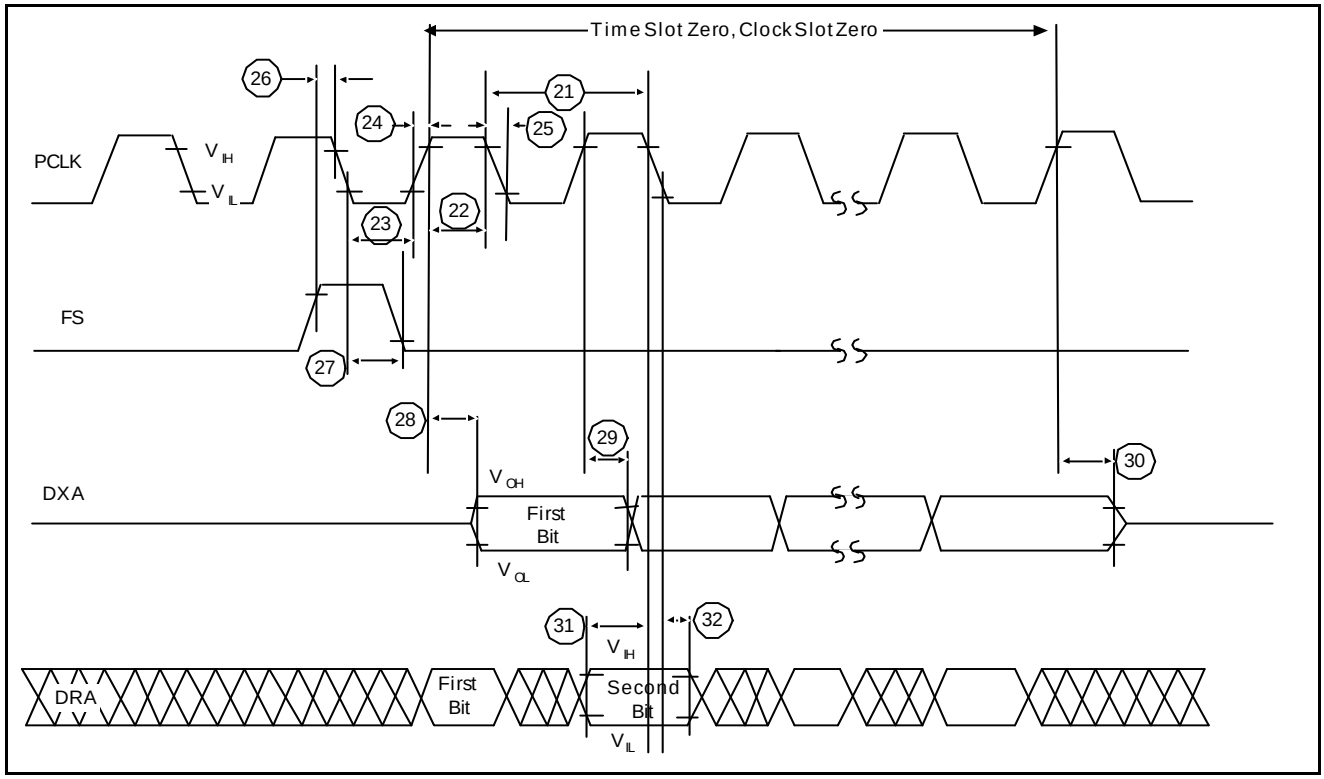


Figure 37 - PCM Highway Timing for XE = 1 (Transmit on Positive PCLK Edge)

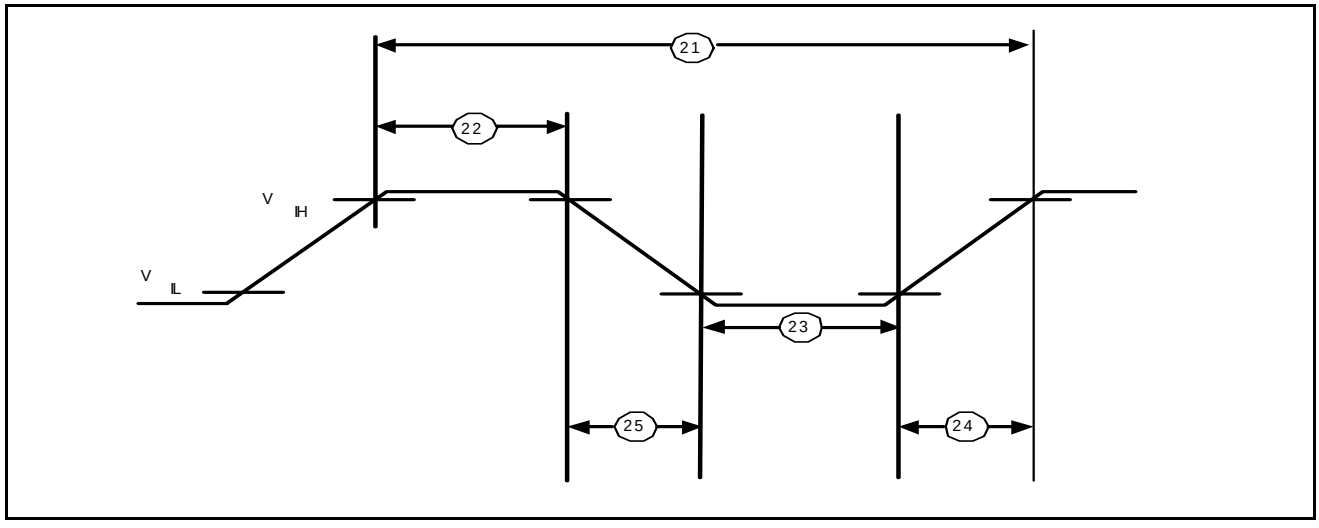


Figure 38 - PCM Clock Timing

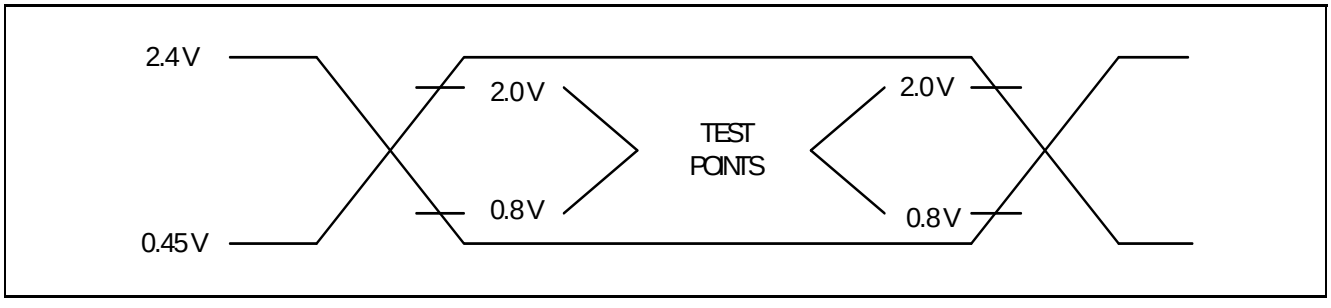


Figure 39 - Input and Output Waveforms for AC Tests

7.3 Switcher Output Timing

(See Figure 40 for the SWOUT, $\overline{SWOUT}$ timing diagram.)

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	Tfall	Output Fall Time		30		ns	*1., 2.*
2	Trise	Output Rise Time		30		ns	*1., 2.*
3LP	TPeriod	Period for Low Power Mode		41.667		µs	*1., 3.*
4LP	Tmax	Max On-Time for Low Power Mode		1.830	1.845	µs	*1., 4.*
3MP	TPeriod	Period for Medium Power Mode		10.417		µs	*1., 4.*
4MP	Tmax	Max On-Time for Medium Power Mode		1.830	1.845	µs	*1., 4.*
3HP	TPeriod	Period for High Power Mode		2.604		µs	*1., 5.*
4HP	Tmax	Max On-Time for High Power Mode		1.830	1.845	µs	*1., 5.*
–	Duty Cycle LP	Duty Cycle Low Power Mode	0		8.8	%	*1., 3.*
–	Duty Cycle MP	Duty Cycle Medium Power Mode	0		17.6	%	*1., 4.*
–	Duty Cycle HP	Duty Cycle High Power Mode	0		70.3	%	*1., 5.*
–		SWISY leading edge blanking period		120		ns	*1.*

Notes:

1. *Guaranteed by characterization or correlation to other tests. Not tested in production.*
2. *Measured with an RC load on SWOUT or $\overline{SWOUT}$ of 330 pF in series with 180 Ω to ground.*
3. *Switching Regulator Control Register is loaded with low power mode 01h flyback mode settings.*
4. *Switching Regulator Control Register is loaded with medium power mode 02h flyback mode settings.*
5. *Switching Regulator Control Register is loaded with high power mode 03h flyback mode settings.*

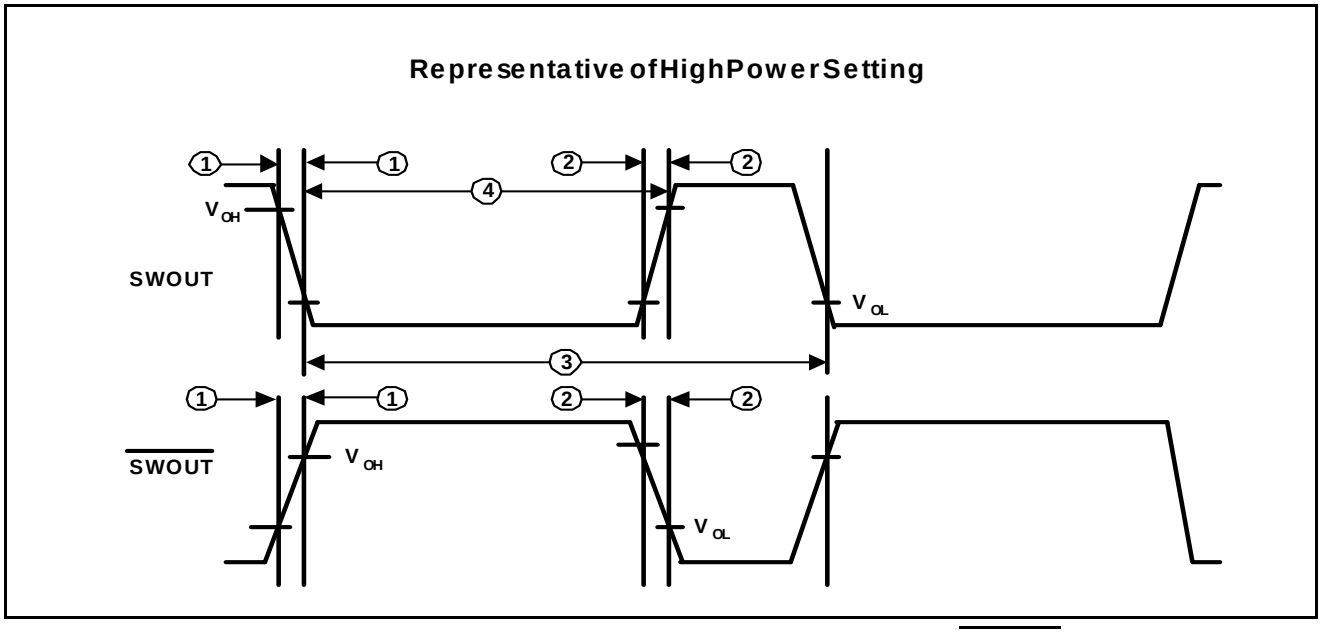


Figure 40 - Switcher Output Waveforms SWOUT, $\overline{SWOUT}$

8.0 Device Pinout

The pins of the Le89156 Single Channel Wideband FXS device are listed and described in this section.

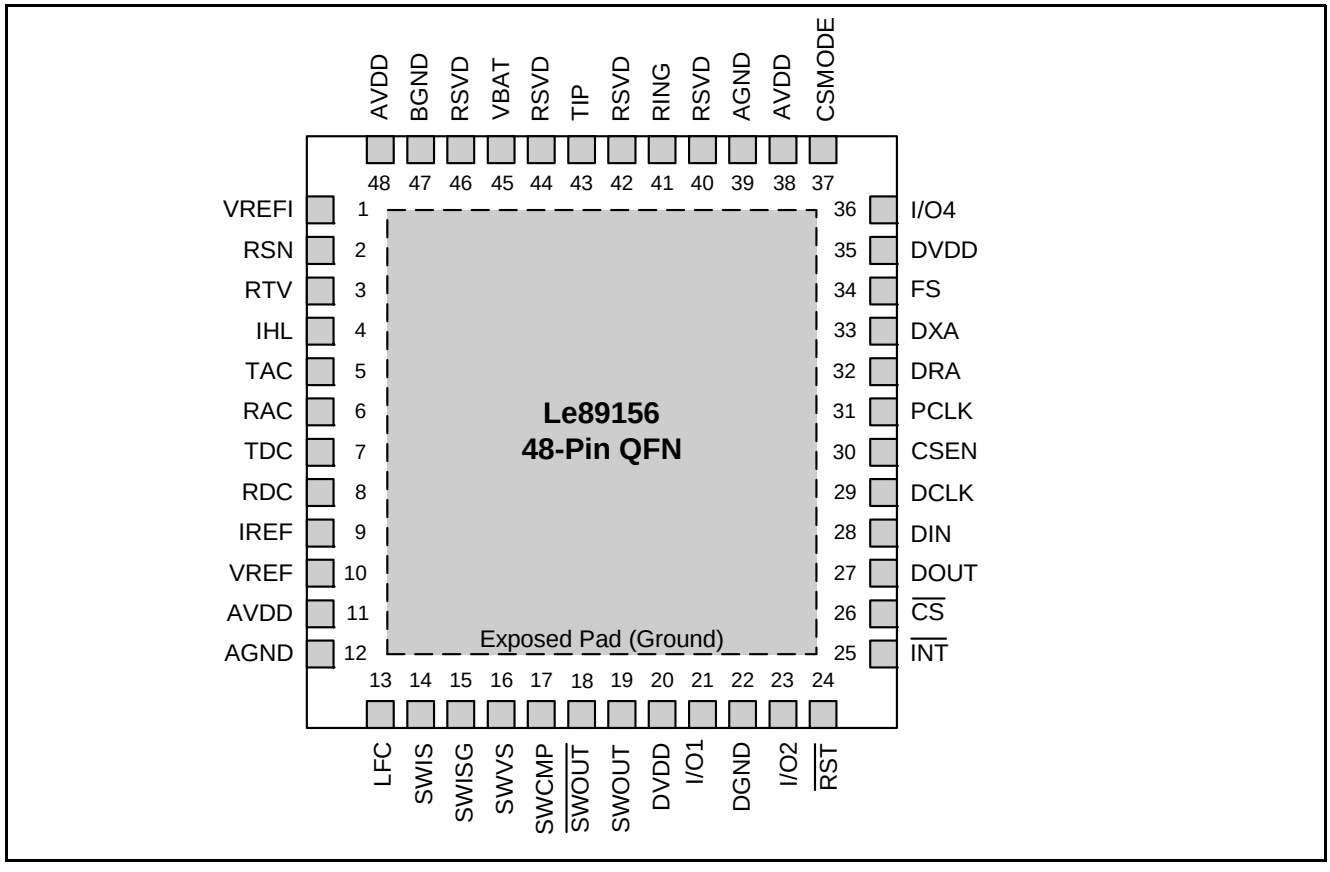


Figure 41 - Le89156 Single Channel Wideband FXS (QFN-48)

Pin	Name	Type	Description
1	VREFI	Input	Analog Voltage Reference Input. Must be connected to VREF (pin 10)
2	RSN	I/O	Receive current summing node
3	RTV	Output	Drive output for two-wire AC impedance scaling resistor
4	IHL	Output	Filters DC feed after capacitor
5	TAC	Input	Tip lead AC sense
6	RAC	Input	Ring lead AC sense
7	TDC	Input	Tip lead DC sense
8	RDC	Input	Ring lead DC sense
9	IREF	Input	Current Reference
10	VREF	Output	Analog Voltage Reference
11	AVDD	Power	Analog 3.3 V supply input
12	AGND	Power	Analog ground return for AVDD
13	LFC	Output	Connection for longitudinal filter capacitor
14	SWIS	Input	Current sense input for switching regulator controller

Table 23 - Le89156 Pin Descriptions

Pin	Name	Type	Description
15	SWISG	Input	Ground reference for switching regulator over current alarm
16	SWVS	Input	Voltage sense for switching regulator controller
17	SWCMP	Output	Compensation connection for switching regulator controller
18	$\overline{\text{SWOUT}}$	Output	Inverted pulse output for gate drive to switching regulator FET
19	SWOUT	Output	Pulse output for gate drive to switching regulator transistor or FET
20	DVDD	Power	Digital 3.3 V supply input
21	I/O1	I/O	General purpose Input/ Output (Can directly drive a 3 V, 150 mW relay; requires an external catch diode across the relay coils)
22	DGND	Power	Digital ground return for DVDD. Connect to AGND
23	I/O2	I/O	General purpose Input/ Output
24	$\overline{\text{RST}}$	Input	Device hardware reset
25	$\overline{\text{INT}}$	Output	Interrupt
26	$\overline{\text{CS}}$	Input	MPI Chip Select
27	DOUT	Output	MPI Data Output
28	DIN	Input	MPI Data Input
29	DCLK	Input	MPI Clock
30	CSEN	Input	Connect to ground for normal mode, used in multiple device mode select
31	PCLK	Input	PCM Clock
32	DRA	Input	PCM Data Receive
33	DXA	Output	PCM Data Transmit
34	FS	Input	PCM Frame Sync
35	DVDD	Power	Digital 3.3 V supply input
36	I/O4	I/O	General purpose Input/ Output
37	CSMODE	Input	Mode input for multiple devices
38	AVDD	Power	Analog 3.3 V supply input
39	AGND	Power	Analog ground return for AVDD
40	RSVD	Open	Reserved. Make no connections to this pin
41	RING	Output	RING-lead (B) output to the 2-wire line
42	RSVD	Open	Reserved. Make no connections to this pin
43	TIP	Output	TIP-lead (A) output to the 2-wire line
45	VBAT	Power	Tracking negative battery supply. Provides power for the line driver
46	RSVD	Open	Reserved. Make no connections to this pin
47	BGND	Power	Battery ground return for VBAT. Connect to AGND
48	AVDD	Power	Analog 3.3 V supply input
–	EXPOSED PAD (EPAD)	Power	Exposed pad substrate connection. This pad is at AGND ground potential and must be soldered to the PCB and connected by multiple vias to a heatsink area on the bottom of the board and to the ground plane.

Table 23 - Le89156 Pin Descriptions (Continued)

9.0 Application Circuits

9.1 Line Interface

Figure 42 below shows a typical line interface circuit for the Le89156 Single Channel Wideband FXS. Decoupling, filtering, and reference generation components are also shown. The switching regulator circuit is shown separately. It may be either an inverting-boost (Figure 43, on page 60) for lower cost or a flyback (Figure 44, on page 63) for higher efficiency and/or a lower V_{SW} voltage input.

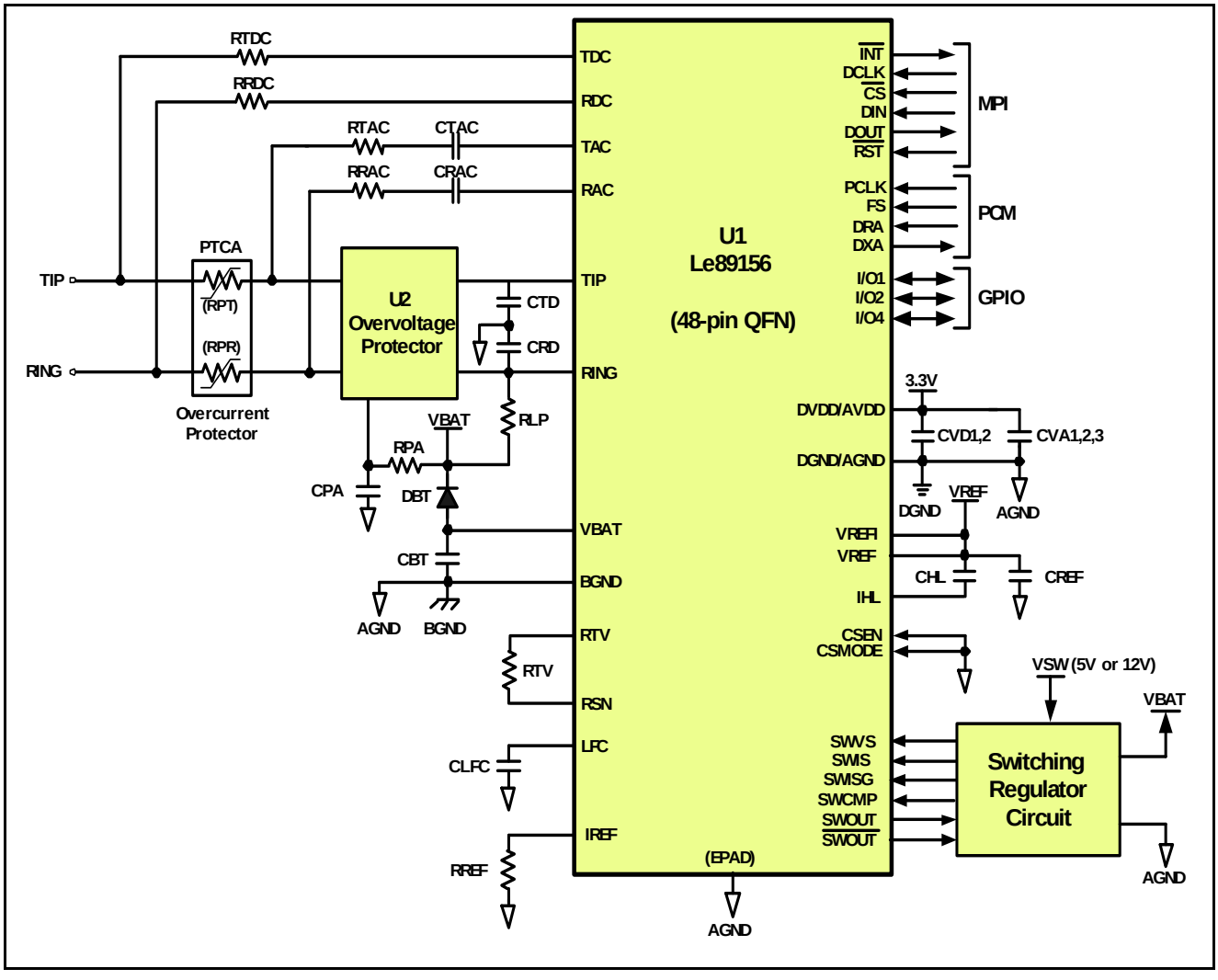


Figure 42 - Le89156 Line Interface Circuit

9.1.1 Le89156 Line Interface Circuit Bill of Materials

Qty.	Item	Type	Value	Tol.	Rating	Size	Notes
2	CBT, CPA*	Ceramic Capacitor	0.1 µF, X7R	20%	100 V	0805	*1.*
3	CHL, CLFC, CVA1	Ceramic Capacitor	4.7 µF, X5R	20%	6.3 V	0603	
2	CRAC, CTAC	Ceramic Capacitor	0.068 µF, X7R	10%	100 V	0805	
2	CRD, CTD	Ceramic Capacitor	0.022 µF, X7R	10%	100 V	0603	
1	CREF	Ceramic Capacitor	1.0 µF, X5R	20%	6.3 V	0603	
2	CVA2, CVA3	Ceramic Capacitor	0.1 µF, X7R	20%	6.3 V	0402	
2	CVD1, CVD2	Ceramic Capacitor	0.01 µF, X7R	10%	16 V	0402	
1	DBT	Diode	*BAS21*		0.2 A/200 V	SOT-23	
1	PTCA*	Dual PTC Thermistor	25 Ω, 0.13 A Hold	20%	230V / 2.8A		*1., 2.*
1	RLP	Resistor	150 KΩ	1%	150 V	0805	*3.*
1	RPA*	Resistor	4.7 kΩ	5%	150 V	0805	*1.*
2	RPR, RPT	Resistor	24.9 Ω	1%	1/4 W	1206	*2.*
2	RRAC, RTAC	Resistor	3.01 kΩ	1%	150 V	0805	
2	RRDC, RTDC	Resistor	402 KΩ	1%	200 V	1206	
1	RREF	Resistor	75.0 kΩ	1%	1/10 W	0603	
1	RTV	Resistor	47.5 kΩ	1%	1/10 W	0603	
1	U1	IC, Single Channel Wideband FXS	*Microsemi Le89156PQC*		-100 V	QFN-48	
1	U2*	IC, Programmable TVS SLIC Protector	*Bourns TISP61089BD* or *STM LCP1531RL*		-150 V	SOIC-8	*1.*

Notes:

1. *Items with an asterisk (*) are optional protection components. The values shown here are typical for applications requiring ITU K.21 Basic Level compliance. Please check with Microsemi CMPG Customer Applications for compliance with other safety standards.*
2. *Populate either PTCA or RPR and RPT, but not both line items. PTCA is recommended for applications requiring power cross protection and for compliance with ITU-T K.21 (Basic Level) or Telcordia GR-1089 (Intra-Building). Recommended PTCA selections are Semitel SCT250D, Bourns CMF-SDP25-2, and TDK-EPC B59825T1120A062*
3. *Optional - populate for Low Power Standby support*

9.2 Inverting-Boost Switching Regulator Circuit Example

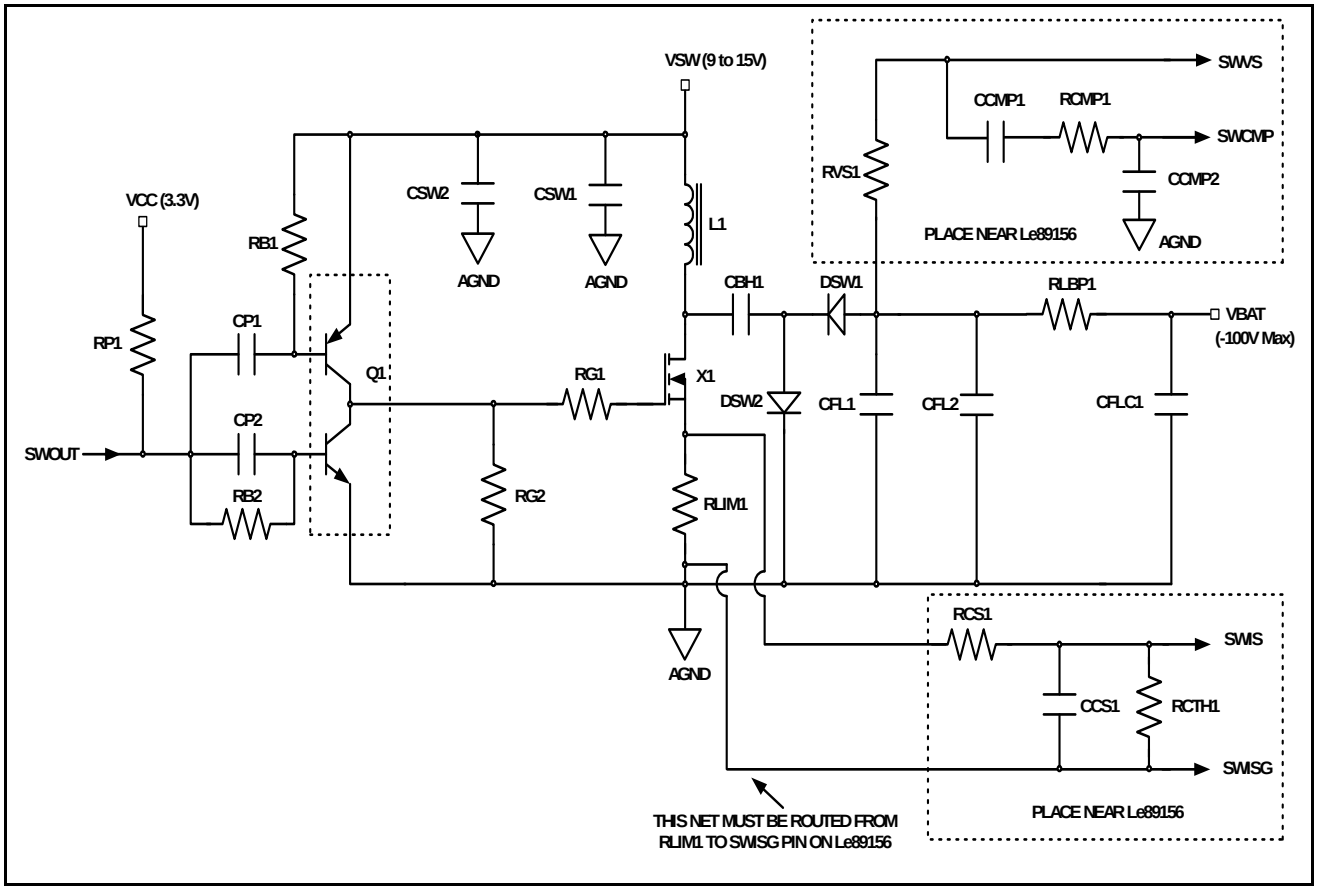


Figure 43 - 12 V Inverting-Boost Switching Regulator Circuit (60 Vrms Ringing Full Tracking)

9.2.1 Inverting-Boost Switching Regulator Circuit Bill of Materials

Qty.	Item	Type	Value	Tol.	Rating	Size	Notes
1	CBH1	Ceramic Capacitor	0.22 µF, X7R	20%	100 V	0805 or 1206	
1	CCMP1	Ceramic Capacitor	4700 pF, X7R	10%	25 V	0402	
1	CCMP2	Ceramic Capacitor		10%	25 V	0402	Do not populate
1	CCS1	Ceramic Capacitor	220 pF, C0G or X7R	10%	25 V	0402	
2	CFL1, CFLC1	Ceramic Capacitor	1.0 µF, X7R	20%	100 V	1206	
1	CFL2	Ceramic Capacitor	1.0 µF, X7R	20%	100 V	1206	Do not populate
2	CP1, CP2	Ceramic Capacitor	470 pF, C0G or X7R	10%	25 V	0402	
1	CSW1	Ceramic Capacitor	10 µF, X5R or X7R	20%	25 V	1206	
1	CSW2	Ceramic Capacitor	0.1 µF, X7R	20%	25 V	0603	
2	DSW1, DSW2	Ultra-Fast Recovery Rectifier	t_{rr} < 30 nS		1 A/ 200 V	SMA	*ES1D*
1	L1	Inductor	6.8 µH, Shielded, I_{SAT} > 3.5A	20%	3.5A	8x8x4 mm	*Taiyo Yuden NR8040T6R8N*, *TDK VLP8040T-6R8M* or equivalent
1	Q1	Dual Transistor	General Purpose NPN and PNP		0.2 A/ 40 V	SOT-363-6 / SC-70-6	*Fairchild FFB3946*, *ON Semi MBT3946DW* or equivalent
1	RB1	Resistor	560 Ω	5%	1/10 W	0603	
1	RB2	Resistor	2.2 KΩ	5%	1/16 W	0402	
1	RCMP1	Resistor	402 KΩ	5%	1/16 W	0402	
2	RCS1, RCTH1	Resistor	1.00 KΩ	1%	1/16 W	0402	
1	RG1	Resistor	10 Ω	5%	1/16 W	0402	
2	RG2, RP1	Resistor	10 KΩ	5%	1/16 W	0402	
1	RLBP1	Resistor	20 Ω	5%	1/4 W	1206	1.
1	RLIM1	Current Sense Resistor	0.05 Ω	1%	1/2 W	1206	*Stackpole CSR1206FK50L0* or equivalent
1	RVS1	Resistor	402 KΩ	1%	150 V	0805	
1	X1	MOSFET, N-Channel	$R_{DS\ (ON)}$ < 800 m Ω, Q_g < 15nC		>1A/ 150 V	TSOP-6 or SOT-223	2., 3., *Fairchild FDC2512, FDT86244,Vishay Si3440DV-T1,* or equivalent

Notes:

1. *Populate a 470 µH, 60 mA, size 1210 inductor at this location if better EMC filtering is required.*
2. *For 50 V_{RMS} maximum ringing, 100 V-rated Avalanche-rated MOSFETs may be used. Recommended devices include Fairchild FDT86113LZ and FQT7N10 LTF.*
3. *Avalanche- or UIS-rated MOSFETs are recommended for greater reliability.*

9.2.2 Inverting-Boost Switching Regulator Circuit Performance

Input Range:	9 V_{DC} to 15 V_{DC}
Supply Efficiency:	The efficiency will vary with load and with input voltage. For a nominal 12 V_{DC} input, the efficiency range is typically 50% to 80% under load
Typical Switcher Input Power (P_{SW}): (V_{SW} = 12V_{DC})	Disconnect with supplies on, but no DC feed to line: 30 mW Low Power Standby (Idle/On-Hook): 68 mW Standby (Idle / On-Hook): 126 mW OHT or OHT Pol. Rev.: 275 mW Talk (Off-Hook): I_{LA} = 26 mA, V_{BAT} = -30 V_{DC}, R_L = 600 Ω: 1.13 W Ringing, 40 V_{RMS} into a 1 REN load: 1.09 W Ringing, 55 V_{RMS} into a 3 REN load: 2.53 W
Maximum Ringing Voltage:	60 V_{RMS} (85 V_{PK})
Maximum Ringing Load Drive:	5 REN
Output Regulation:	1.0% with 12 V_{DC} input and -95 V_{DC} output load varied from 0 to 30 mA
Output Accuracy:	-4 V_{DC} to +4 V_{DC} from the fixed ringing voltage setting
Operating Frequency:	Disconnect, Low Power Standby and Standby: 24 kHz All other states: 300 kHz

9.3 Flyback Switching Regulator Circuit Example

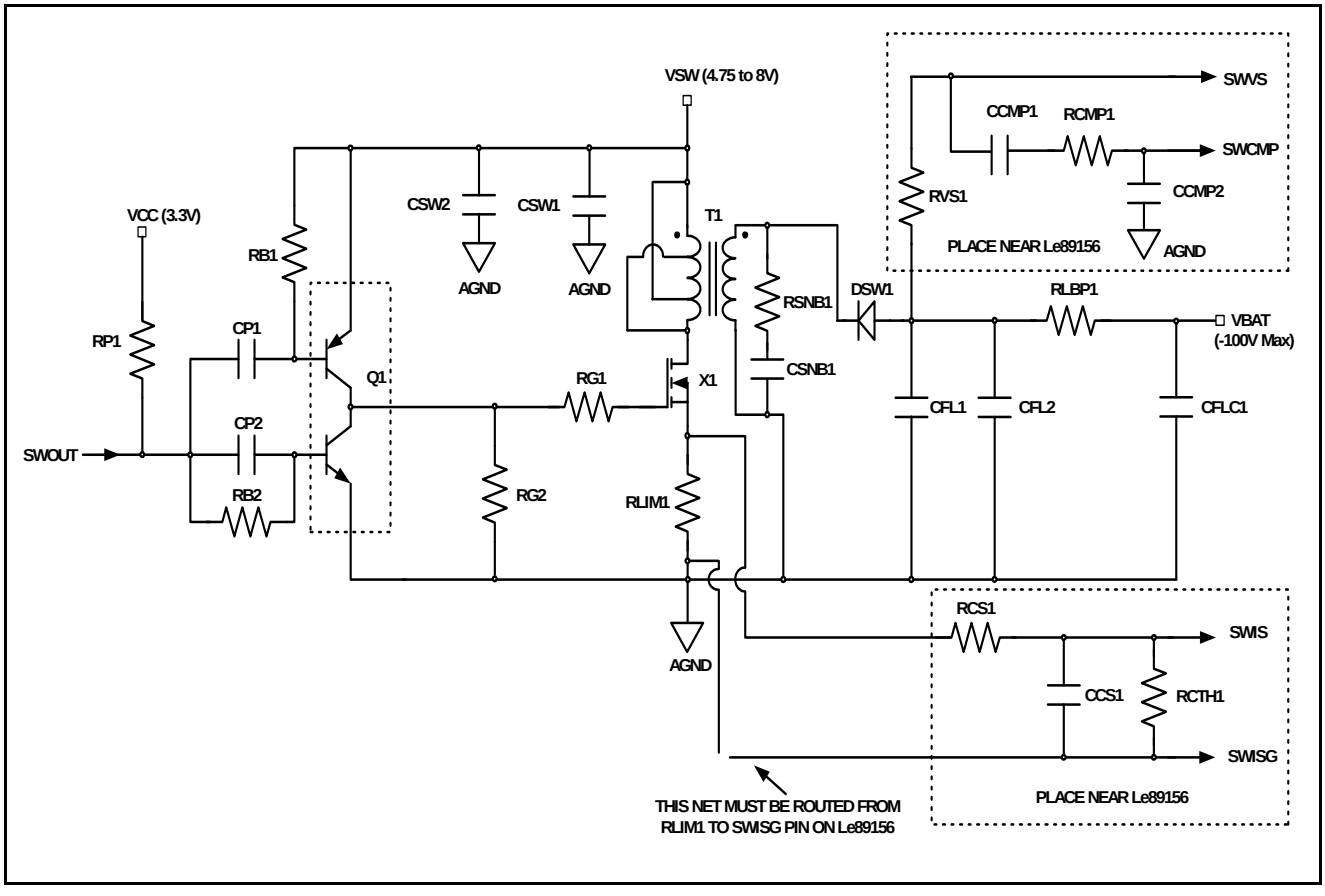


Figure 44 - 5 V Flyback Switching Regulator Circuit Example (65 Vrms Ringing Full Tracking)

9.3.1 Flyback Switching Regulator Circuit Bill of Materials

Qty	Item	Type	Value	Tol.	Rating	Size	Notes
1	CCMP1	Ceramic Capacitor	0.047 µF, X7R	10%	16 V	0402	
1	CCMP2	Ceramic Capacitor		10%	25 V	0402	Do not populate
1	CCS1	Ceramic Capacitor	220 pF, C0G or X7R	10%	25 V	0402	
2	CFL1, CFLC1	Ceramic Capacitor	1.0 µF, X7R	20%	100 V	1206	
1	CFL2	Ceramic Capacitor	1.0 µF, X7R	20%	100 V	1206	Do not populate
2	CP1, CP2	Ceramic Capacitor	470 pF, C0G or X7R	10%	25 V	0402	
1	CSNB1	Ceramic Capacitor	47 pF, C0G	10%	200 V	0805	
1	CSW1	Ceramic Capacitor	10 µF, X5R or X7R	20%	16 V	1206	
1	CSW2	Ceramic Capacitor	0.1 µF, X7R	20%	16 V	0603	
1	DSW1	Ultra-Fast Recovery Rectifier	t_{rr} < 30 nS		1 A/ 200 V	SMA	*ES1D*
1	Q1	Dual Transistor	General Purpose NPN and PNP		0.2 A/ 40 V	SOT-363-6 / SC-70-6	*Fairchild FFB3946*, *ON Semi MBT3946DW,* or equivalent
1	RB1	Resistor	560 Ω	5%	1/10 W	0603	
1	RB2	Resistor	2.2 KΩ	5%	1/16 W	0402	
1	RCMP1	Resistor	200 KΩ	5%	1/16 W	0402	
1	RCS1	Resistor	1.00 KΩ	1%	1/16 W	0402	
1	RCTH1	Resistor	2.00 KΩ	1%	1/16 W	0402	
1	RG1	Resistor	10 Ω	5%	1/16 W	0402	
2	RG2, RP1	Resistor	10 KΩ	5%	1/16 W	0402	
1	RLBP1	Resistor	20 Ω	5%	1/4 W	1206	1.
1	RLIM1	Current Sense Resistor	0.015 Ω	1%	1/2 W	1206	*Stackpole CSR1206FK15L0* or equivalent
1	RSNB1	Resistor	1.0 KΩ	5%	1/8 W	0805	
1	RVS1	Resistor	402 KΩ	1%	150 V	0805	
1	T1	Flyback Transformer	Custom			EE8.8	*UMEC TG-UTB1473s* or *Sumida C8102*
1	X1	MOSFET, N-Channel, Logic Level	$R_{DS\ (ON)}$ < 150 m Ω, Q_g < 15nC		>3A/ 60 V	SOT-223 or SOIC-8	2., *Diodes DMN6068SE-13, ON Semi NTF3055L108*, *A&O AO4440*, or equivalent

Notes:

1. *Populate a 470 µH, 60 mA, size 1210 inductor at this location if better EMC filtering is required.*
2. *Avalanche- or UIS-rated MOSFETs are recommended for greater reliability.*

9.3.2 Flyback Switching Regulator Performance

Input Range:	4.75 V_{DC} to 8.0 V_{DC} or 9 V_{DC} to 16 V_{DC}
Supply Efficiency:	The efficiency will vary with load and with input voltage. For 5 V_{DC} input, the efficiency range is typically 55% to 70% under load. For 12 V_{DC} input, the efficiency range is typically 60% to 80% under load.
Typical Switcher Input Power (P_{SW}): (V_{SW} = 5V_{DC}, Full Tracking)	Disconnect with supplies on, but no DC feed to line: 30 mW Low Power Standby (Idle / On-Hook): 86 mW Standby (Idle / On-Hook): 144 mW OHT or OHT Pol. Rev.: 275 mW Talk (Off-Hook): I_{LA} = 26 mA, V_{BAT} = -30 V_{DC}, R_L = 600 Ω: 1.28 W Ringing, 55 V_{RMS} into a 3 REN load: 3.6 W
Typical Switcher Input Power (P_{SW}): (V_{SW} = 12V_{DC}, Full Tracking)	Disconnect with supplies on, but no DC feed to line: 30 mW Low Power Standby (Idle / On-Hook): 74 mW Standby (Idle / On-Hook): 142 mW OHT or OHT Pol. Rev.: 315 mW Talk (Off-Hook): I_{LA} = 26 mA, V_{BAT} = -30 V_{DC}, R_L = 600 Ω: 1.06 W Ringing, 55 V_{RMS} into a 3 REN load: 2.33 W
Maximum Ringing Voltage:	65 V_{RMS} (92 V_{PK})
Maximum Ringing Load Drive:	5 REN
Output Regulation:	1.0% with 12 V_{DC} input and -95 V_{DC} output load varied from 0 to 30 mA
Output Accuracy:	-4 V_{DC} to +4 V_{DC} from the fixed ringing voltage setting
Operating Frequency:	Disconnect, Low Power Standby, and Standby (On-Hook Idle): 24 kHz On-Hook Transmission and Talk (Off-Hook): 96 kHz Ringing: 384 kHz

10.0 Package Outline

The package outline and recommended land pattern of the Le89156 Single Channel Wideband FXS are described in this section.

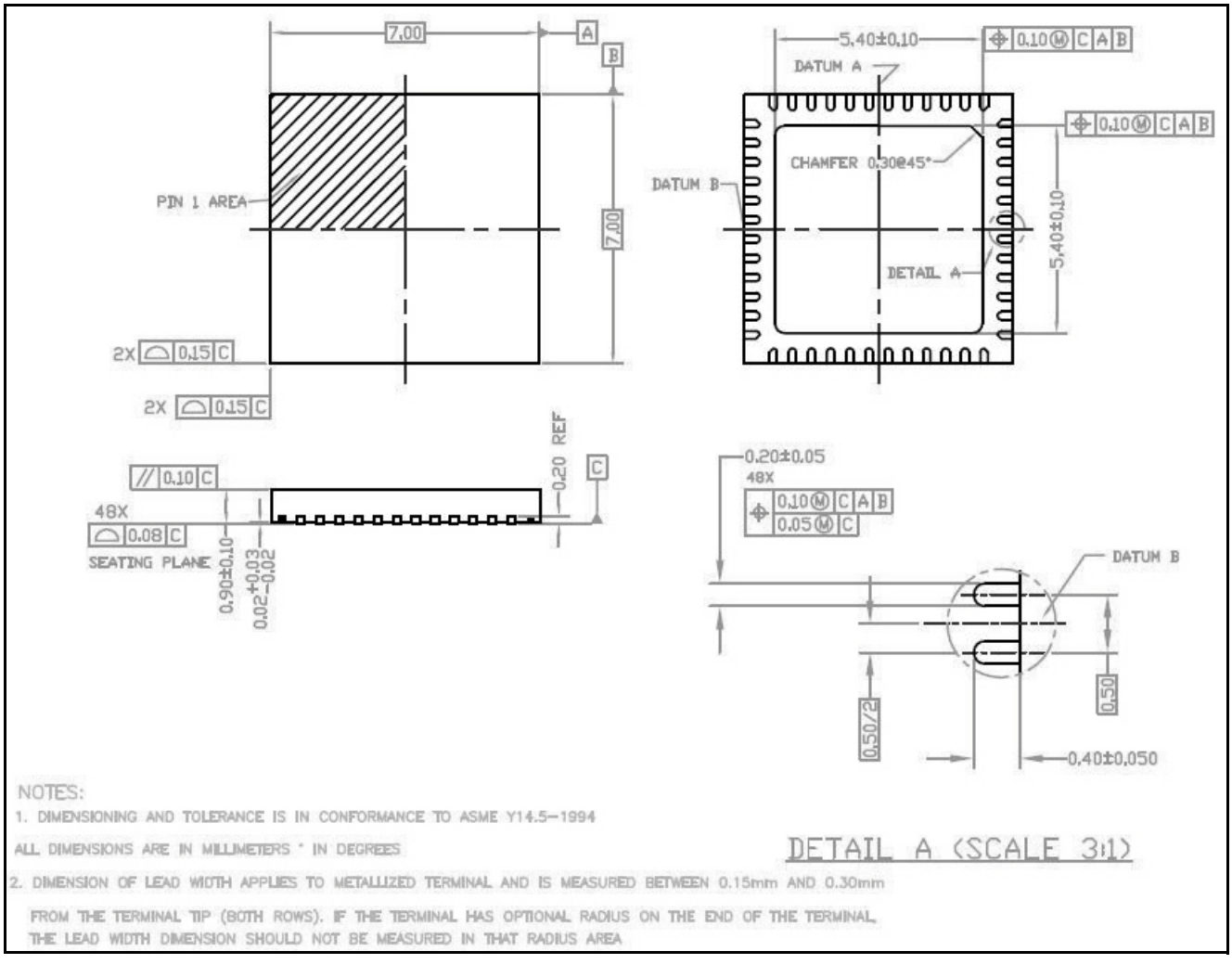
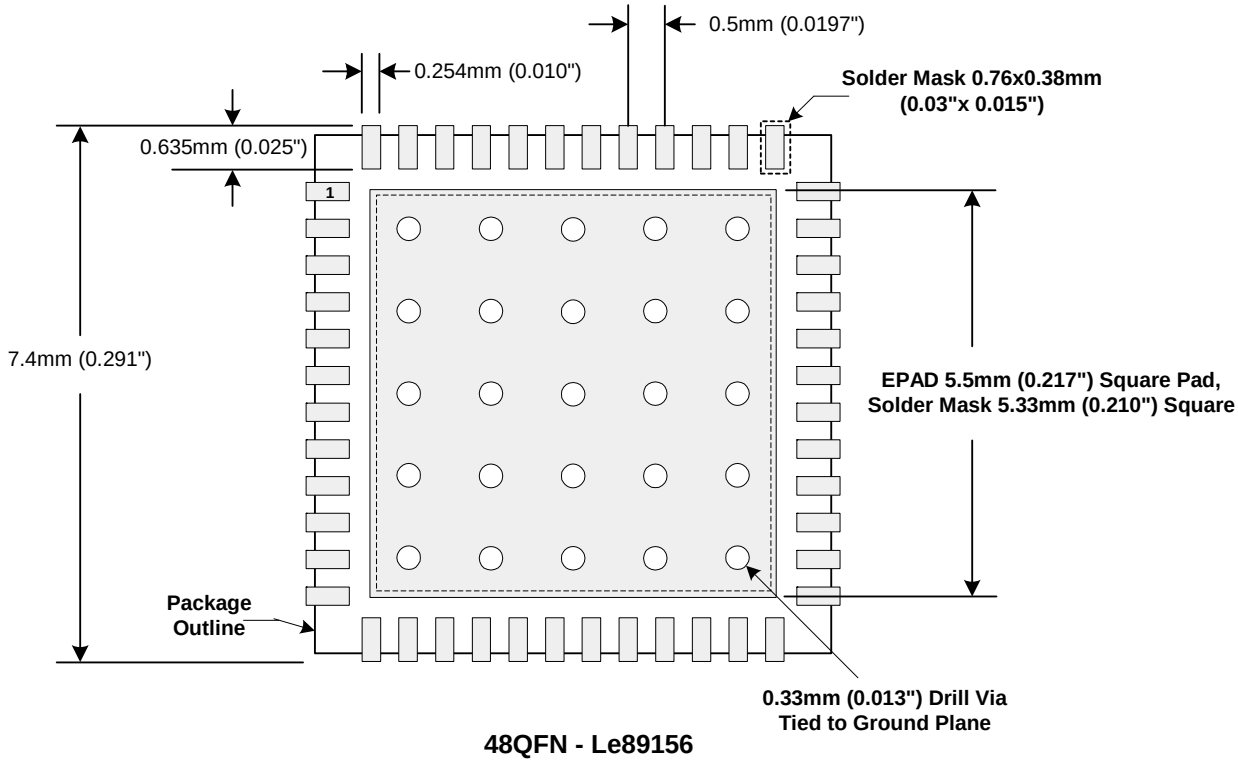


Figure 45 - Le89156 (QFN-48) Package Drawing



48QFN - Le89156
7mm x 7mm, 0.5mm pitch

NOTES:

1. Minimum spacing between pins and the EPAD must be 0.3mm (0.076")
2. The thermal pad must be present on all layers
3. Connections to ground should be solid. No thermal patterns.
4. Controlling dimensions are in mm

Figure 46 - Recommended Land Pattern

11.0 Related Collateral

11.1 Documentation

- **Le89156 Single Channel Wideband FXS Product Brief**
  - Document ID#: 141475
- **VE8910 1FXS Chipset Data Sheet**
  - Document ID#: 081575
- **VoicePath API-II CSLAC Reference Guide**
  - Document ID#: 081301
- **VeriVoice Test Suite Software Product Preview**
  - Document ID#: 081535
- **Le880SLVV & Le890SLVV VeriVoice Auditor Test Suite Software for VE880 and VE890 Series Data Sheet**
  - Document ID#: 081489
- **Le890SLVVP VeriVoice Professional Test Suite Software for VE890 Series Data Sheet**
  - Document ID#: 132063
- **VeriVoice Manufacturing Test Package Reference Guide**
  - Document ID#: 141005
- **Microsemi Telephony Applications Platform (ZTAP) User's Guide**
  - Document ID#: 136057
- **Le71HR8927G Reference Design User Guide for the Le89156 Single Channel Wideband FXS**
  - Document ID#: 142126

11.2 Development Hardware

- **Microsemi Telephony Applications Platform (ZTAP) Kit - OPN: Le71HK0004**
  - The Le71HK0004 *ZTAP* is a Linux-based development platform for the *VE890 Series* and other Microsemi voice product families.
- **Evaluation Module - OPN: Le71HR8927G**
  - The Le71HR8927G Evaluation Module with two Le89156 devices with and associated external components and protection circuit. This module measures 50 x 57 mm and plugs into the *ZTAP* board's *SM2* receptacle. Each FXS channel on this module can generate up to 85-V_{PK} ringing with 5 REN drive capability.

11.3 Software

- **VoicePath API-II - OPN: Le71SK0002**
  - The *VP-API-II* is a set of 'C' source used by the host application to interface to the *VE890 Series* and other Microsemi voice product families. A signed Software License Agreement (SLA) is required.
- **VoicePath API-II Lite - OPN: Le71SDKAPIL**
  - The *VP-API-II Lite* is identical to *VP-API-II*, with reduced functionality. *VP-API-II Lite* does not support cadencing, Caller ID, or FXO signal generation (DTMF, Flash Hook, or Dial Pulse). A Software License Agreement (SLA) is not required for *VP-API-II Lite*.
- **VoicePath Profile Wizard - OPN: Le71SDKPRO**
  - The *VP Profile Wizard* is a *Microsoft Windows* GUI application that aids in the organization and creation of country profiles used in the *VP-API-II* into a single project file.
- **VeriVoice Auditor Test Suite - OPN: Le890SLVV**
  - The *VeriVoice Auditor Test Suite* for the *VE890 Series* is a subscriber line (FXS) test software package for VoIP equipment. It features all the outward tests of the *Telcordia GR-909-CORE* standard and returns pass / fail results. *VeriVoice Auditor* is one of the industry's most cost effective VoIP line testing solutions.
- **VeriVoice Professional Test Suite - OPN: Le890SLVVP**
  - The *VeriVoice Professional Test Suite* for the *VE890 Series* is a subscriber line (FXS) test software package for VoIP equipment. It features all the outward tests of the *Telcordia GR-909-CORE* standard and other subscriber line tests with measured results. *VeriVoice Professional is* one of the industry's most advanced VoIP line testing solutions.
- **VeriVoice Manufacturing Test Package - OPN: ZLS800VVMT**
  - The *VeriVoice Manufacturing Test Package* for the *VE880 and VE890 Series* is a portable, platform-independent C source code module which performs factory testing and calibration of assembled boards with Microsemi FXS voice devices
- **ZTAP Support Package - OPN: Le71SDKZTAP**
  - This software package contains system files for the *ZTAP* board and *Microsoft Windows* USB drivers for communicating with it.
- **Microsemi Voice Toolkit - OPN: Le71SDKTK**
  - The Microsemi Voice Toolkit (*MiToolkit*) is a scripting environment that allows for the development and distribution of Tcl related collateral for Microsemi voice hardware and software products. *MiToolkit* includes several custom Tcl extension packages, i.e., *VP-Script* and *Mini-PBX*.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

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