Si321x User's Quick Reference Guide

1. Introduction

This document describes the initiation and operation of the single-channel ProSLIC™ family of parts in short loop telecom applications. The indirect register address values outside of parentheses in this document refer to the Si3210 and Si3211. The indirect register address values inside parentheses are for the Si3215 and Si3216. A full understanding of the ProSLIC family requires the designer to read the appropriate data sheet as well as applications notes for specific operation. Example register settings are listed in Table 1 and Table 2 on pages 4 and 8.

1.1. Understanding the Telephony Requirement

The telephony features and parametric requirements vary from country to country. Therefore, it is important to first consider these features and parameters for a SLIC. Critical parameters include ringing, on-hook voltage, off-hook current, two-wire impedance, transmit and receive gains, four-wire return loss, and call progress tones. All parameters are defined in the ProSLIC by using software control. This section describes the registers associated with each parameter. See the appropriate ProSLIC data sheet to calculate values.

1.1.1. Ringing Parameters

Ringing voltage and frequency must be selected to ensure that the maximum ringing load at the end of the longest loop is driven with sufficient signal. North American applications require 40 V_{rms} at 20 Hz across a 5 REN (ringer equivalent number) load. Assuming the short loop application consists of a subscriber loop length of 2000 ft. or less, the ringing requirement from the ringing source is approximately 46 V_{rms} or 65 V_{PK} of balanced sinusoidal ringing. The ProSLIC is capable of generating ringing amplitudes from 90 V_{PK} using sinusoidal or trapezoidal wave shapes. The ProSLIC ringing waveform parameters are set by indirect registers 19–22 (6–9 for Si3215/16). Ringing waveshape and cadence parameters are defined by direct registers 34, 48–51, and 64. Refer to the "Ringing Generation" section in the ProSLIC data sheet for equations and specific information about setting these registers.

1.1.2. Linefeed Parameters

On-hook voltage, also called open circuit voltage, signals all terminals sharing the TIP and RING circuit that the line is not in use. A general standard for this voltage is 48 V nominal with a 42.5 V minimum. ProSLIC direct register 72 (0x48) sets this parameter. Off-hook loop current is the value of current provided by the SLIC to power the phone when off-hook. For global short loop applications, 20 mA to 23 mA is common. ProSLIC direct register 71 (0x47) sets this parameter.

1.1.3. AC Characteristics

Two-wire impedance is the voice-band impedance synthesized by the SLIC. It is measured by the two-wire return loss requirement as specified in each telephony market. The ProSLIC provides eight discrete selections for two-wire impedance synthesis. ProSLIC direct register 10 (0x0A) selects this parameter. Capacitive compensation can also be selected in direct register 10 (CLC). A line capacitance compensation setting of 10 nF provides compensation for the typical ProSLIC application circuit.

Transmit and receive gain are set to achieve overall relative levels from the two-wire domain to the digital PCM domain and vice versa. Coarse and fine gain adjustment is found in the ProSLIC. ProSLIC direct register 9 and indirect registers 26 and 27 (13 and 14 for the Si3215 or Si3216) set the transmit and receive gain.

Four-wire return loss (often called the transhybrid balance or hybrid echo cancellation) is the measure of cancellation of reflected signal originating from the receive path. Typical telephony requirements specify a four-wire return loss of greater than 22 dB. Four-wire return loss is achieved by subtracting a portion of the original receive signal from the transmit path. For the short loop case, it is assumed that the impedance used to measure four-wire return loss is equal to the SLIC synthesized impedance. Therefore, the nominal echo signal will be –6 dB of the original signal. The ProSLIC HYBA block sets the amount of receive signal that is subtracted from the transmit path. ProSLIC direct register 11 (0x0B) sets this parameter.

Call progress tones are necessary for subscriber line functionality. The ProSLIC generates single and dual tones for call progress functions (dial tone, DTMF, etc.). ProSLIC indirect registers 13–18 (0–5 for Si3215/16) set the parameters for tone generation.

1.1.4. Battery Supply Parameters

The ProSLIC's linefeed power supply is based on subscriber line parameters. The most negative battery, VBATH, is selected based on minimum ringing requirements. Ringing requirements are defined by minimum ringing potential and maximum ringing load (minimum ringing impedance). A typical application in North America requires V_{rms} into a load of 5 REN at the end of the longest possible loop. This scenario forces the calculation of minimum ringing source potential. This minimum ringing source potential defines the minimum VBATH.

Example:

- Requirement: 45 V_{rms} into 5REN at a maximum TIP/RING loop impedance of 100 Ω.
- 5 REN is defined in North America as 1386 Ω in series with 40 µF (1400 Ω at 20 Hz).
- 45 V_{rms} at the end of 100 Ω wire into 1400 Ω at 20 Hz requires a 48.2 V_{rms} source.
- A 48.2 V_{rms} source is 68.2 V_{PK} or 68.2 V_{PP} per TIP or RING from a balanced source.
- The requirement of 68.2 V_{PK} plus SLIC output circuit overhead voltage defines the minimum required VBATH.
- An adequate linefeed circuit overhead voltage of 7.3 V must be added.
- The minimum required VBATH is 75 VDC.

The minimum off-hook battery, VBATL, is defined by the minimum supply rail required to provide sufficient overhead for transmission at the longest off-hook loop.

Example:

- Off-hook phone impedance: 430 Ω
- Maximum TIP/RING wire impedance: 100 Ω
- ProSLIC off-hook overhead voltage: V_{CM} and V_{OV}
- Typical loop current setting: 23 mA
- Minimum V_{BATL} = [23 mA x 530 Ω] + 3 V(V_{CM}) + 7.5 V(V_{OV}) = 23 V minimum

Application Note "AN45: Design Guide for the Si3210 DC-DC Converter" provides detailed guidance for Si3210/15/16 battery generation design and is available on the Silicon Labs web site, www.silabs.com.

1.1.5. External Component Considerations

The discrete transistors in the ProSLIC circuit provide high-voltage dc feed and ringing signals to telephone sets. Power dissipation must be considered for these transistors under abnormal fault conditions. The ProSLIC monitors the current and voltage of all transistors in the circuit and uses this information to select the OPEN mode and alert the local processor if power thresholds are exceeded. Indirect registers 32–34 (19–21 for Si3215/16) and 37–39 (24–26 for Si3215/16) set the power thresholds and power threshold filter coefficients. Direct register 19 sets the interrupt mask for the individual transistor power alarms. Register 22 indicates and clears the interrupt pending for a given transistor power alarm. A typical ProSLIC application requires the SOT23 package for Q1–4 and the SOT-223 package for Q5 and Q6. Refer to the ProSLIC Power Design Guide for calculating power coefficients and setting the associated indirect registers.

If the ProSLIC circuit is going to be used outside the commercial temperature range, the SOT89 package should be used for Q1 and Q2. This is due to the power dissipation during the ringing mode.

The Si3201 linefeed IC integrates the high-voltage discrete transfer circuit into a single device and may be used instead of the discrete solution. Consult the Si3210 or Si3215/16 data sheet for an explanation of the application circuit.

1.1.6. Digital Audio Interface

The PCM highway consists of time-multiplexed channels on a synchronous serial bus. Transmit and receive time slot selection must be done to assign each device non-overlapping channels on this PCM bus. The ProSLIC has a programmable clock slot for transmit and receive PCM. This allows the programming of a given ProSLIC's PCM channel (time slot) to begin on any clock slot relative to the 125 µs Frame Sync pulse. Registers 2–5 set the PCM clock slots.

For example:

- Frame Sync = 8 kHz, PCLK = 2.048 MHz
- Initial time slot begins on clock slot 0 (zero)
- Eight ProSLIC channels
- ProSLICs can be set to clock slots 0, 8, 16, 24, 32, 40, 48, and 56

1.1.7. Calibration

Calibrate all circuits of the ProSLIC for accurate parametric operation. Registers 96 and 97 enable and execute calibration routines. After calibration is initiated, Register 96 indicates the completion of the calibration routines.

1.2. ProSLIC Initialization

Perform the following steps:

1. Hold $\overline{\text{RESET}}$ low, and apply power.
2. PCLK and FS must be present and stable.
3. Preset $\overline{\text{CS}}$ and SCLK to high state (if SCLK is to be static between $\overline{\text{CS}}$s).
4. $\overline{\text{CS}}$ should be deasserted a minimum of 250 ns between access bytes.
5. Release $\overline{\text{RESET}}$.
6. Wait 2 ms (16 FS) after releasing $\overline{\text{RESET}}$ before communicating to the ProSLIC.
7. Set Daisy Chain mode if used (direct register 0, 3-byte access from here on in daisy chain mode).
8. Read direct registers 8, 11, and 64 to verify communication with ProSLIC values should be 0x02, 0x33, and 0x00.
9. Write all initial indirect registers (refer to ProSLIC data sheet, direct registers 28–31). Write indirect registers 0–41, 43 and 99–104 (0–9, 13–27, 66, and 69–74 for Si3215/16). Write indirect registers 35–39 each to 0x8000 (22–26 for Si3215/16). (Save the defined values for step 27.)
10. Write Direct Register 8 to 0. This will take ProSLIC out of Loopback mode. Write Direct Register 108 to 0xEB. (This turns on all the Rev E features).
11. Write Battery Voltages (direct registers 74, 75). (**Optional; refer to data sheet**)
12. Perform dc-dc calibration.
    a. Write direct Registers 92 and 93. (Refer to dc-dc converter spreadsheet.)
    b. Turn on dc-dc converter; clear direct Register 14, bit 4.
    c. Poll Register 82, and wail until battery voltage is at the desired value.
    d. Perform dc-dc converter calibration; set direct Register 93, bit 7.
    e. Poll DR93 for calibration completion.
13. Write Direct Register 64 to 0. Set SLIC to Open State.
14. Perform SLIC calibration (0x1E to direct register 97 then 0x47 to 96).
15. Poll direct register 96 for completion of calibration.
16. Perform the Manual Calibration Procedure described in the next section.
17. Set Direct Register 23, bit 2. (Common mode calibration error interrupt enable) Watch for a ProSLIC interrupt during calibration. If this occurs, there was an error during calibration.
18. Perform SLIC calibration (0x01 to direct register 97 then 0x40 to 96). Before performing this calibration, monitor direct register 68 to ensure line is on-hook.
19. Poll direct register 96 for completion of calibration.
20. Flush out energy accumulators. For Si3210 and Si3211, write indirect registers 88–95, 97, 193–211 to 0x0000. For Si3215 and Si3216, write indirect registers 75–82, 84, and 208–211 to 0x0000.
21. Write Direct Registers 19-23 to 0xFF to clear and enable interrupts (**Optional; refer to data sheet**). Writing a read-only bit has no effect.
22. Write PCM mode and clock slot assignment (direct registers 2–5, then set and enable with direct register 1; refer to data sheet).
23. Initialize voice path (direct registers 8-11; refer to data sheet).
24. Initialize OSC1, OSC2, Ringing, Pulse Metering (direct registers 32-51; refer to data sheet).
25. "Write detect thresholds and filters (direct registers 63, 67, 69, 70) (**Optional; refer to data sheet**).
26. Write dc feed parameters (direct registers 65-67, 71-73) (**Optional; refer to data sheet**).
27. Write indirect registers 35–39 (22–26 for Si3215/16) to desired values. (Refer to data sheet).
28. Write all other direct registers and indirect registers that are different than default. (Refer to data sheet.)

1.3. Manual Calibration Procedure

Perform the following steps:

1. Write hex 1F to direct register 98. Wait 40 ms.
2. Read value of direct register 88. If the result value is greater than zero, decrement the value in direct register 98 by one. For example, if direct register 98 is equal to hex 1F and direct register 88 reads greater than zero, write direct register 98 to hex 1E. Wait at least 40 ms for each register write to take effect.
3. Repeat Step 2 until direct register 88 is equal to zero.
4. Write hex 1F to direct register 99. Wait 40 ms.
5. Read value of direct register 89. If the result value is greater than zero, decrement the value in direct register 99 by one. For example, if direct register 99 is equal to hex value 1F and direct register 89 reads greater than zero, write direct register 99 to hex 1E. Wait at least 40 ms for each register write to take effect.
6. Repeat step 5 until direct register 89 is equal to zero.

1.4. ProSLIC Operation

Perform the following steps:

1. Set operation mode (direct register 64).
2. Respond to interrupts (direct registers 18–20).
3. Read decoded DTMF (direct register 24).
4. Poll realtime loop status (direct register 68).
5. Generate pulse metering (direct register 35).
6. Poll line monitoring (direct registers 76–89, 94).

1.5. Conclusion

The ProSLIC is a highly-programmable, short loop telephony solution. Use this document (as well as the data sheet and other specific application notes) as a guide to operating the ProSLIC.

1.6. Register Description

Table 1 and Table 2 serve as guides for recommended settings under default conditions.

Table 1. Si321x Direct Registers

Direct Register		Default Value	Alternate Value	Type	Description
(decimal)	(hex)	(hex)	(hex)		
0	0x00	0x02		Initialization	Serial Interface
1	0x01	0x08	0x28	Initialization	PCM Mode
2	0x02	0x00		Initialization	PCM TX Clock Slot Low Byte (1 PCLK cycle/LSB)
3	0x03	0x00		Initialization	PCM TX Clock Slot High Byte
4	0x04	0x00		Initialization	PCM RX Clock Slot Low Byte (1 PCLK cycle/LSB)
5	0x05	0x00		Initialization	PCM RX Clock Slot High Byte
6	0x06	0x00		Normal Oper.	DIO Control (external battery operation, Si3211/12)
8	0x08	0x02	0x00	Initialization	Loopbacks (digital loopback default)
9	0x09	0x00		Initialization	Transmit and receive path gain and control
10	0x0A	0x08	0x28	Initialization	Two-wire impedance (600 Ω and enabled)
11	0x0B	0x33		Initialization	Transhybrid Balance/Four-wire Return Loss
14	0x0E	0x10		Initialization	Powerdown Control 1
15	0x0F	0x00		Initialization	Powerdown Control 2
18	0x12	0x00		Normal Oper.	Interrupt Register 1 (clear with 0xFF)
19	0x13	0x00		Normal Oper.	Interrupt Register 2 (clear with 0xFF)
20	0x14	0x00		Normal Oper.	Interrupt Register 3 (clear with 0xFF)
21	0x15	0x00	0xFF	Initialization	Interrupt Mask 1
22	0x16	0x00	0xFF	Initialization	Interrupt Mask 2
23	0x17	0x00	0xFF	Initialization	Interrupt Mask 3
24	0x18	0x00		Normal Oper.	DTMF Digit Decode Output
28	0x1C	0x00		Initialization	Indirect Data Low Byte
29	0x1D	0x00		Initialization	Indirect Data High Byte
30	0x1E	0x00		Initialization	Indirect Address

Note: Any register not listed is reserved and should not be used.

Table 1. Si321x Direct Registers (Continued)

Direct Register		Default Value	Alternate Value	Type	Description
(decimal)	(hex)	(hex)	(hex)		
31	0x1F	0x00		Initialization	Indirect Address Status
32	0x20	0x00		Init/Normal Oper.	Oscillator 1 Control—tone generation
33	0x21	0x00		Init/Normal Oper.	Oscillator 2 Control—tone generation
34	0x22	0x00		Initialization	Ringing Oscillator Control
35	0x23	0x00		Init/Normal Oper.	Pulse Metering Oscillator Control
36	0x24	0x00		Initialization	OSC1 Active Low Byte (125 μs/LSB)
37	0x25	0x00		Initialization	OSC1 Active High Byte (125 μs/LSB)
38	0x26	0x00		Initialization	OSC1 Inactive Low Byte (125 μs/LSB)
39	0x27	0x00		Initialization	OSC1 Inactive High Byte (125 μs/LSB)
40	0x28	0x00		Initialization	OSC2 Active Low Byte (125 μs/LSB)
41	0x29	0x00		Initialization	OSC2 Active High Byte (125 μs/LSB)
42	0x2A	0x00		Initialization	OSC2 Inactive Low Byte (125 μs/LSB)
43	0x2B	0x00		Initialization	OSC2 Inactive High Byte (125 μs/LSB)
44	0x2C	0x00		Initialization	Pulse Metering Active Low Byte (125 μs/LSB)
45	0x2D	0x00		Initialization	Pulse Metering Active High Byte (125 μs/LSB)
46	0x2E	0x00		Initialization	Pulse Metering Inactive Low Byte (125 μs/LSB)
47	0x2F	0x00		Initialization	Pulse Metering Inactive High Byte (125 μs/LSB)
48	0x30	0x00	0x80	Initialization	Ringing Osc. Active Timer Low Byte (2 s,125 μs/LSB)
49	0x31	0x00	0x3E	Initialization	Ringing Osc. Active Timer High Byte (2 s,125 μs/LSB)
50	0x32	0x00	0x00	Initialization	Ringing Osc. Inactive Timer Low Byte (4 s, 125 μs/LSB)
51	0x33	0x00	0x7D	Initialization	Ringing Osc. Inactive Timer High Byte (4 s, 125 μs/LSB)
52	0x34	0x00		Normal Oper.	FSK Data Bit
63	0x3F	0x54		Initialization	Ringing Mode Loop Closure Debounce Interval (1.25 ms/LSB)
64	0x40	0x00		Normal Oper.	Mode Byte—primary control
65	0x41	0x61		Initialization	External Bipolar Transistor Settings
66	0x42	0x03		Initialization	Battery Control
67	0x43	0x1F		Initialization	Automatic/Manual Control

Note: Any register not listed is reserved and should not be used.

Table 1. Si321x Direct Registers (Continued)

Direct Register		Default Value	Alternate Value	Type	Description
(decimal)	(hex)	(hex)	(hex)		
68	0x44	0x00		Normal Oper.	Loop Condition Indicators (for polling)
69	0x45	0x0A	0x0C	Initialization	Loop Closure Debounce Interval (1.25 ms/LSB)
70	0x46	0x0A		Initialization	Ring Trip Debounce Interval (1.25 ms/LSB)
71	0x47	0x00	0x01	Initialization	Off-Hook Loop Current Limit (20 mA + 3 mA/LSB)
72	0x48	0x20		Initialization	On-Hook Voltage (open circuit voltage) = 48 V (1.5 V/LSB)
73	0x49	0x02		Initialization	Common Mode Voltage—VCM = –3 V (–1.5 V/LSB)
74	0x4A	0x32		Initialization	VBATH (ringing) = –75 V (–1.5 V/LSB)
75	0x4B	0x10		Initialization	VBATL (off-hook) = –24 V (TRACK = 0) (–1.5 V/LSB)
76	0x4C	0x00		Informative	Power Monitor Pointer
77	0x4D	0x00		Informative	Power Monitor Output (30.4 mW/LSB)
78	0x4E	0x00		Informative	Loop Voltage (1.5 V/LSB, bit 6 = sign bit)
79	0x4F	0x00		Informative	Loop Current (1.25 mA/LSB, bit 6 = sign bit)
80	0x50	0x00		Informative	TIP Voltage (.376 V/LSB)
81	0x51	0x00		Informative	RING Voltage (.376 V/LSB)
82	0x52	0x00		Informative	VBAT Voltage 1 (.376 V/LSB)
83	0x53	0x00		Informative	VBAT Voltage 2 (.376 V/LSB) (0.625 μs delayed)
84	0x54	0x00		Informative	Q1 Current (.319 mA/LSB)
85	0x55	0x00		Informative	Q2 Current (.319 mA/LSB)
86	0x56	0x00		Informative	Q3 Current (37.6 μA/LSB)
87	0x57	0x00		Informative	Q4 Current (37.6 μA/LSB)
88	0x58	0x00		Informative	Q5 Current (.316 mA/LSB)
89	0x59	0x00		Informative	Q6 Current (.316 mA/LSB)
92	0x5C	0xFF	7F	Initialization	DC–DC Converter PWM Period (61.035 ns/LSB)
93	0x5D	0x14	0x19	Initialization	DC–DC Converter Min. Off Time (61.035 ns/LSB)
94	0x5E	0xFF		Informative	DC–DC Converter PWM Pulse (61.035 ns/LSB)
96	0x60	0x1F		Initialization	Calibration Control Register 1 (written second and starts calibration)
97	0x61	0x1F		Initialization	Calibration Control Register 2 (written before Register 96)

Note: Any register not listed is reserved and should not be used.

Table 1. Si321x Direct Registers (Continued)

Direct Register		Default Value	Alternate Value	Type	Description
(decimal)	(hex)	(hex)	(hex)		
98	0x62	0x10		Informative	Calibration result (see data sheet)
99	0x63	0x10		Informative	Calibration result (see data sheet)
100	0x64	0x11		Informative	Calibration result (see data sheet)
101	0x65	0x11		Informative	Calibration result (see data sheet)
102	0x66	0x08		Informative	Calibration result (see data sheet)
103	0x67	0x88		Informative	Calibration result (see data sheet)
104	0x68	0x00		Informative	Calibration result (see data sheet)
105	0x69	0x00		Informative	Calibration result (see data sheet)
106	0x6A	0x20		Informative	Calibration result (see data sheet)
107	0x6B	0x08		Informative	Calibration result (see data sheet)
108	0x63	0x00	0xEB	Initialization	Feature enhancement register

Note: Any register not listed is reserved and should not be used.

Table 2. Si321x Indirect Registers

Indirect Register Si3210/11/12		Indirect Register Si3215/16		Example Value	Type	Description
(decimal)	(hex)	(decimal)	(hex)	(hex)		
0	0x00			0x55C2	Initialization	DTMF Detection Coefficient
1	0x01			0x51E6	Initialization	DTMF Detection Coefficient
2	0x02			0x4B85	Initialization	DTMF Detection Coefficient
3	0x03			0x4937	Initialization	DTMF Detection Coefficient
4	0x04			0x3333	Initialization	DTMF Detection Coefficient
5	0x05			0x0202	Initialization	DTMF Detection Coefficient
6	0x06			0x0202	Initialization	DTMF Detection Coefficient
7	0x07			0x0198	Initialization	DTMF Detection Coefficient
8	0x08			0x0198	Initialization	DTMF Detection Coefficient
9	0x09			0x0611	Initialization	DTMF Detection Coefficient
10	0x0A			0x0202	Initialization	DTMF Detection Coefficient
11	0x0B			0x00E5	Initialization	DTMF Detection Coefficient
12	0x0C			0x0A1C	Initialization	DTMF Detection Coefficient
13	0x0D	0	0x00	0x7B30	Initialization	Oscillator 1 Frequency Coefficient (dial tone)
14	0x0E	1	0x01	0x0063	Initialization	Oscillator 1 Amplitude Coefficient 1 (dial tone)
15	0x0F	2	0x02	0x0000	Initialization	Oscillator 1 Phase Coefficient 1 (dial tone)
16	0x10	3	0x03	0x7870	Initialization	Oscillator 2 Frequency Coefficient (dial tone)
17	0x11	4	0x04	0x007D	Initialization	Oscillator 2 Amplitude Coefficient 1 (dial tone)
18	0x12	5	0x05	0x0000	Initialization	Oscillator 2 Phase Coefficient 2 (dial tone)
19	0x13	6	0x06	0x0000	Initialization	Ringing DC Offset (0 V Typical)
20	0x14	7	0x07	0x7EF0	Initialization	Ringing Frequency Coefficient (20 Hz)

Note: Any register not listed is reserved and should not be used. Indirect registers have specific bit offsets (refer to ProSLIC data sheet).

Table 2. Si321x Indirect Registers (Continued)

Indirect Register Si3210/11/12		Indirect Register Si3215/16		Example Value	Type	Description
(decimal)	(hex)	(decimal)	(hex)	(hex)		
21	0x15	8	0x08	0x0160	Initialization	Ringing Amplitude 1 (20 Hz)
22	0x16	9	0x09	0x0000	Initialization	Ringing Initialization 2 (0x0000 For Sinusoid)
23	0x17	10	0x0A	0x2000	Initialization	Pulse Metering Rise Time: $\frac{\left(\frac{1}{32767} \times \text{fullscale}\right)}{\text{LSB}}$
24	0x18	11	0x0B	0x2000	Initialization	Pulse Metering Oscillator Initialization Register
25	0x19	12	0x0C	0x0000	Initialization	Pulse Metering Oscillator Frequency Coefficient
26	0x1A	13	0x0D	0x4000	Initialization	Receive Path Digital Gain (0 dB)
27	0x1B	14	0x0E	0x4000	Initialization	Transmit Path Digital Gain (0 dB)
28	0x1C	15	0x0F	0x1000	Initialization	Loop Closure Threshold High (1.27 mA/LSB)
29	0x1D	16	0x10	0x3600	Initialization	Ring Trip Threshold (1.27 mA/LSB)
30	0x1E	17	0x11	0x1000	Initialization	Common Mode Low Threshold (0.375 V/LSB)
31	0x1F	18	0x12	0x0080	Initialization	Common Mode High Threshold (0.375 V/LSB)
32	0x20	19	0x13	0x07C0	Initialization	Power Threshold Q1, Q2 (30.4 mW/LSB)
33	0x21	20	0x14	0x376F	Initialization	Power Threshold Q3, Q4 (3.62 mW/LSB)
34	0x22	21	0x15	0x1B80	Initialization	Power Threshold Q5, Q6 (30.4 mW/LSB)
35	0x23	22	0x16	0x8000	Initialization	Loop Closure LPF Coefficient (800/ 2π4096) Hz/LSB
36	0x24	23	0x17	0x0320	Initialization	Ring Trip LPF Coefficient (800/ 2π4096) Hz/LSB
37	0x25	24	0x18	0x008C	Initialization	Power Threshold LPF Q1, Q2
38	0x26	25	0x19	0x008C	Initialization	Power Threshold LPF Q3, Q4

Note: Any register not listed is reserved and should not be used. Indirect registers have specific bit offsets (refer to ProSLIC data sheet).

Table 2. Si321x Indirect Registers (Continued)

Indirect Register Si3210/11/12		Indirect Register Si3215/16		Example Value	Type	Description
(decimal)	(hex)	(decimal)	(hex)	(hex)		
39	0x27	26	0x1A	0x0010	Initialization	Power Threshold LPF Q5, Q6
40	0x28	27	0x1B	0x00	Initialization	Common Mode Bias, ringing (1.5 V/LSB)
41	0x29	64	0x40	0x0C00	Initialization	DC–DC Minimum VOV (1.5 V/LSB)
43	0x2B	66	0x42	0x1000	Initialization	Loop Closure Threshold, low (1.27 mA/LSB)
99	0x63	69	0x45	0x00DA	Initialization	FSK 0 Bit, X Coefficient
100	0x64	70	0x46	0x6B60	Initialization	FSK 0 Bit Initialization Coefficient
101	0x65	71	0x47	0x0074	Initialization	FSK 1 Bit, X Coefficient
102	0x66	72	0x48	0x79C0	Initialization	FSK 1 Bit Initialization Coefficient
103	0x67	73	0x49	0x1120	Initialization	FSK 0 to 1 Transition Coefficient
104	0x68	74	0x4A	0x3BE0	Initialization	FSK 1 to 0 Transition Coefficient

Note: Any register not listed is reserved and should not be used. Indirect registers have specific bit offsets (refer to ProSLIC data sheet).

DOCUMENT CHANGE LIST

Revision 0.4 to Revision 0.5

- “Introduction” section updated
- “Understanding the Telephony Requirement” section updated
- “Ringing Parameters” section updated
- “AC Characteristics” section updated
- “Battery Supply Parameters” section updated
- “External Component Considerations” section updated
- “ProSLIC Initialization” steps updated
- “Register Description” section updated
- Table 1, Si321x Direct Registers, updated
- Table 2, Si321x Indirect Registers, updated

Revision 0.5 to Revision 0.51

- Updated “ProSLIC Initialization” steps.
- Updated “Manual Calibration Procedure” .

Revision 0.51 to Revision 0.52

- “Introduction” updated.
- “Battery Supply Parameters” section updated
- “External Component Considerations” section updated
- Table 2 updated.

Revision 0.52 to Revision 0.6

- "ProSLIC Initialization," on page 3 updated.

Revision 0.6 to Revision 0.7

- Removed references to Si3212.
- Corrected errors in step 9 in "ProSLIC Initialization," on page 3.

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